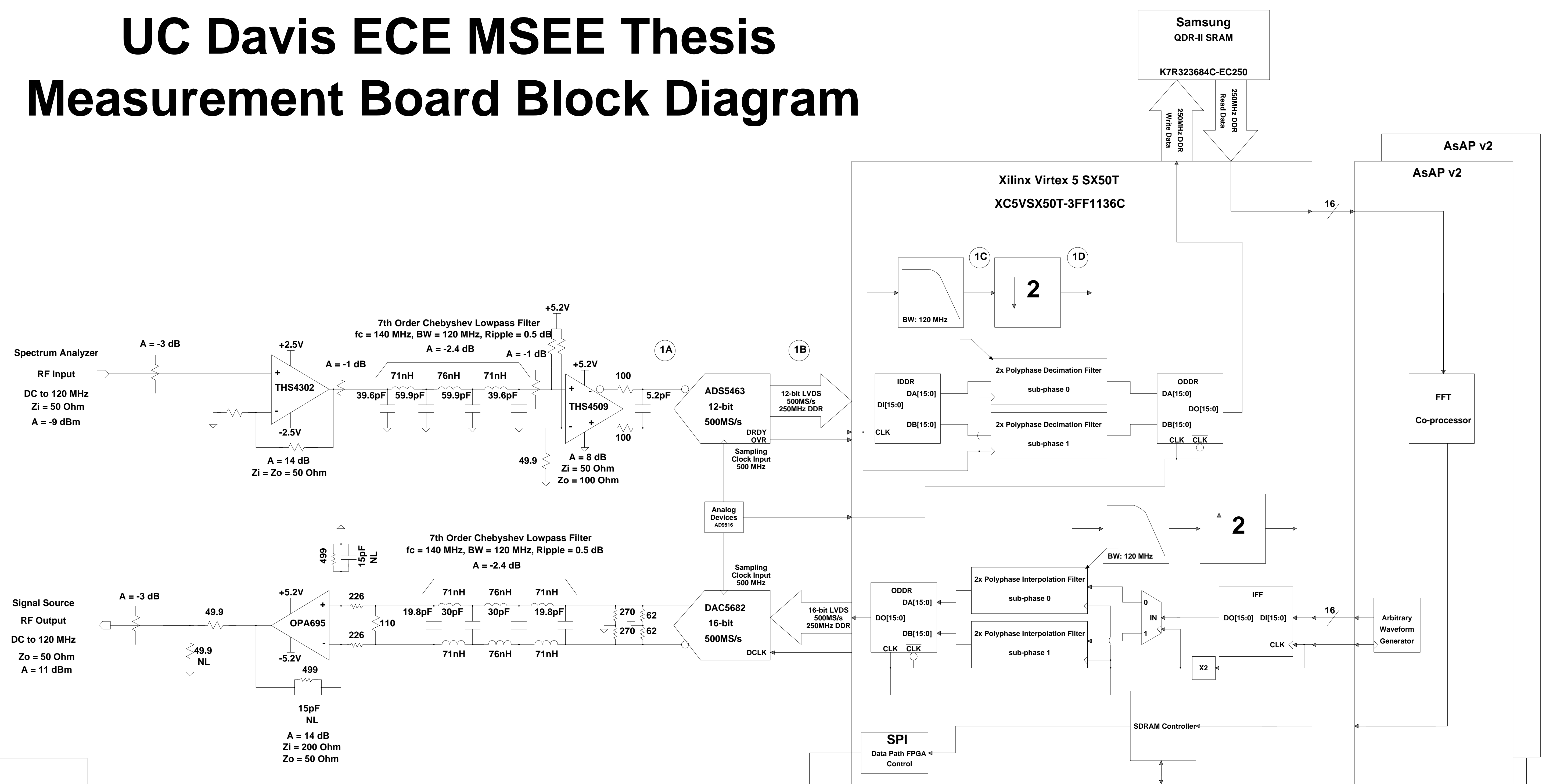
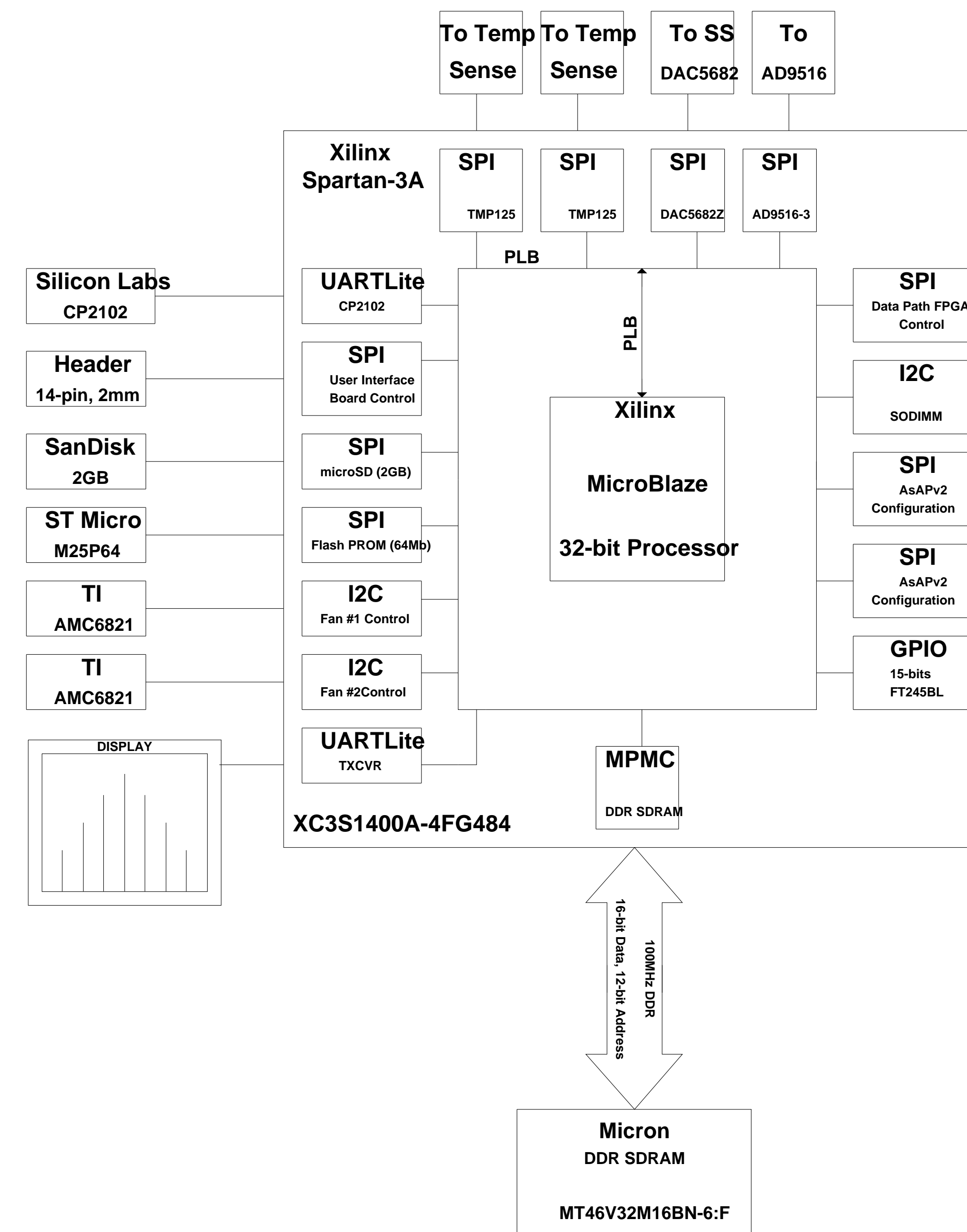
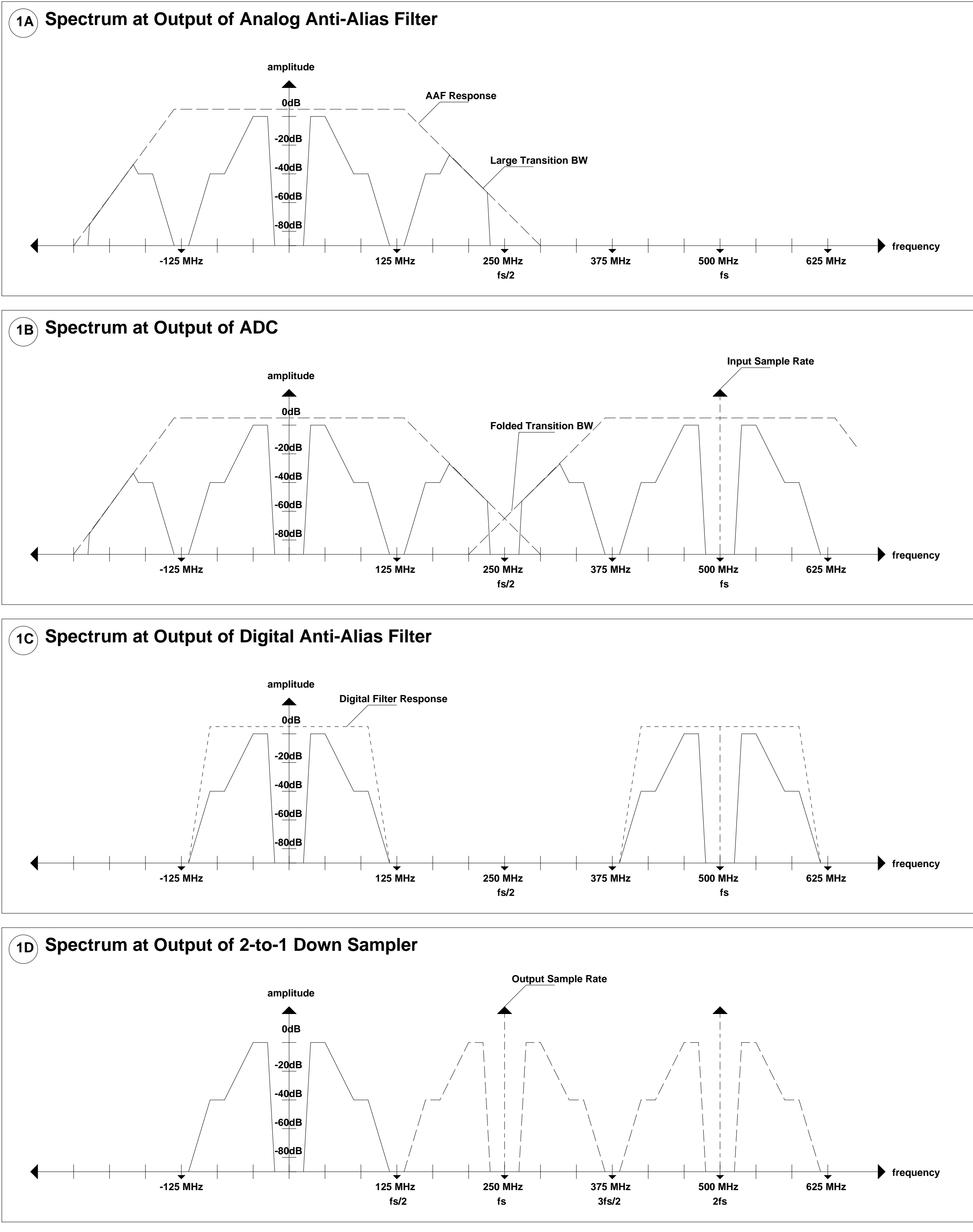


UC Davis ECE MSEE Thesis Measurement Board Block Diagram



Spectrum Analyzer Spectra Analysis



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43	ASAPV2 #2 POWER SUPPLY DECOUPLING

Notes and References

Data Sheets and User Guides:

Xilinx Virtex-5 SX50T:

1. Data Sheet: http://www.xilinx.com/support/documentation/data_sheets/ds100.pdf
2. DC and Switching: http://www.xilinx.com/support/documentation/data_sheets/ds202.pdf
3. User Guide: http://www.xilinx.com/support/documentation/user_guides/ug190.pdf
4. Packaging and Pinout: http://www.xilinx.com/support/documentation/user_guides/ug195.pdf
5. Configuration Guide: http://www.xilinx.com/support/documentation/user_guides/ug191.pdf
6. Rocket I/O GTP Guide: http://www.xilinx.com/support/documentation/user_guides/ug196.pdf
7. PCB Designer's Guide: http://www.xilinx.com/support/documentation/user_guides/ug203.pdf
8. System Monitor Guide: http://www.xilinx.com/support/documentation/user_guides/ug192.pdf

Xilinx Spartan-3A XC3S1400A:

1. Data Sheet: http://www.xilinx.com/support/documentation/data_sheets/ds529.pdf
2. User Guide: http://www.xilinx.com/support/documentation/user_guides/ug331.pdf
3. Configuration Guide: http://www.xilinx.com/support/documentation/user_guides/ug332.pdf

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1. K7R323684C-EC250 Data Sheet: http://www.samsung.com/global/system/business/semiconductor/product/2007/7/30/948789ds_k7r32xx84c_rev11.pdf

TI ADS5463 12-bit, 500MS/s:

1. ADS5463 Data Sheet: <http://focus.ti.com/lit/ds/symlink/ads5463.pdf>

TI DAC5682Z 16-bit, 1GS/s:

1. DAC5682Z Data Sheet: <http://focus.ti.com/lit/ds/symlink/dac5682z.pdf>

TI High-Speed Op-Amps: THS4302, THS4509, OPA695

1. THS4302 Data Sheet: <http://focus.ti.com/lit/ds/symlink/th4302.pdf>
2. THS4509 Data Sheet: <http://focus.ti.com/lit/ds/symlink/th4509.pdf>
3. OPA695 Data Sheet: <http://focus.ti.com/lit/ds/symlink/opa695.pdf>

TI Power Supply Regulators:

1. PTH08T220WAZ Data Sheet: <http://focus.ti.com/lit/ds/symlink/pth08t220w.pdf>
2. PTH08T260WAZ Data Sheet: <http://focus.ti.com/lit/ds/symlink/pth08t260w.pdf>
3. PTH12050YAZ Data Sheet: <http://focus.ti.com/lit/ds/symlink/pth12050y.pdf>
4. TPS79601 Data Sheet: <http://focus.ti.com/lit/ds/symlink/tps79601.pdf>
5. TPS74201 Data Sheet: <http://focus.ti.com/lit/ds/symlink/tps74201.pdf>
6. TPS73701 Data Sheet: <http://focus.ti.com/lit/ds/symlink/tps73701.pdf>
7. LP2951D Data Sheet: <http://focus.ti.com/lit/ds/symlink/lp2951.pdf>
8. TPS72301 Data Sheet: <http://focus.ti.com/lit/ds/symlink/tps72301.pdf>
9. TL7733BCD Data Sheet: <http://focus.ti.com/lit/ds/symlink/tl7733b.pdf>
10. TPS3808G25 Data Sheet: <http://focus.ti.com/lit/ds/symlink/tps3808g25.pdf>

TI Fan Controllers

1. AMC6821 Data Sheet: <http://focus.ti.com/lit/ds/symlink/amc6821.pdf>

Micron DDR2 SDRAM SODIMM:

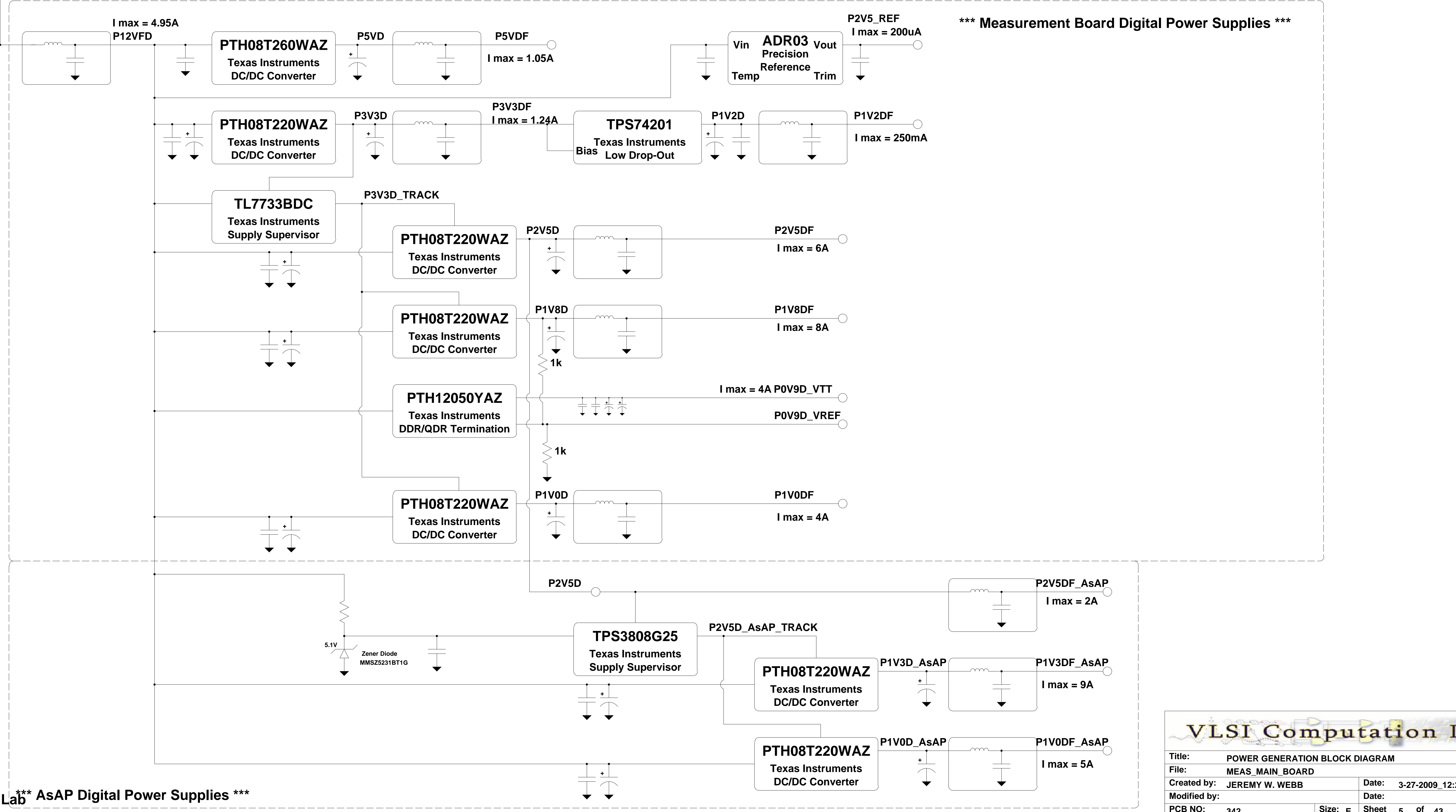
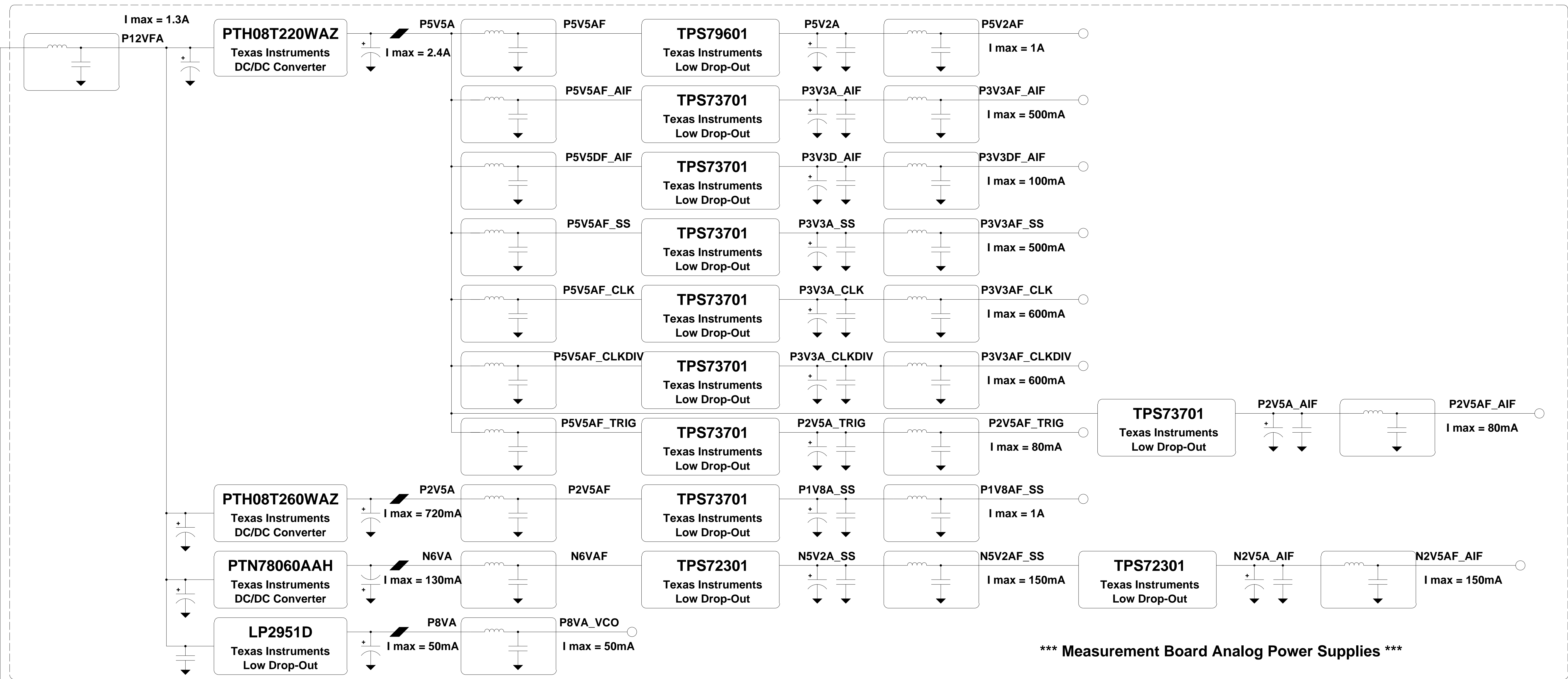
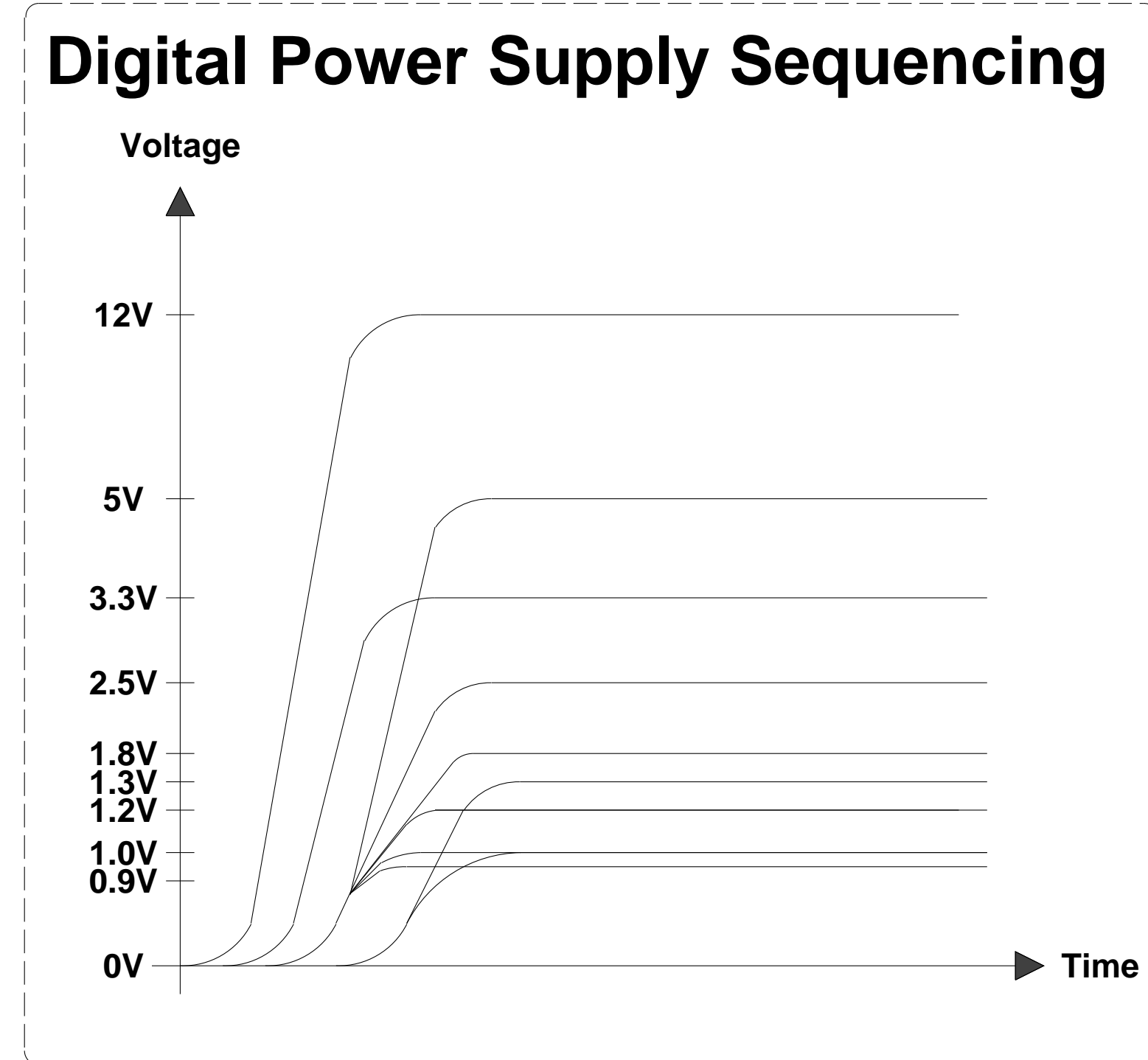
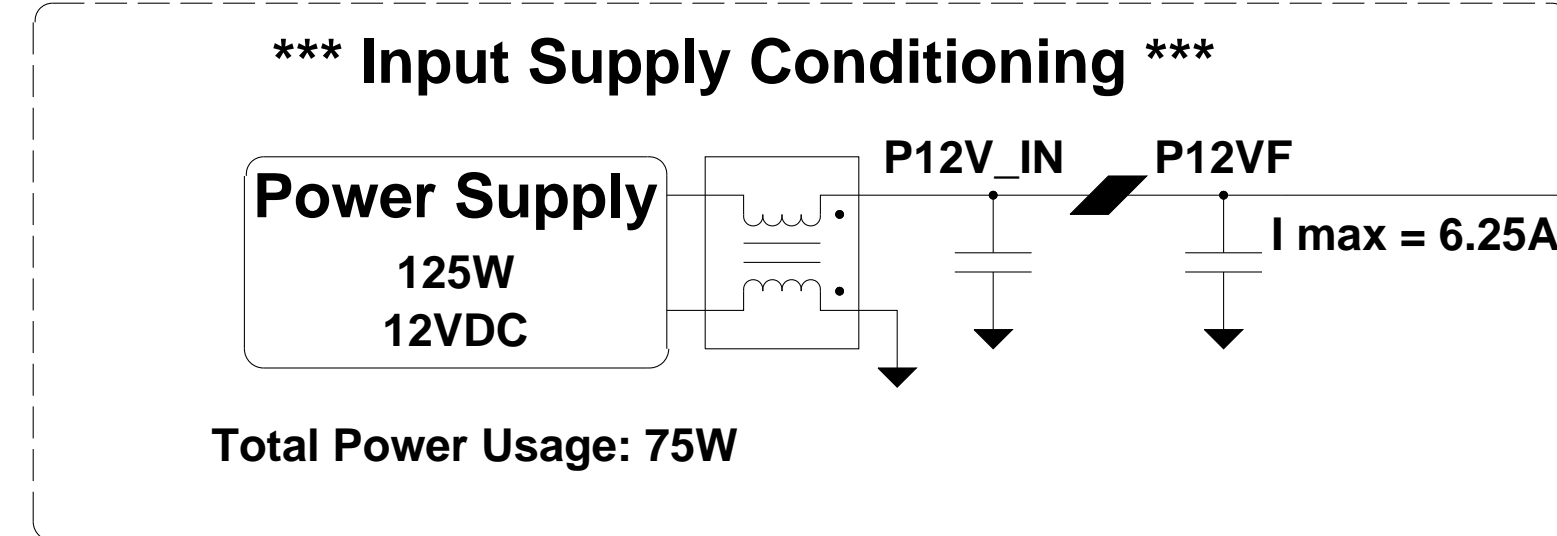
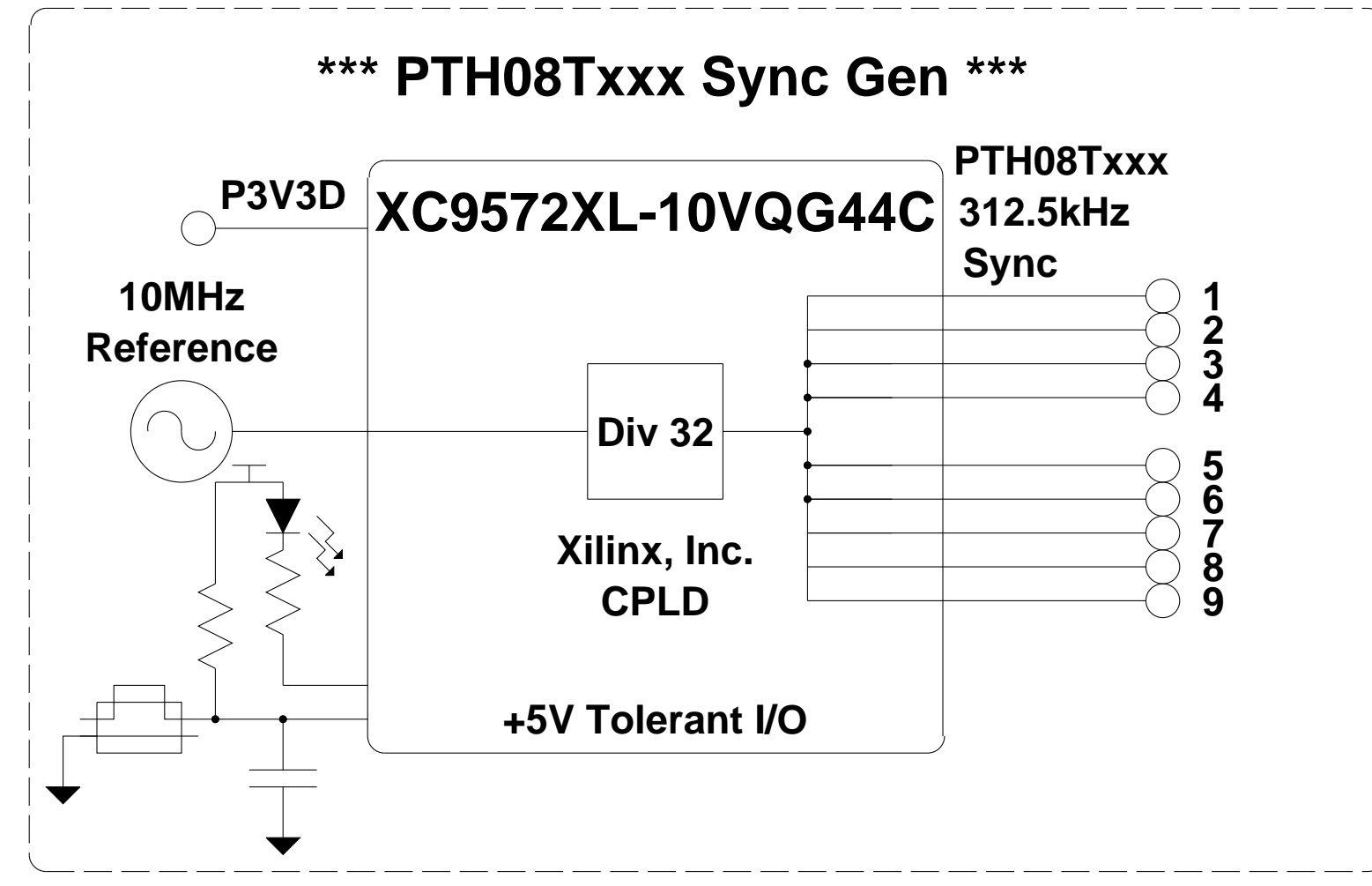
1. MT16HTF25664HY-667E1 Data Sheet: http://download.micron.com/pdf/datasheets/modules/ddr2/HTF16C128_256x64H.pdf

Analog Devices Clock PLL IC:

1. AD9516-3 Data Sheet: http://www.analog.com/UploadedFiles/Data_Sheets/AD9516_3.pdf

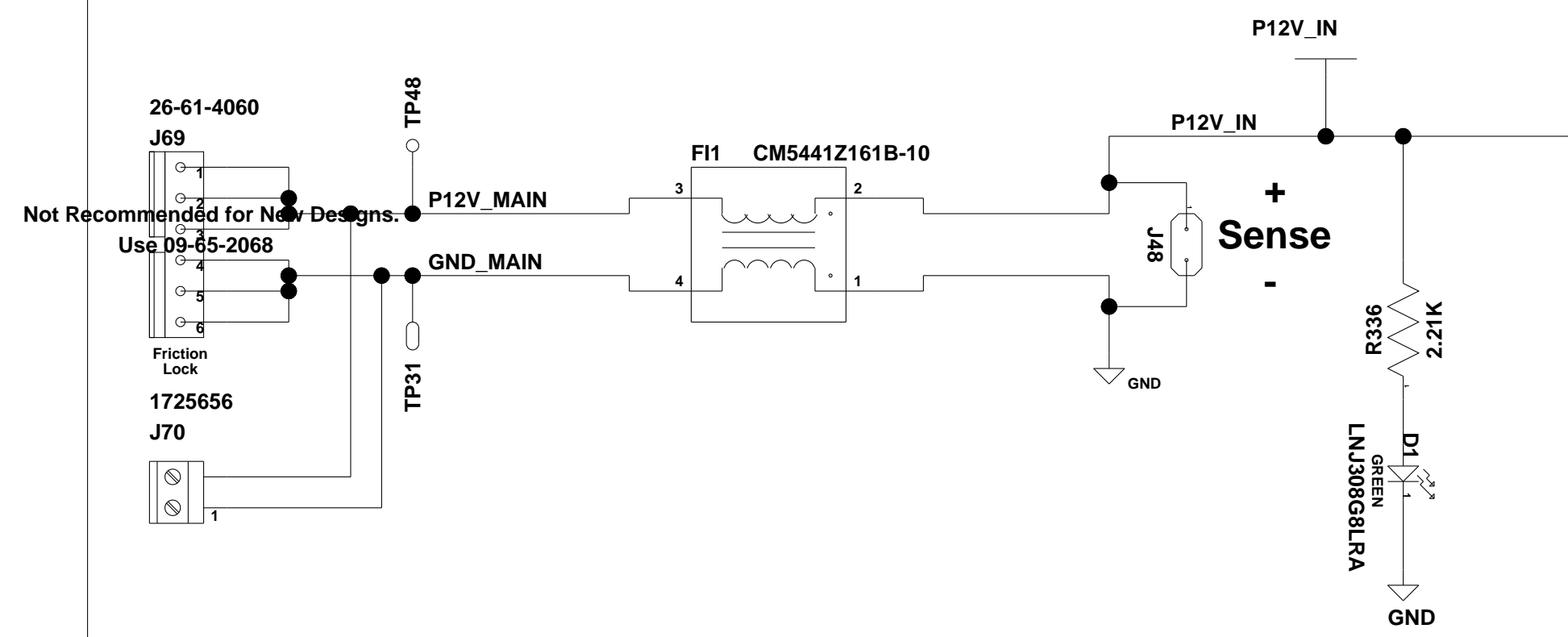
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Modified by:		Date:	
PCB NO:	342	Size:	E
Sheet:	4	of:	43
REV:	001		

Power Generation Block Diagram

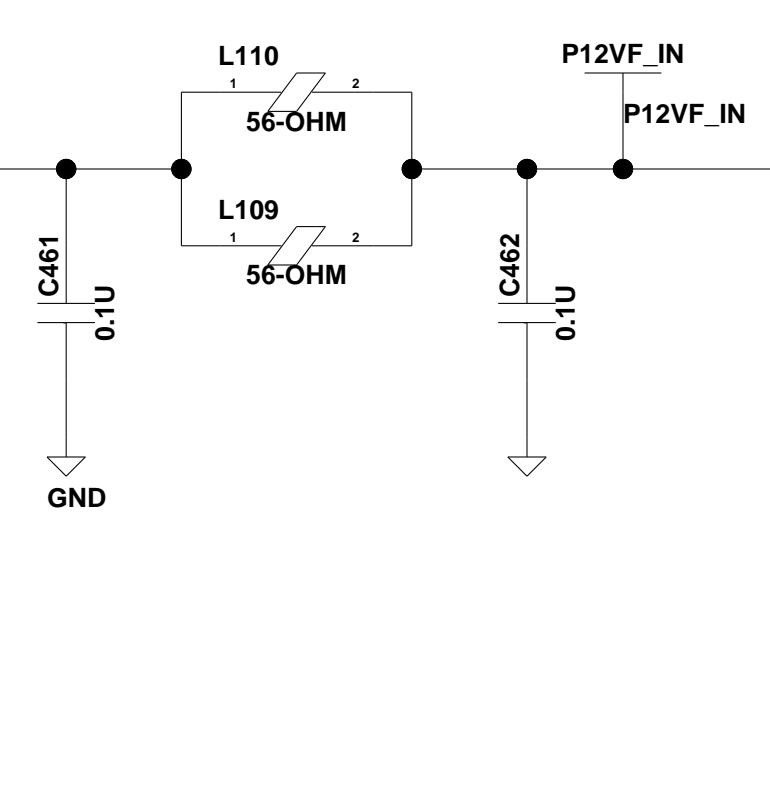


MAIN POWER INPUT AND FAN CONTROL

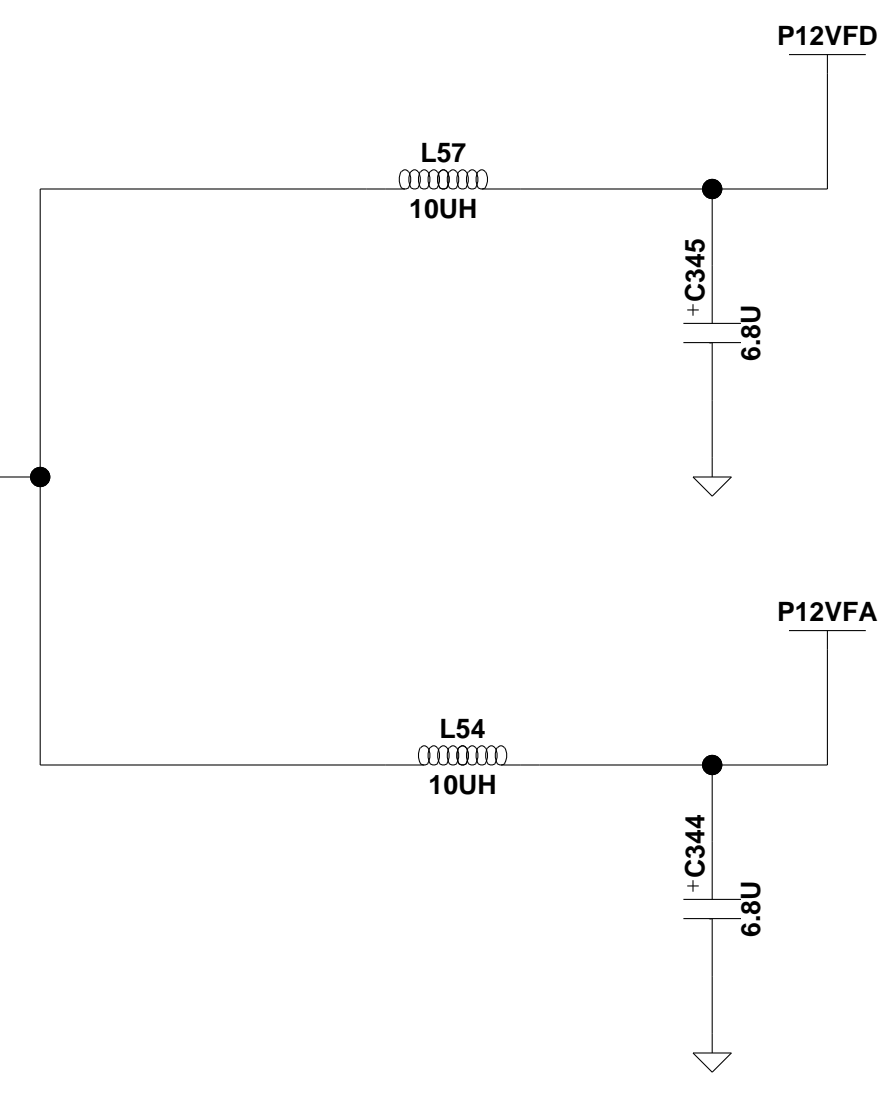
A +12V SUPPLY INPUT



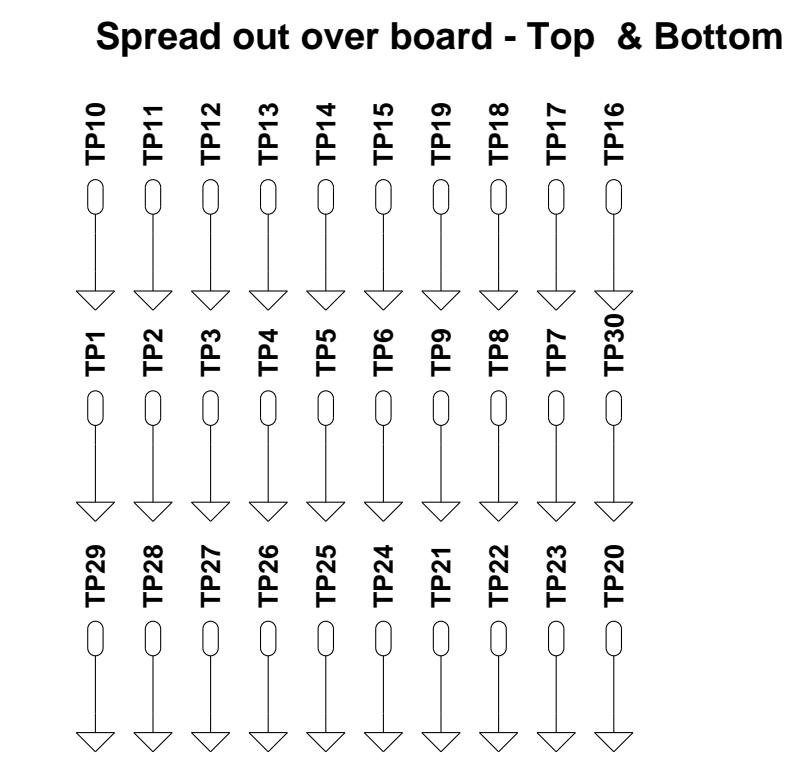
B +12V Filtering



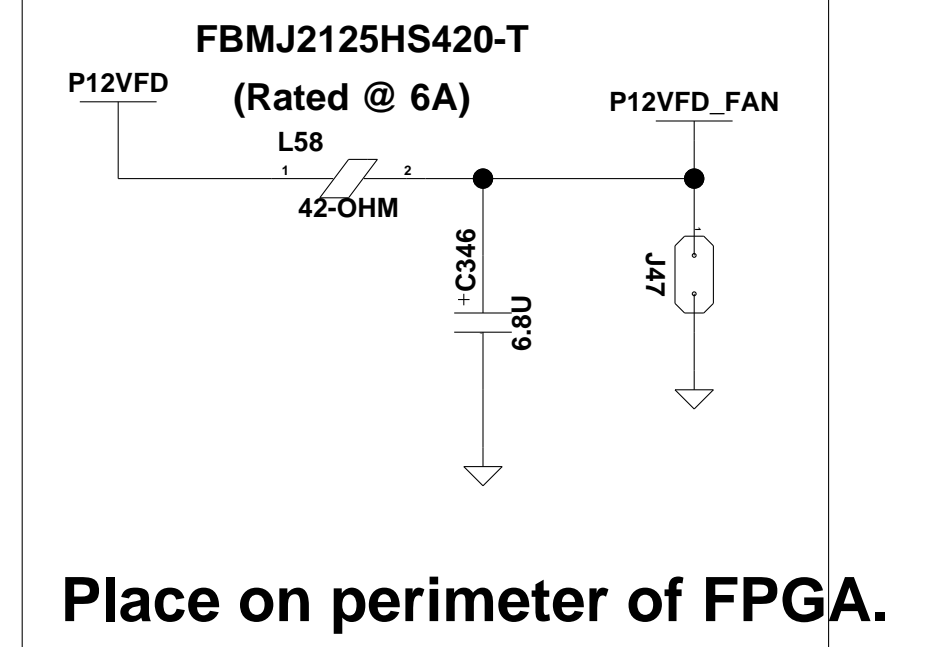
C +12V Analog and Digital Filtering



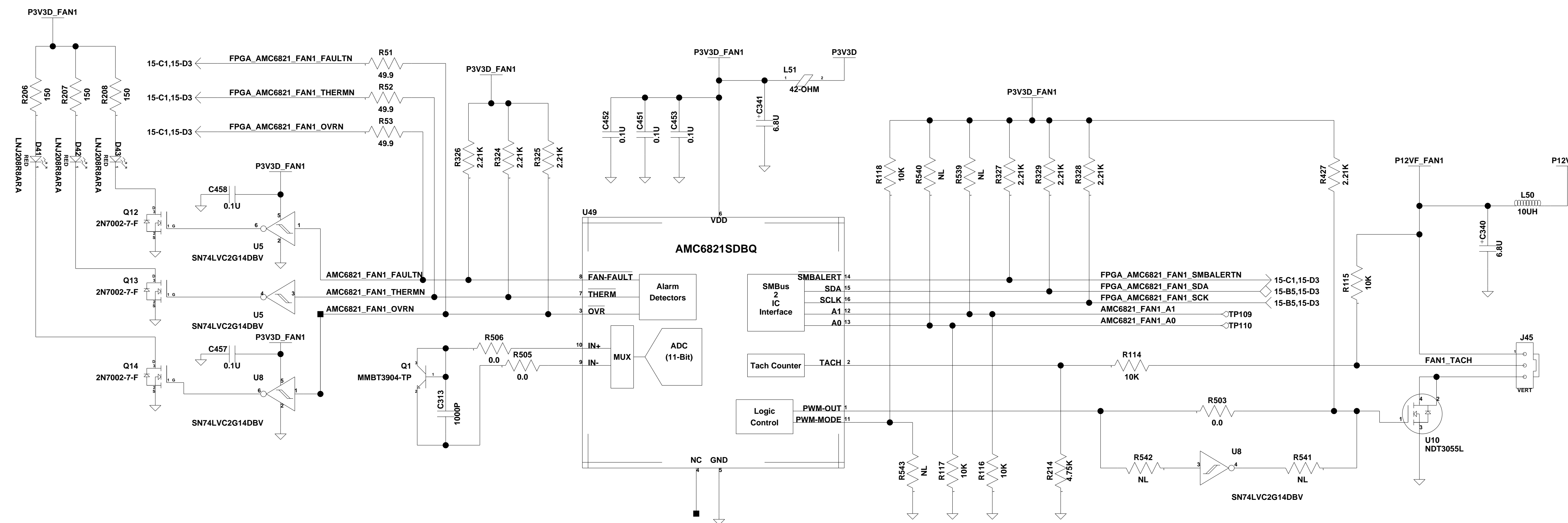
D GROUND Tst Pts



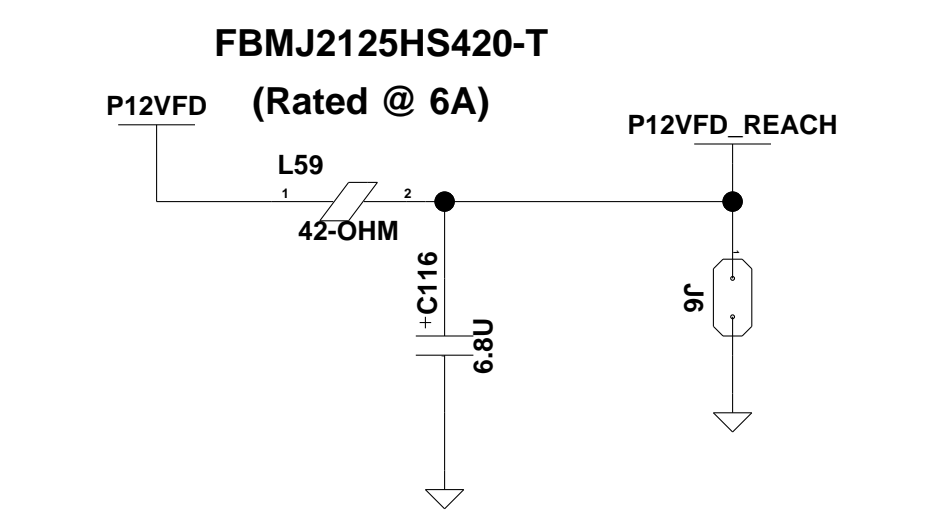
E FPGA Fan



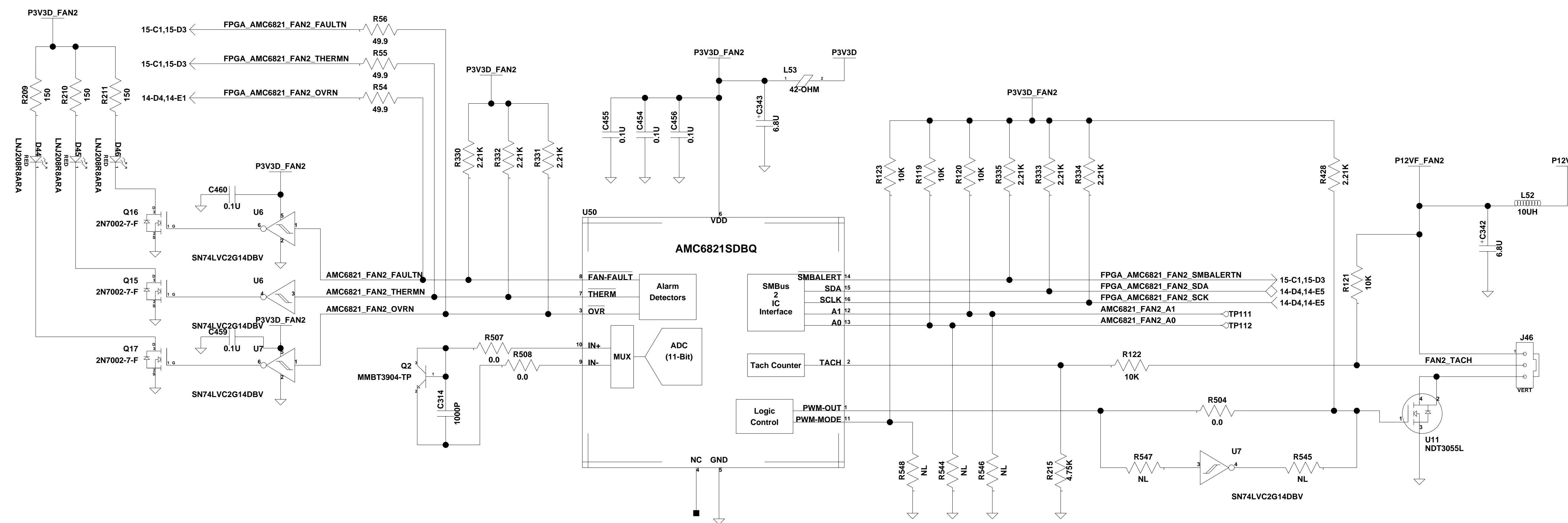
F Instrument Fan #1 Control



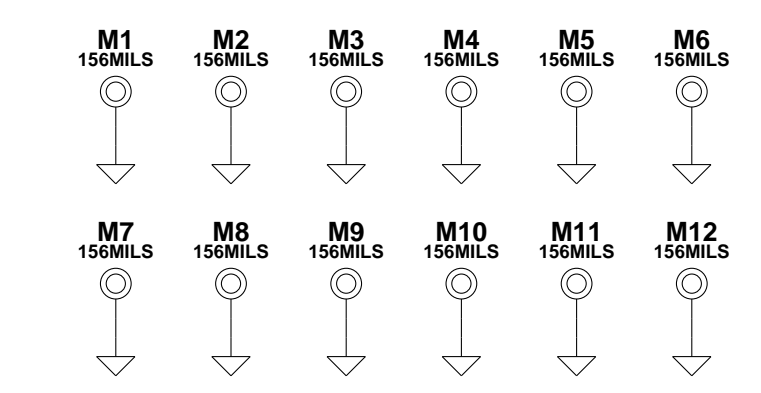
G Reach Display PWR



H Instrument Fan #2 Control

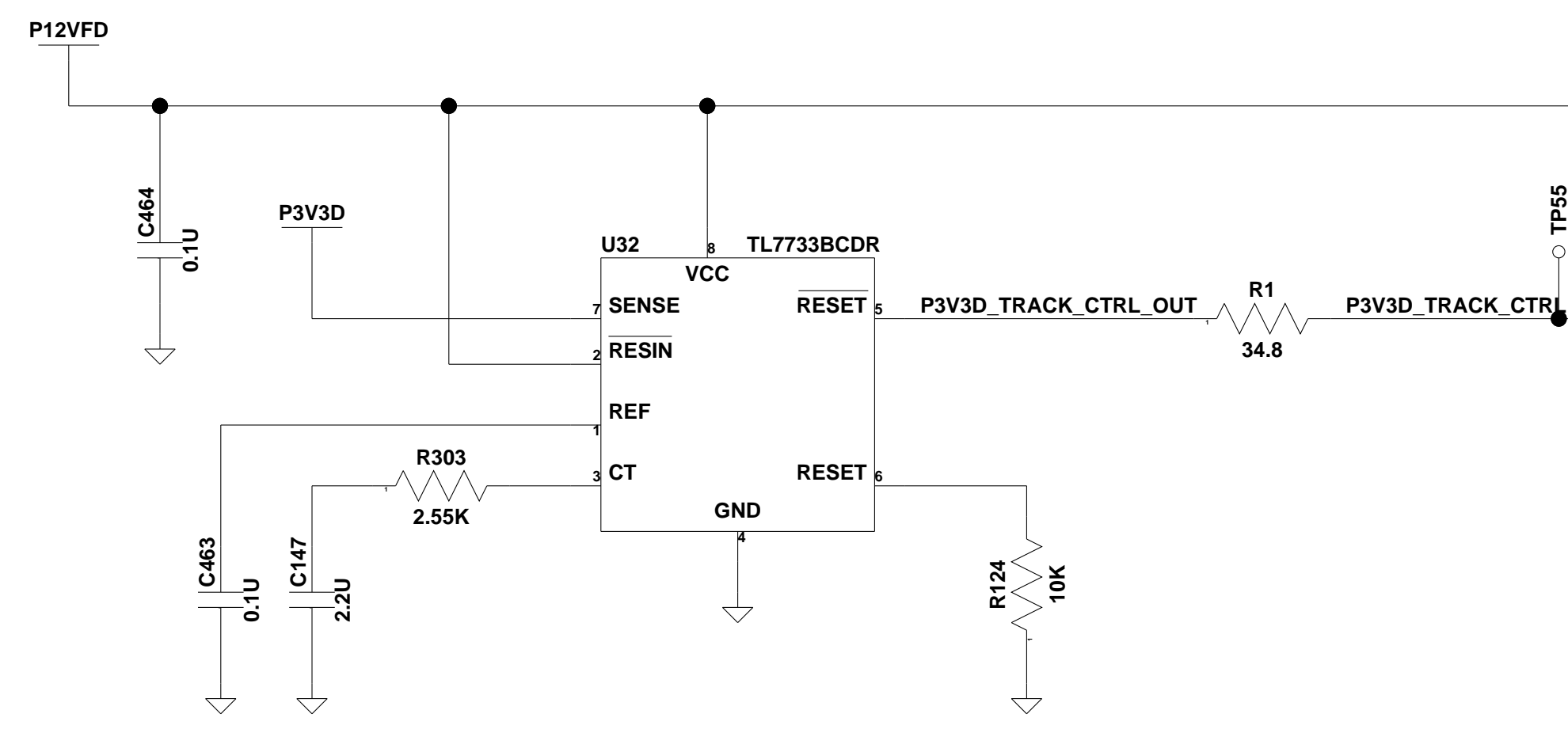


I MOUNTING HOLES

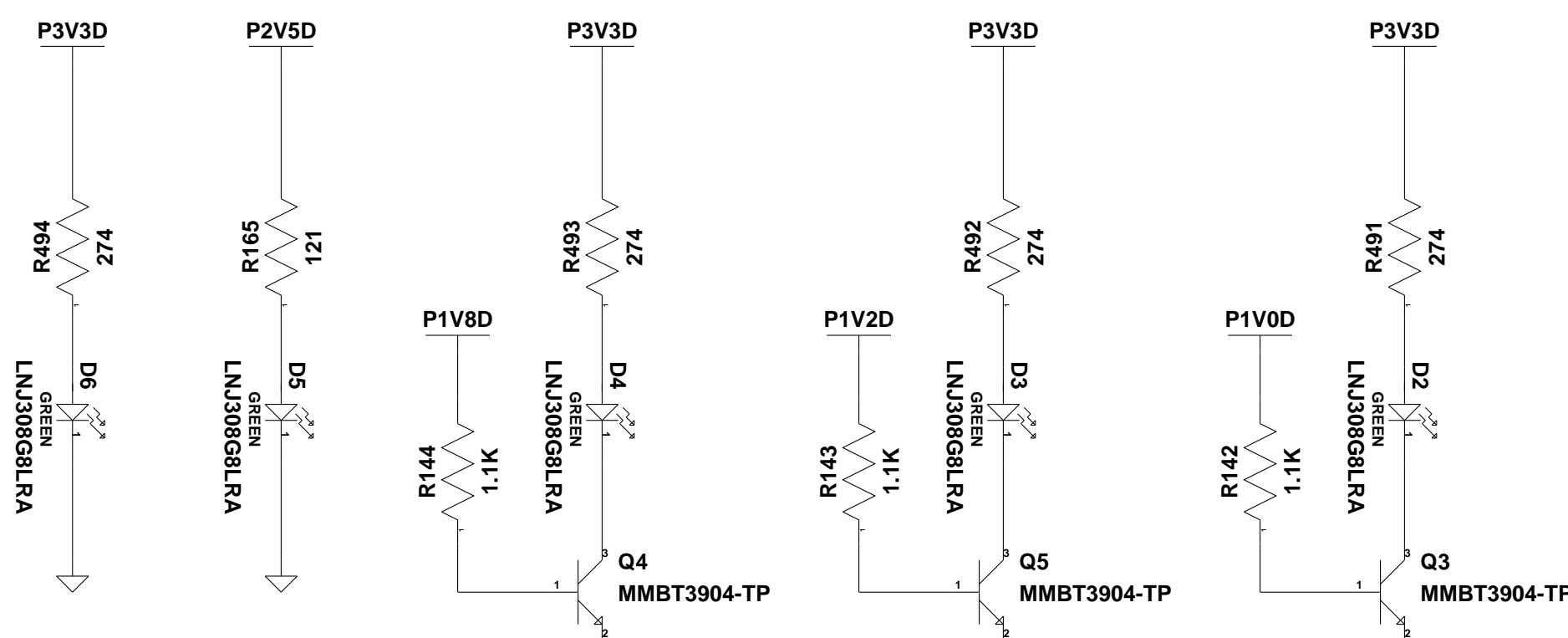


Xilinx Virtex-5 SX50T Digital Supply Regulation and Sequencing

A Digital Supply Sequencers

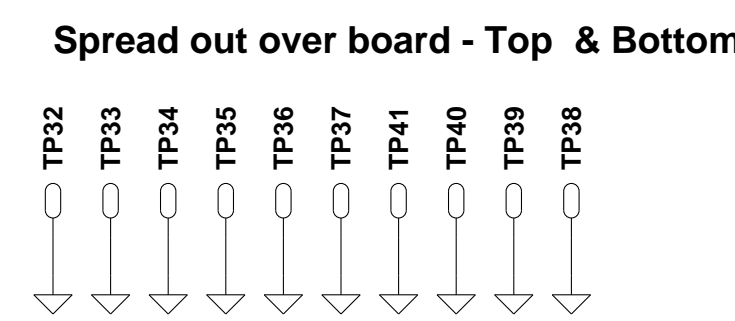


B POWER LEDs

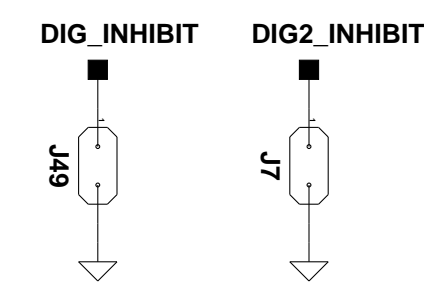


PLACE LEDs NEAR EDGE OF BOARD
Green LED (LNJ308GLRA):
ILED = (VCC - VF)/IF
VF = 1.9V IF = 5mA

C GROUND Tst Pts

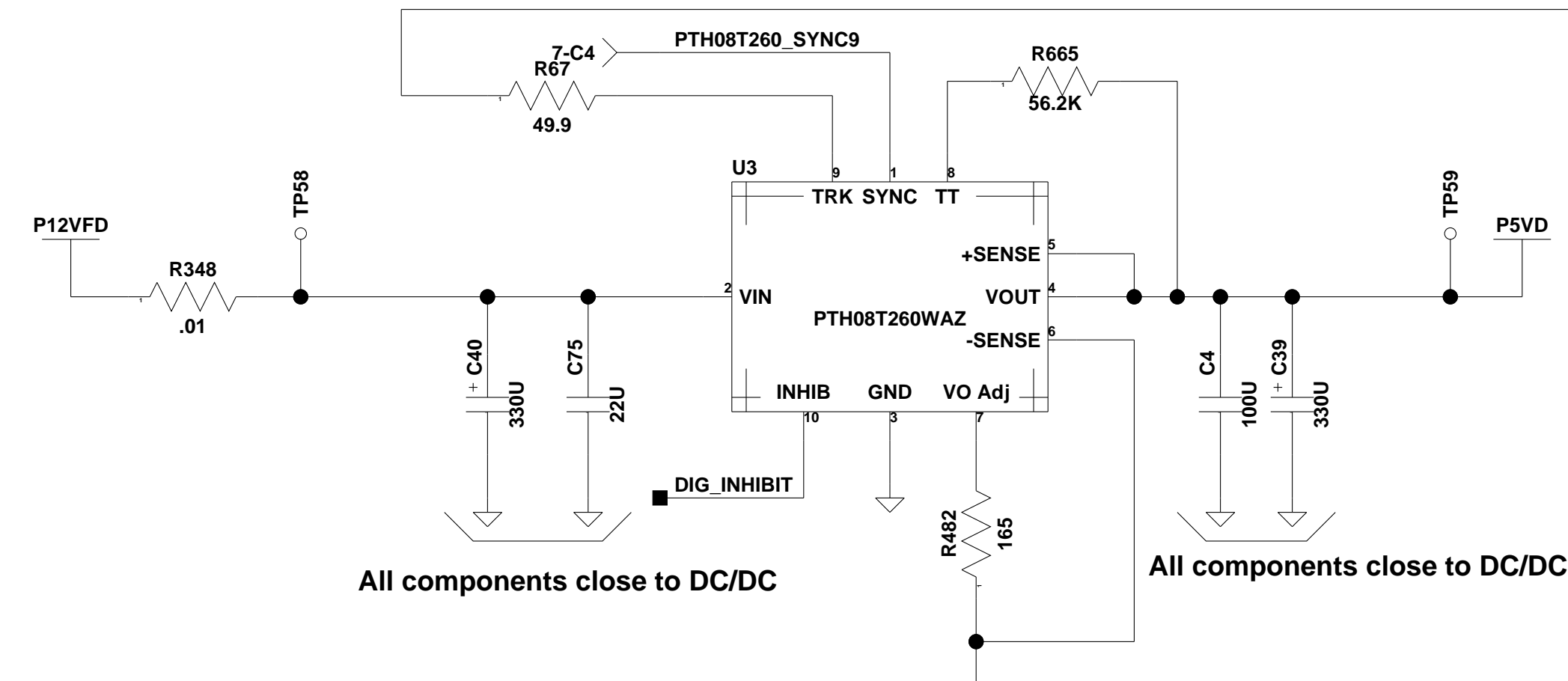


D PTH08T220WAZ DISABLE



Load Jumper to Disable DC/DC Converters

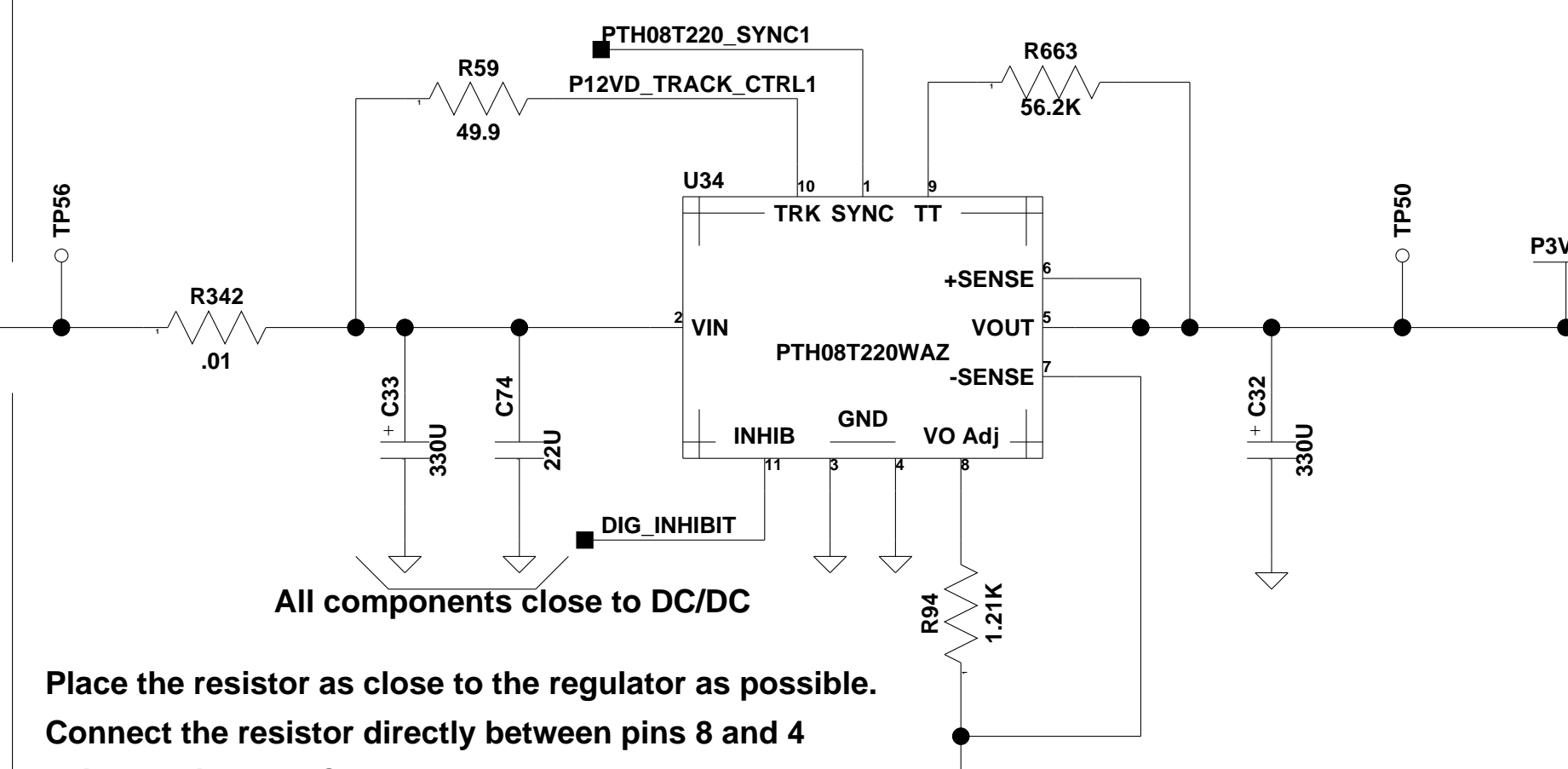
E +5V Digital Supply Regulation



5.0V Rset = 165 Ohm, PTH08T260W, Vout = 5.01 V

Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 7 and 3 using dedicated PCB traces.

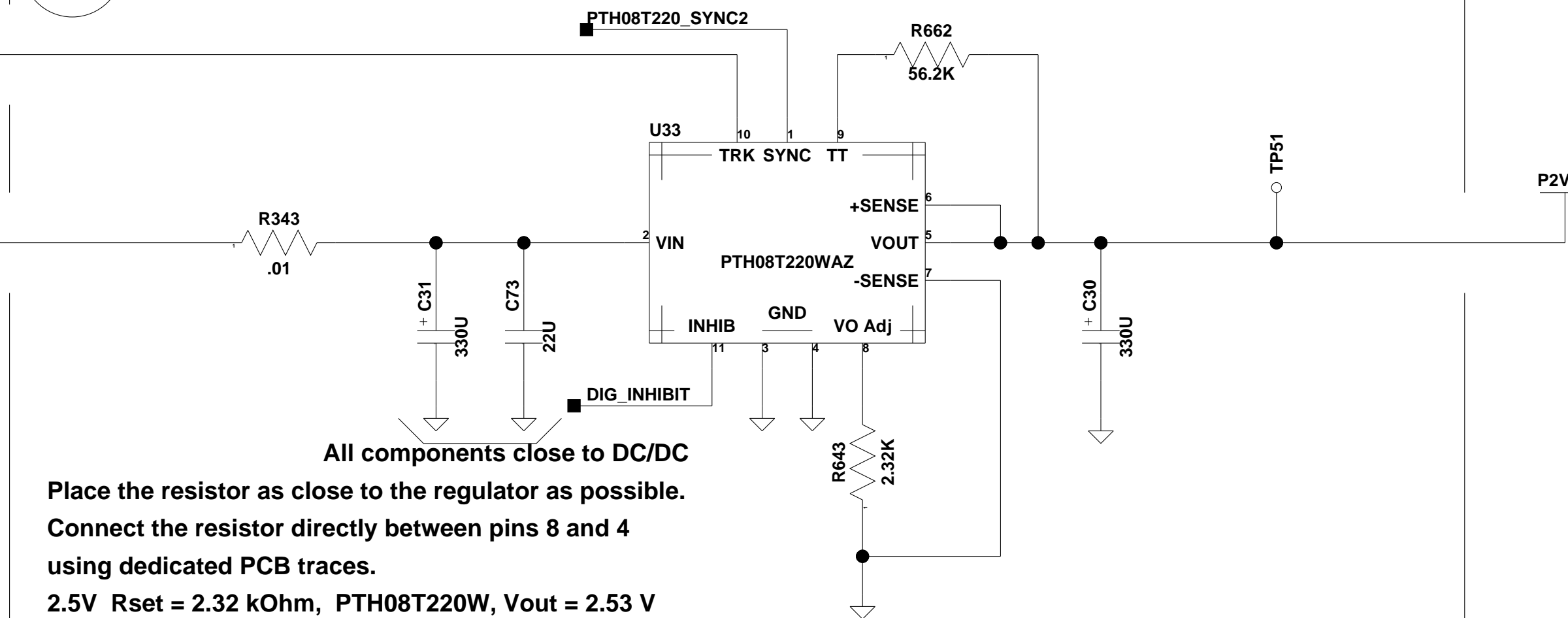
F +3.3V Digital Power Supply



All components close to DC/DC
Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 8 and 4 using dedicated PCB traces.

3.3V Rset = 1.21 kOhm, PTH08T220W, Vout = 3.303636 V

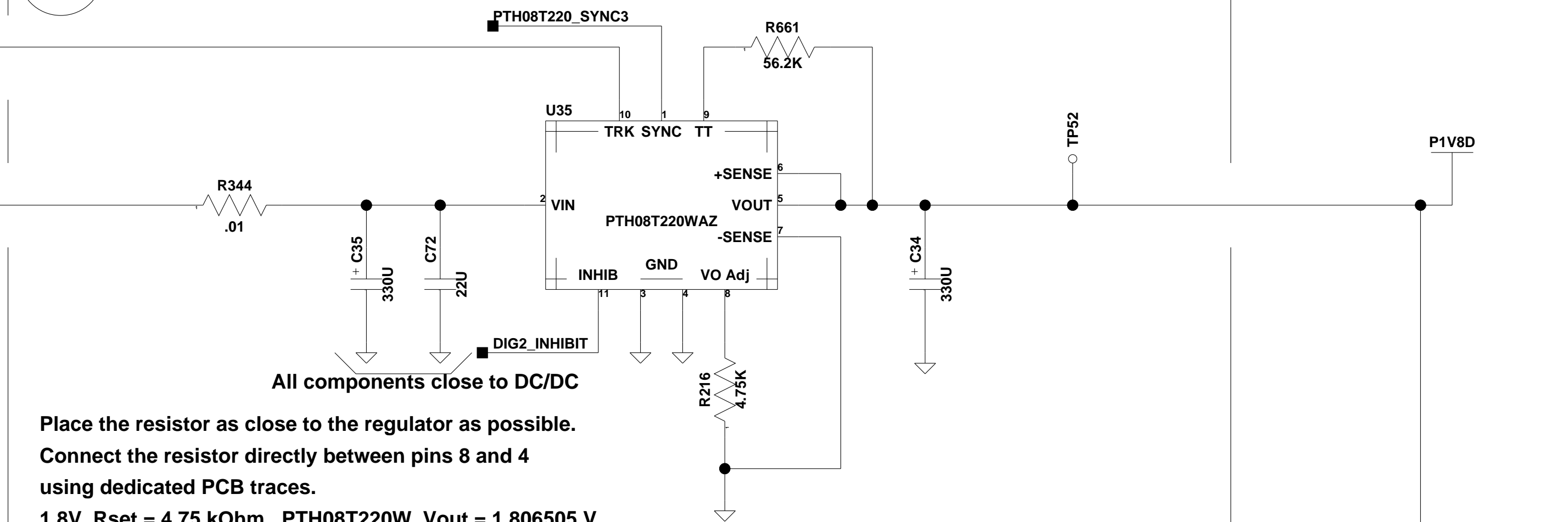
H +2.5V Digital Power Supply



All components close to DC/DC
Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 8 and 4 using dedicated PCB traces.

2.5V Rset = 2.32 kOhm, PTH08T220W, Vout = 2.53 V

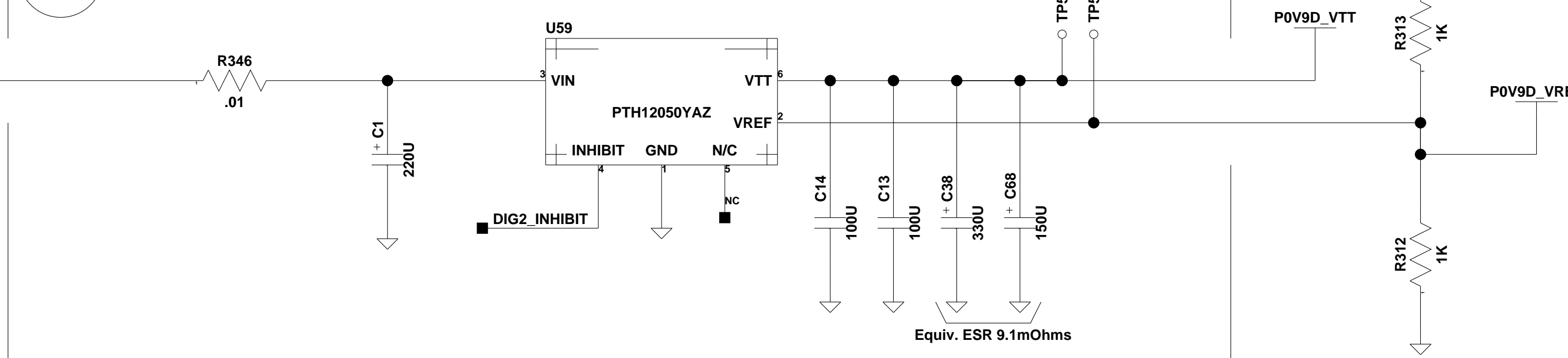
I +1.8V Digital Power Supply



All components close to DC/DC
Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 8 and 4 using dedicated PCB traces.

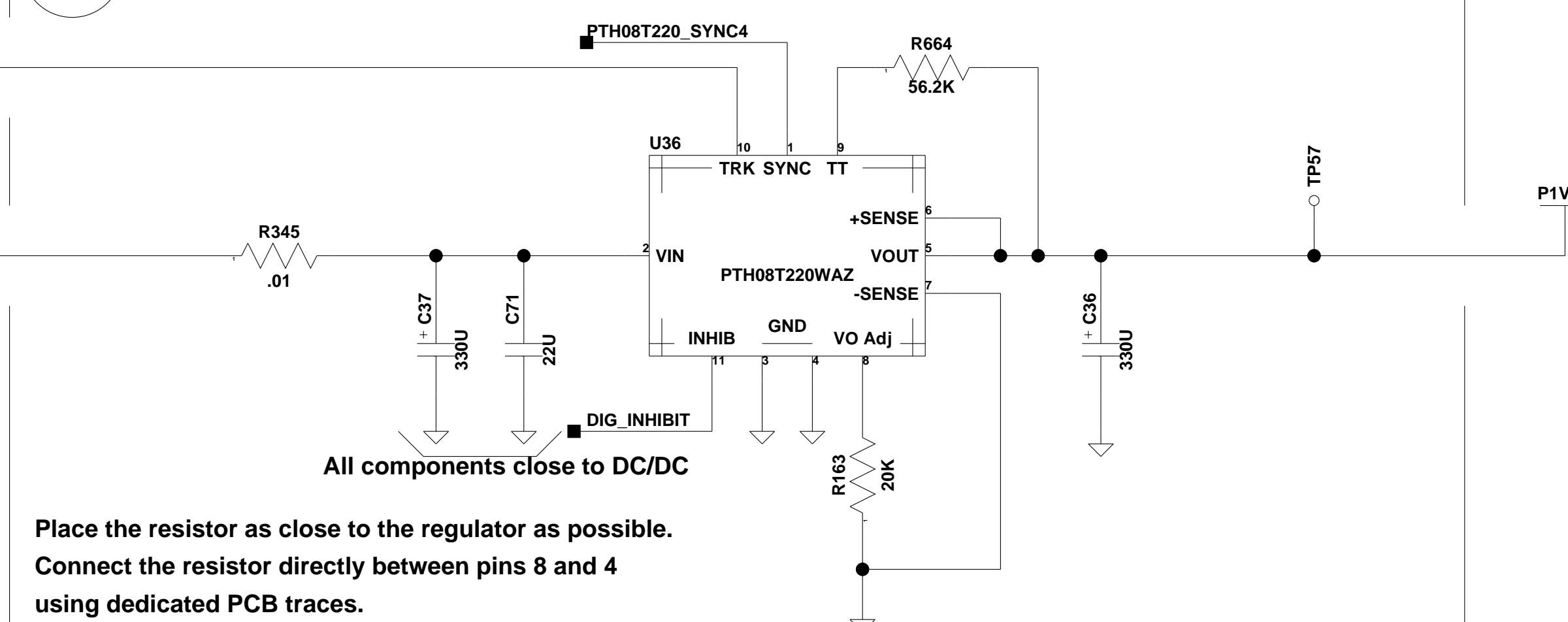
1.8V Rset = 4.75 kOhm, PTH08T220W, Vout = 1.806505 V

J DDR/QDR VTT/VREF Generation



Equiv. ESR 9.1mOhms

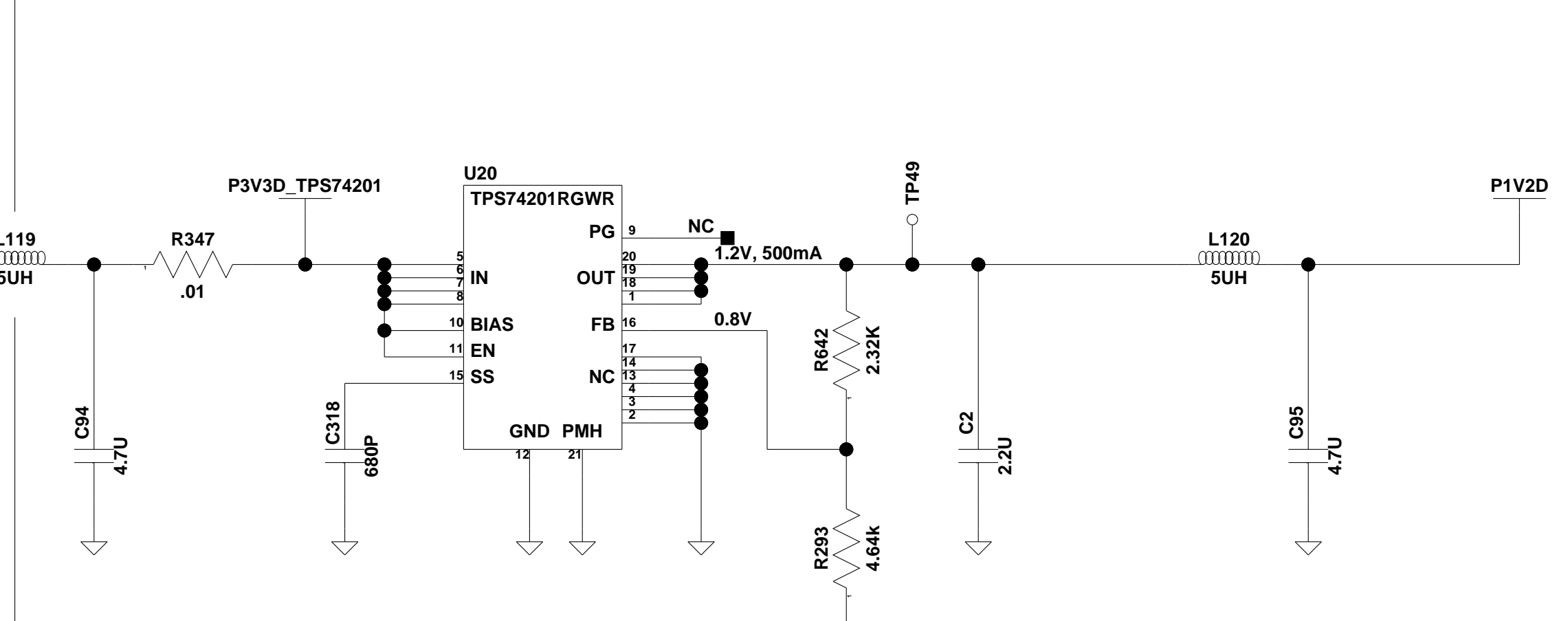
K +1.0V Digital Power Supply



All components close to DC/DC
Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 8 and 4 using dedicated PCB traces.

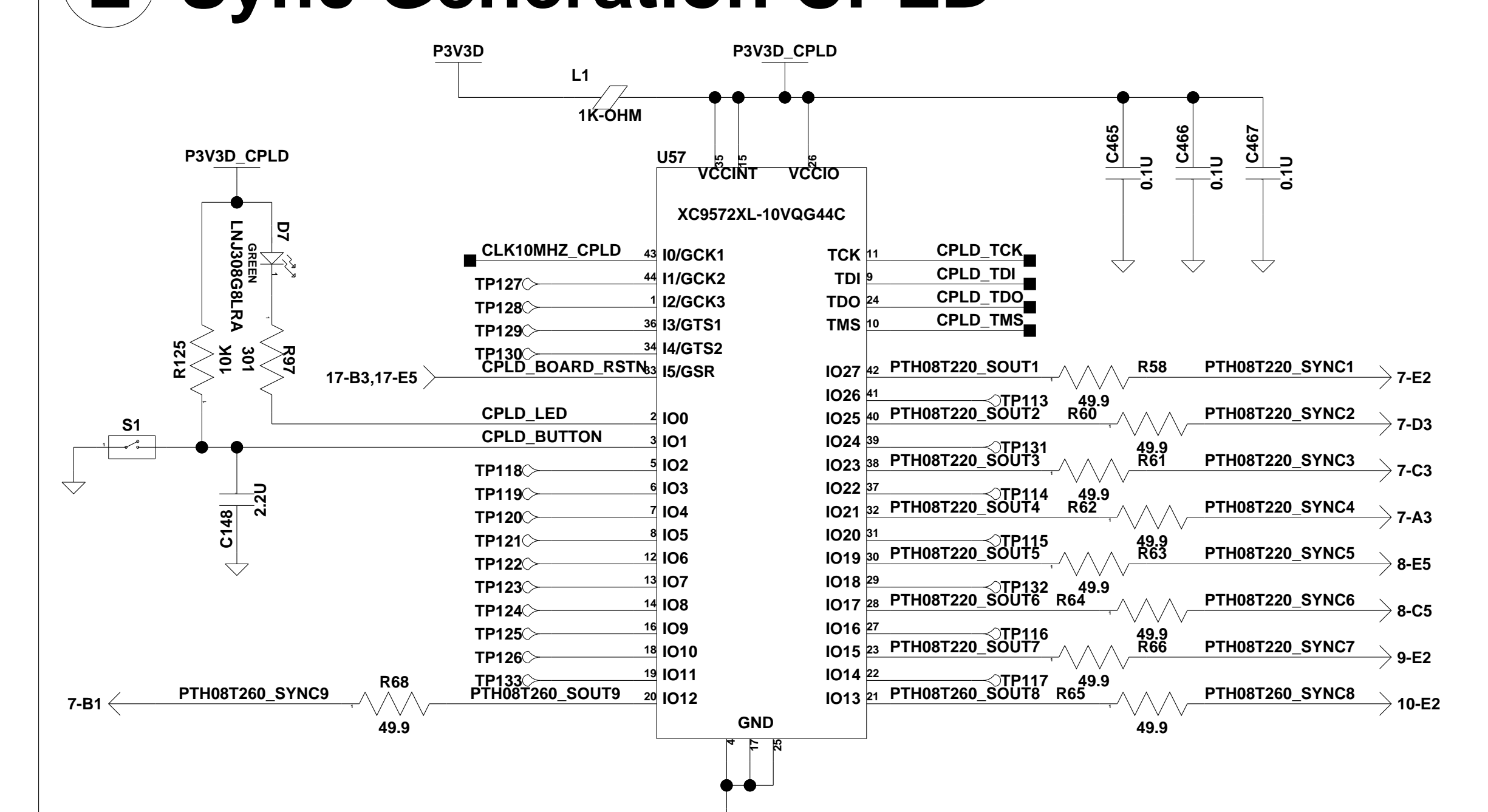
1.0V Rset = 20.0kOhm, PTH08T220W, Vout = 1.011979 V

G +1.2V Digital Power Supply

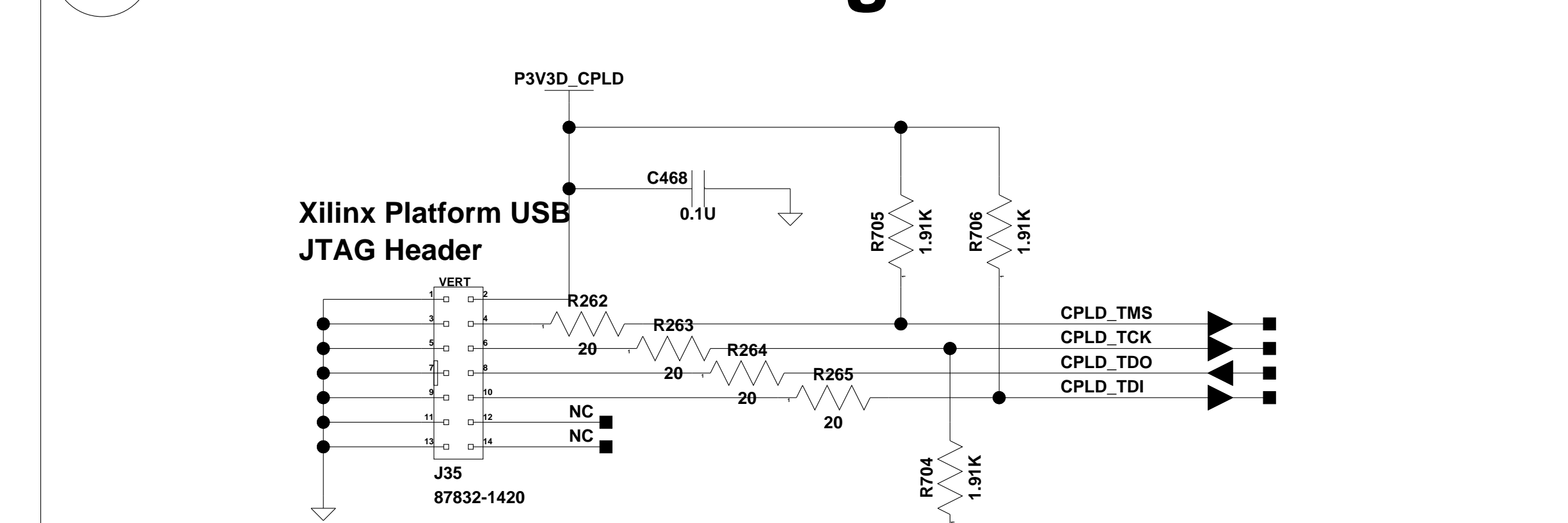


Digital Power Supply Sequence Order:
1. +12V Input
2. +3.3V
3. +2.5V, +1.8V, +1.2V, +1V, DDR VTT/VREF

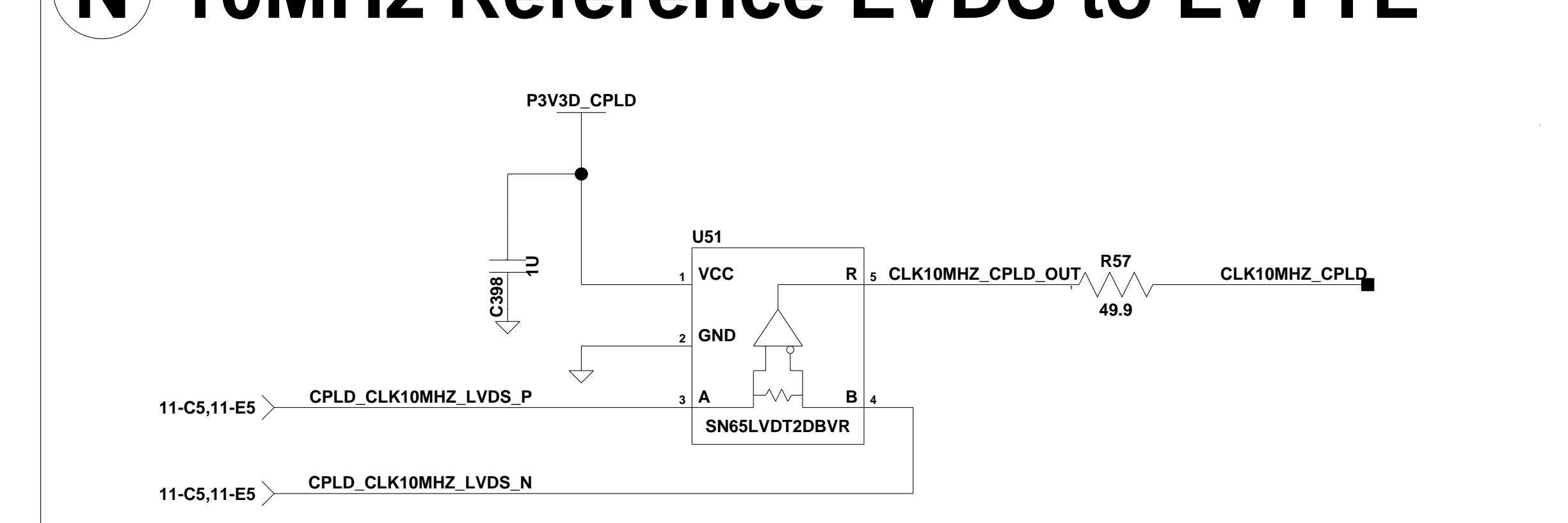
L Sync Generation CPLD



M CPLD JTAG Configuration

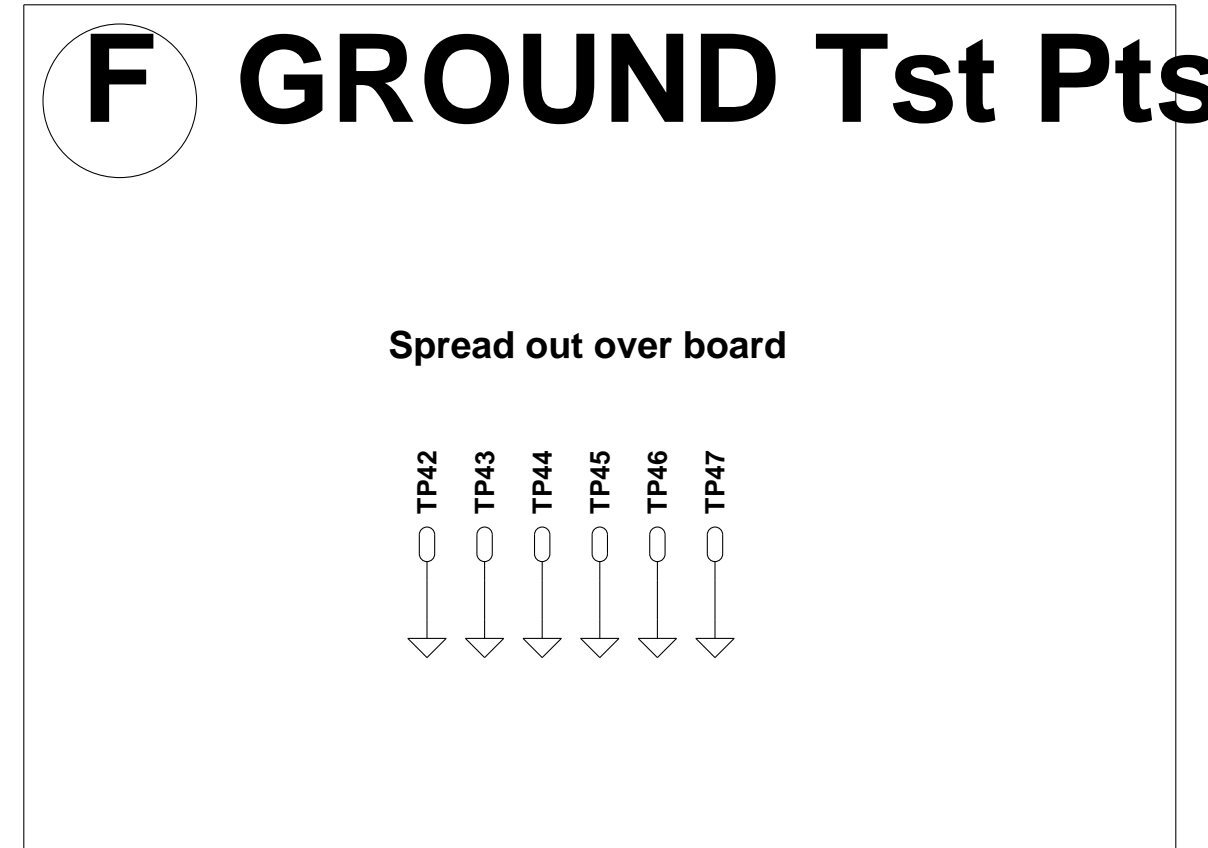
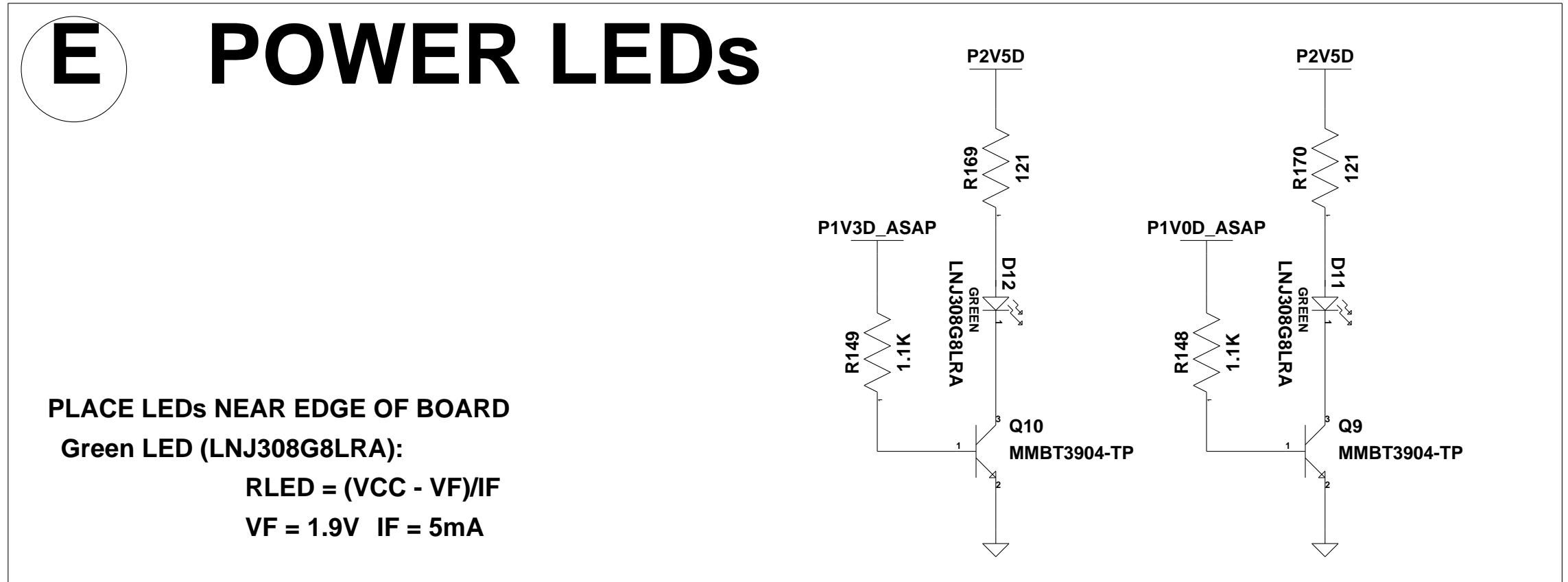
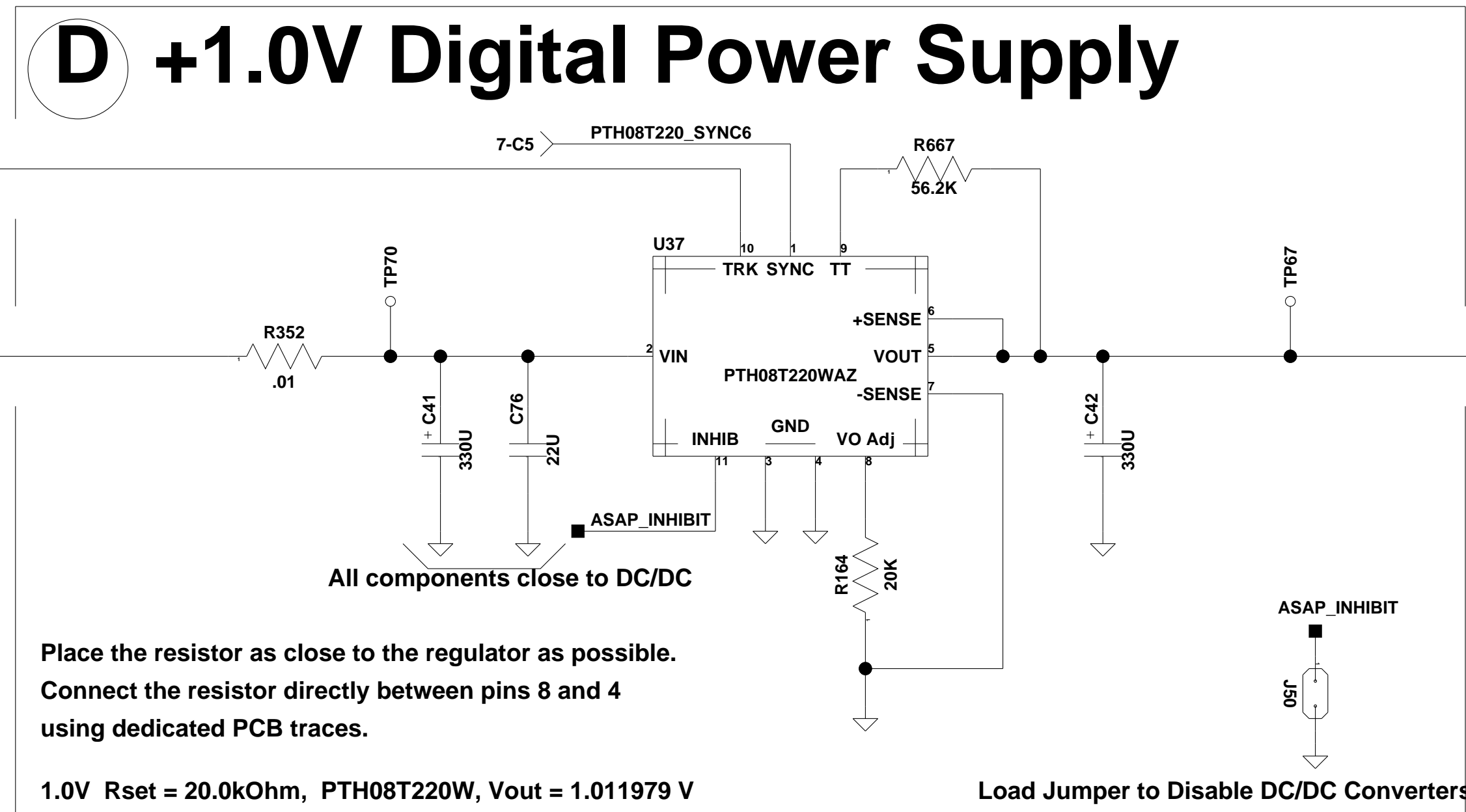
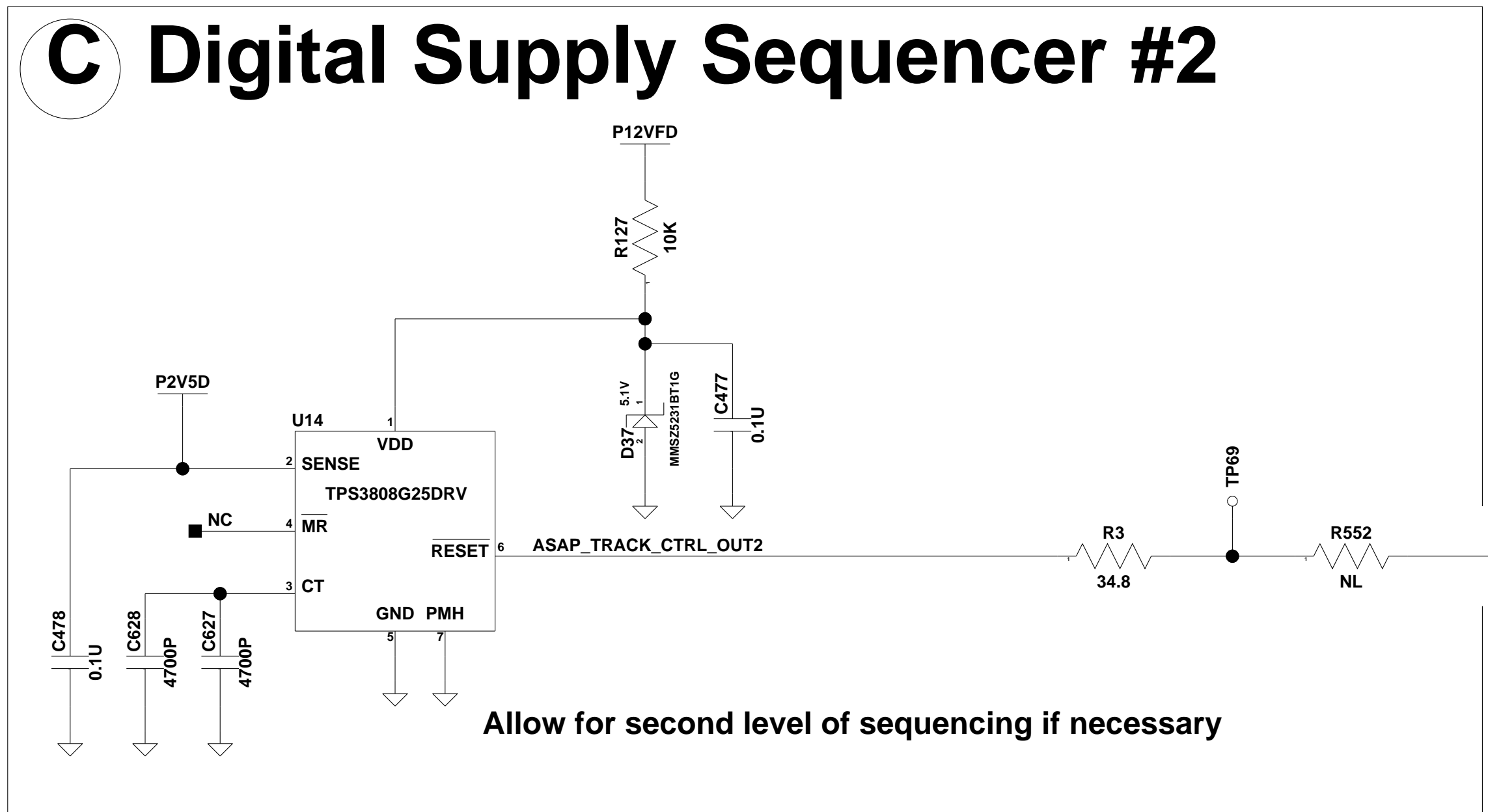
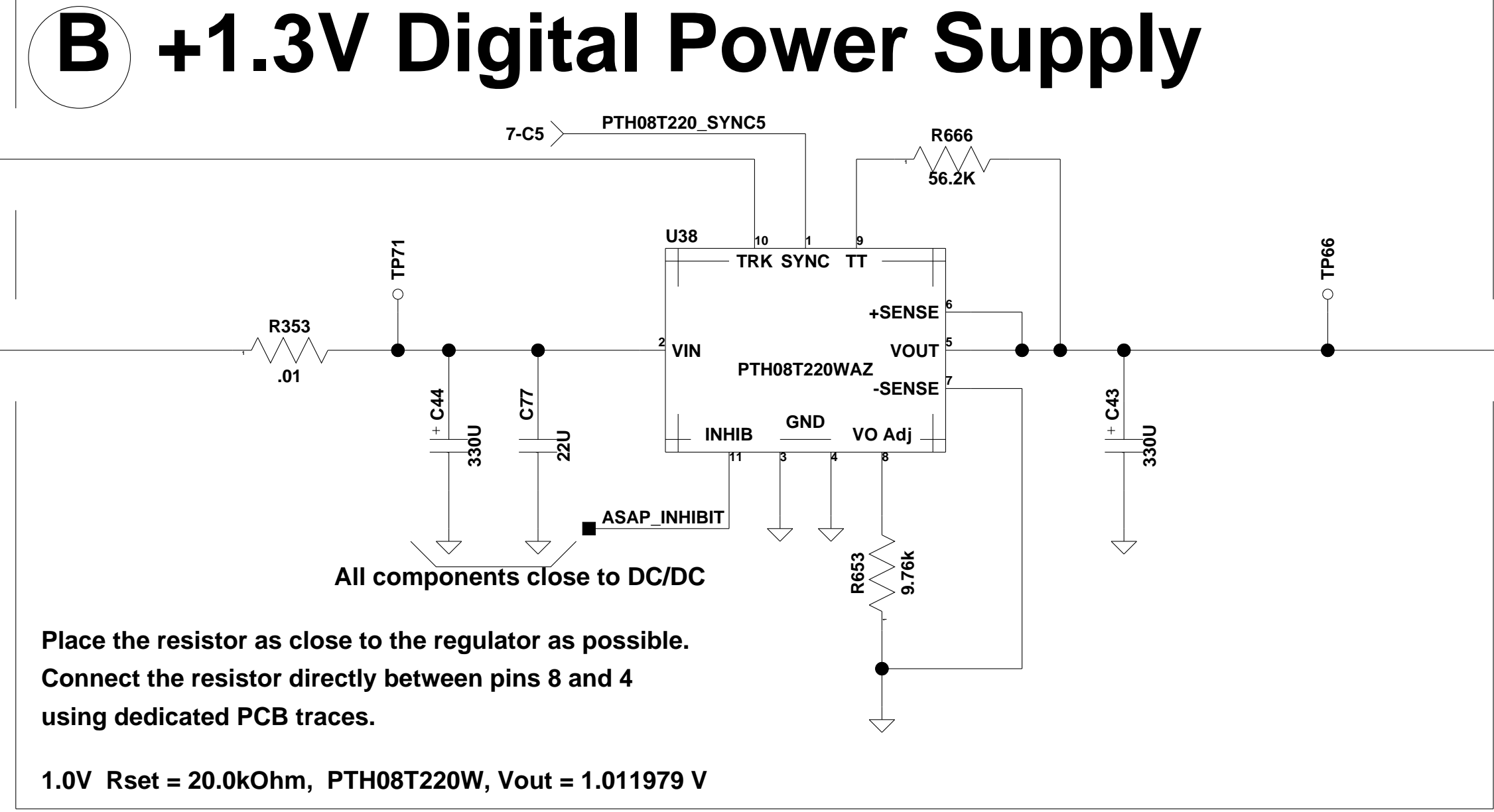
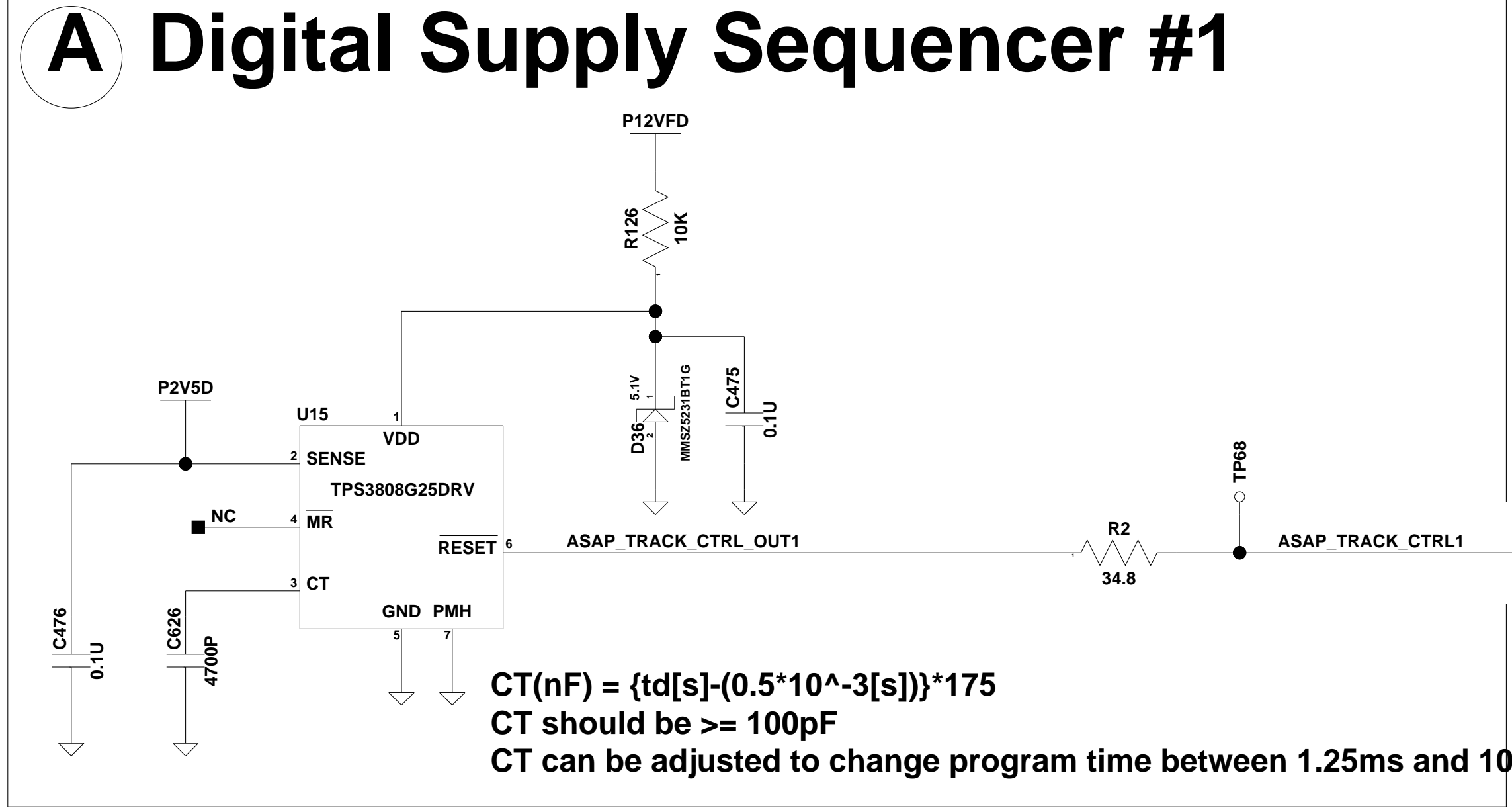


N 10MHz Reference LVDS to LVTTTL



AsAP Digital Power Regulation and Sequencing

- Digital Power Supply Sequence Order:
1. +12V Input
 2. +3.3V
 3. +2.5V
 4. +1.3V, +1V

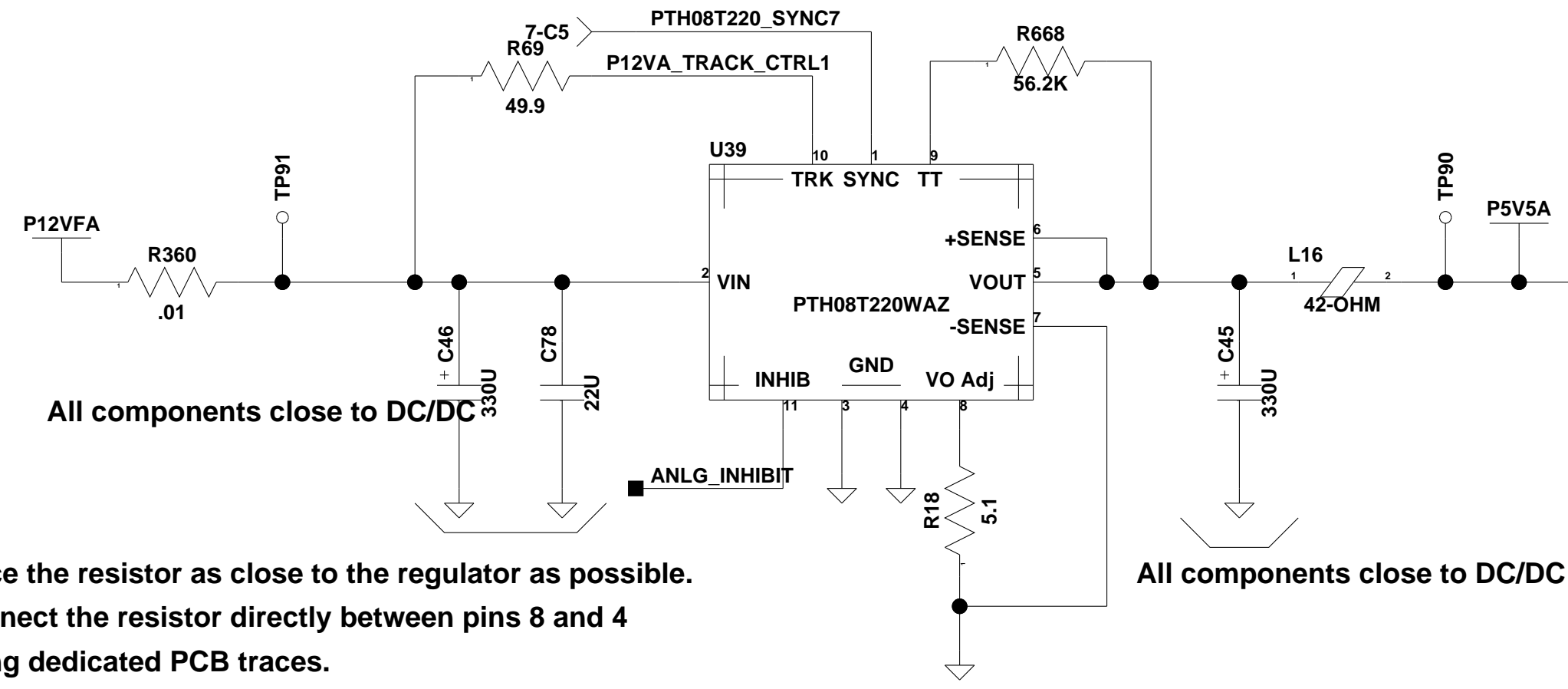


VLSI Computation LAB			
Title: ASAP DIGITAL POWER REGULATION AND SEQUENCING			
File: MEAS_MAIN_BOARD			
Created by: JEREMY W. WEBB	Date: 4-20-2009_13:35		
Modified by:	Date:		
PCB NO: 342	Size: D	Sheet 8 of 43	REV: 001

Analog Power Regulation - Part 1 of 2

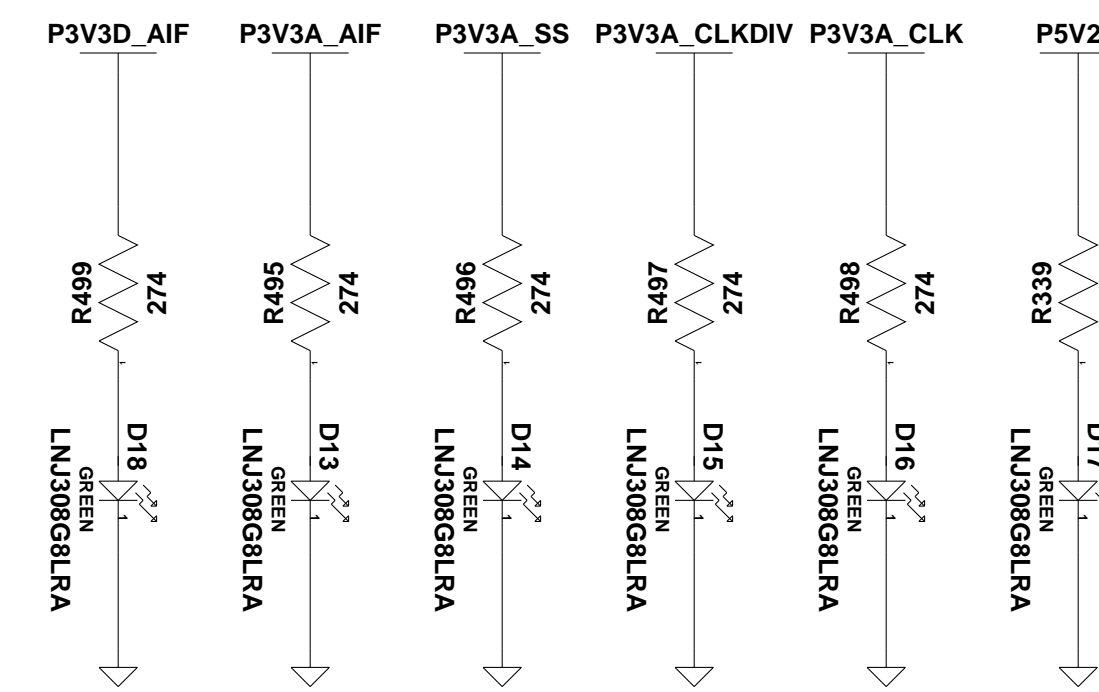
A +5.5V Analog Supply Regulation

5.5V Rset = 100 Ohm, PTH08T220W, Vout = 5.498027315 V



Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 8 and 4 using dedicated PCB traces.

B POWER LEDs



PLACE LEDs NEAR EDGE OF BOARD
Green LED (LNJ308G8LRA):
RLED = (VCC - VF)/IF
VF = 1.9V IF = 5mA

C +5.5V Filter

DCR: 21.8mOhm
Isat: 9.36A
Shielded

D +3.3V AIF Analog Supply Regulation

R1	R2	Vout
52.3k	30.1k	+3.3V

E +5.5V Filter

DCR: 21.8mOhm
Isat: 9.36A
Shielded

F +3.3V AIF Digital Supply Regulation

R1	R2	Vout
52.3k	30.1k	+3.3V

G +5.5V Filter

DCR: 21.8mOhm
Isat: 9.36A
Shielded

H +3.3V Signal Source Analog Supply Regulation

R1	R2	Vout
52.3k	30.1k	+3.3V

I +5.5V Filter

DCR: 21.8mOhm
Isat: 9.36A
Shielded

J +3.3V Clock Divider Analog Supply Regulation

R1	R2	Vout
52.3k	30.1k	+3.3V

K +5.5V Filter

DCR: 21.8mOhm
Isat: 9.36A
Shielded

L +3.3V Clock Analog Supply Regulation

R1	R2	Vout
52.3k	30.1k	+3.3V

M +5.5V Filter

DCR: 21.8mOhm
Isat: 9.36A
Shielded

N +5.2V Analog Supply Regulation

Power Dissipation = (5.5V - 5V)*1A = 500mW

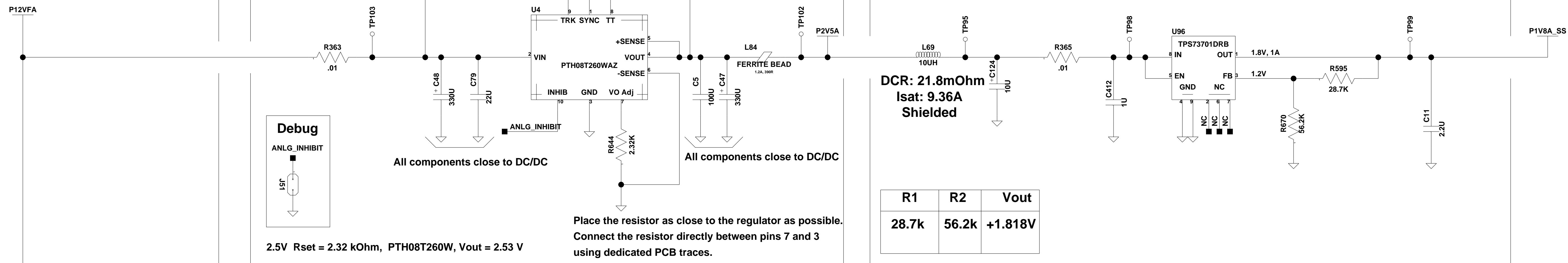
Vout = 1.21 * (1 + (R1/243)) = 5.210849383 V

All components close to TPS79601

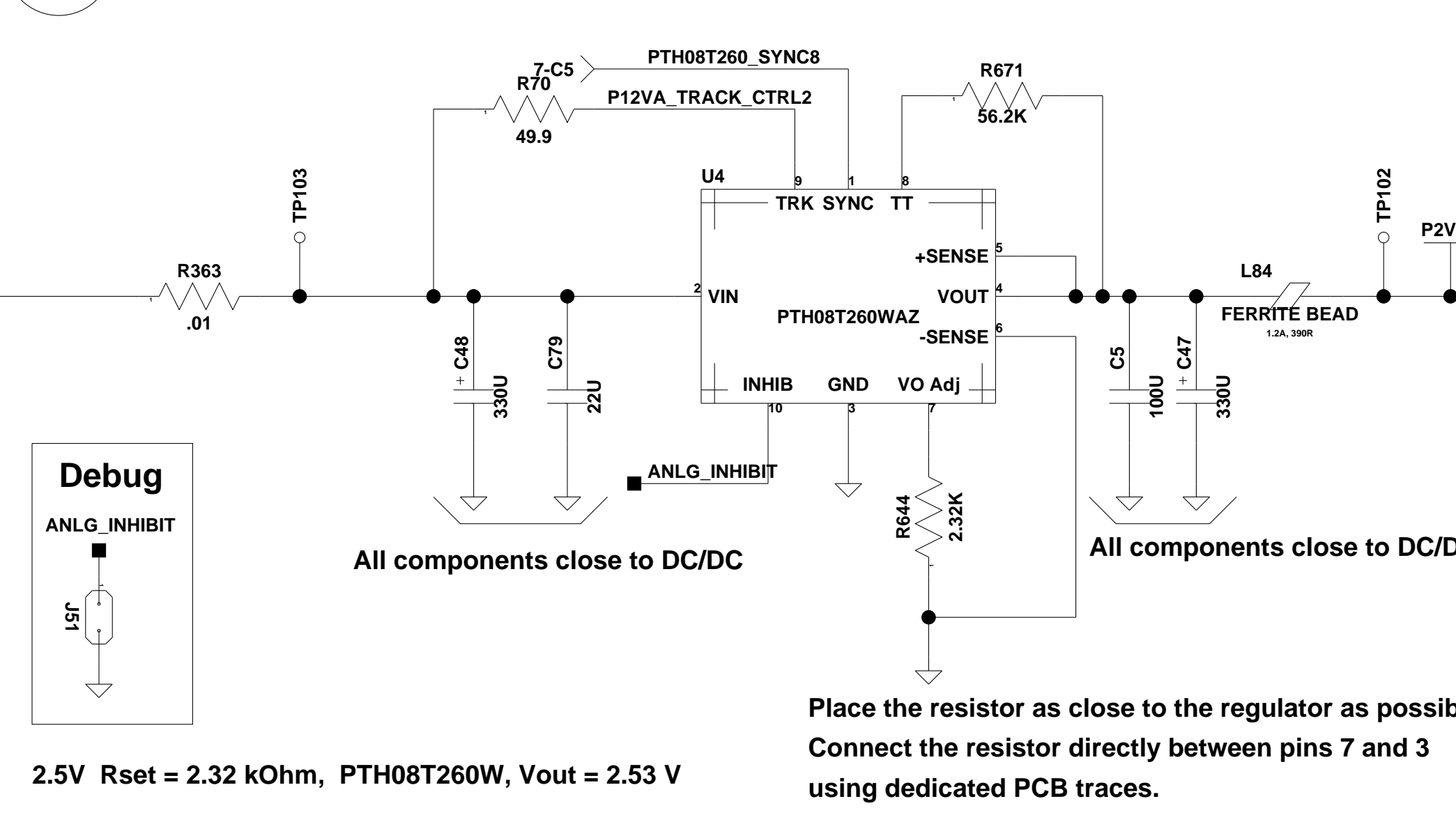
All components close to TPS79601

Analog Power Regulation - Part 2 of 2

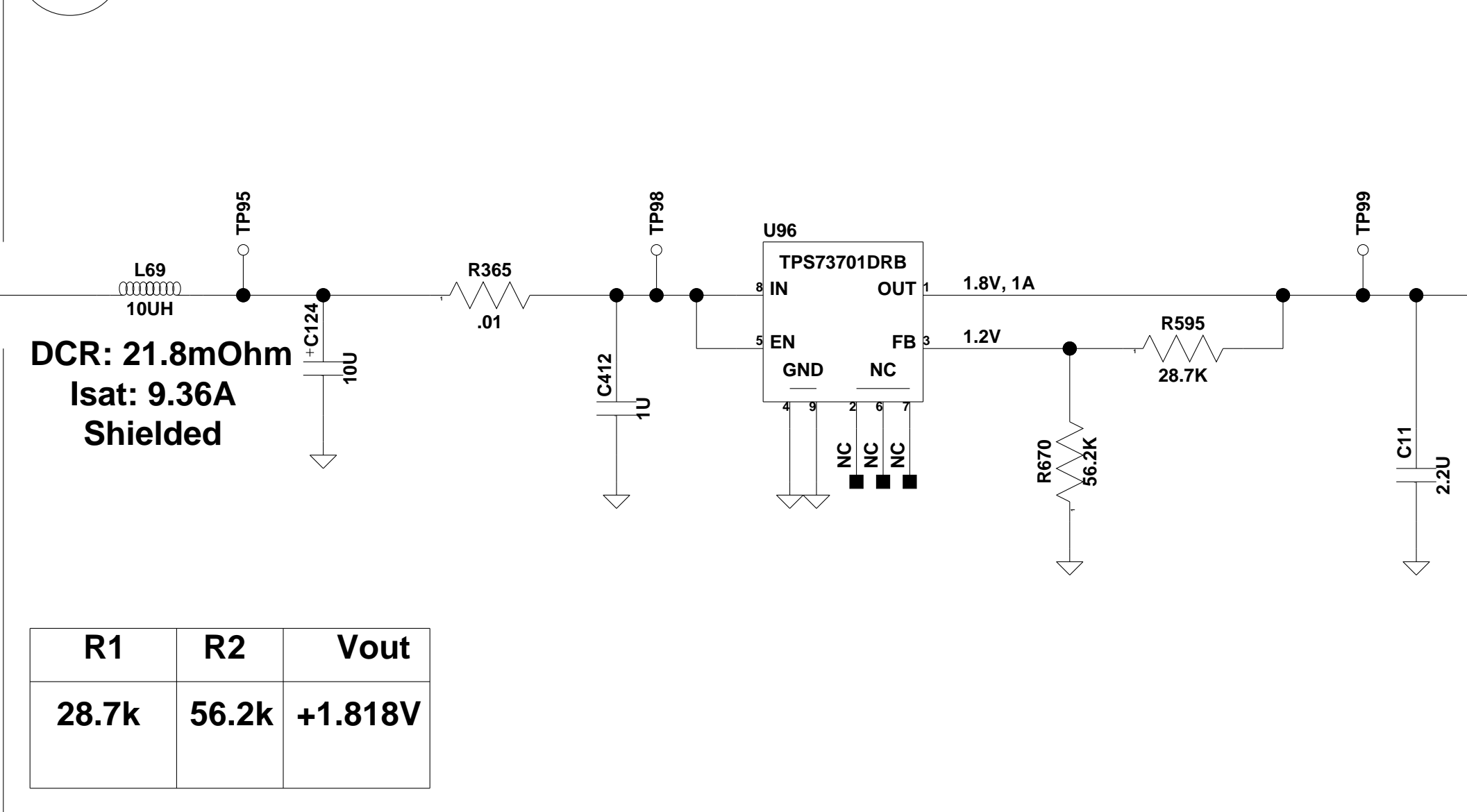
A +12V Analog



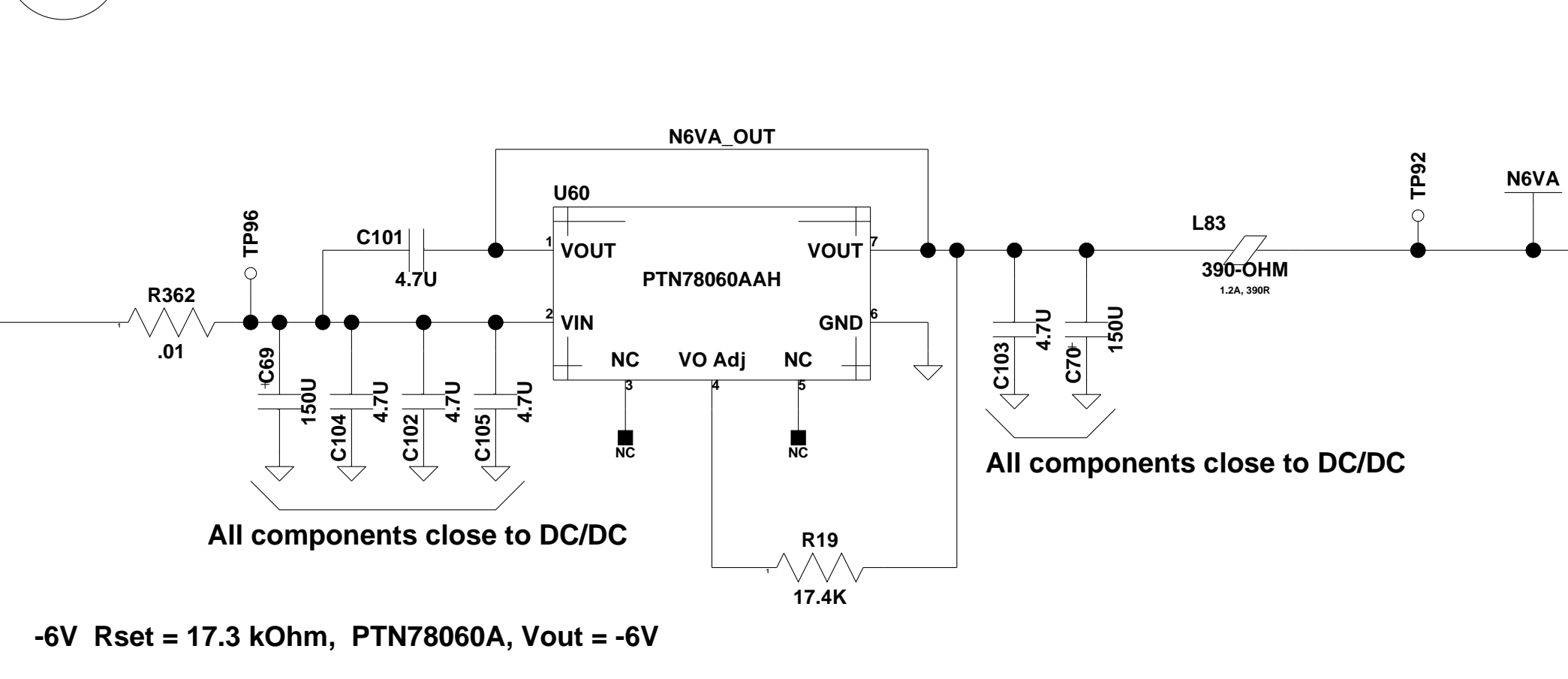
B +2.5V Analog Supply Regulation



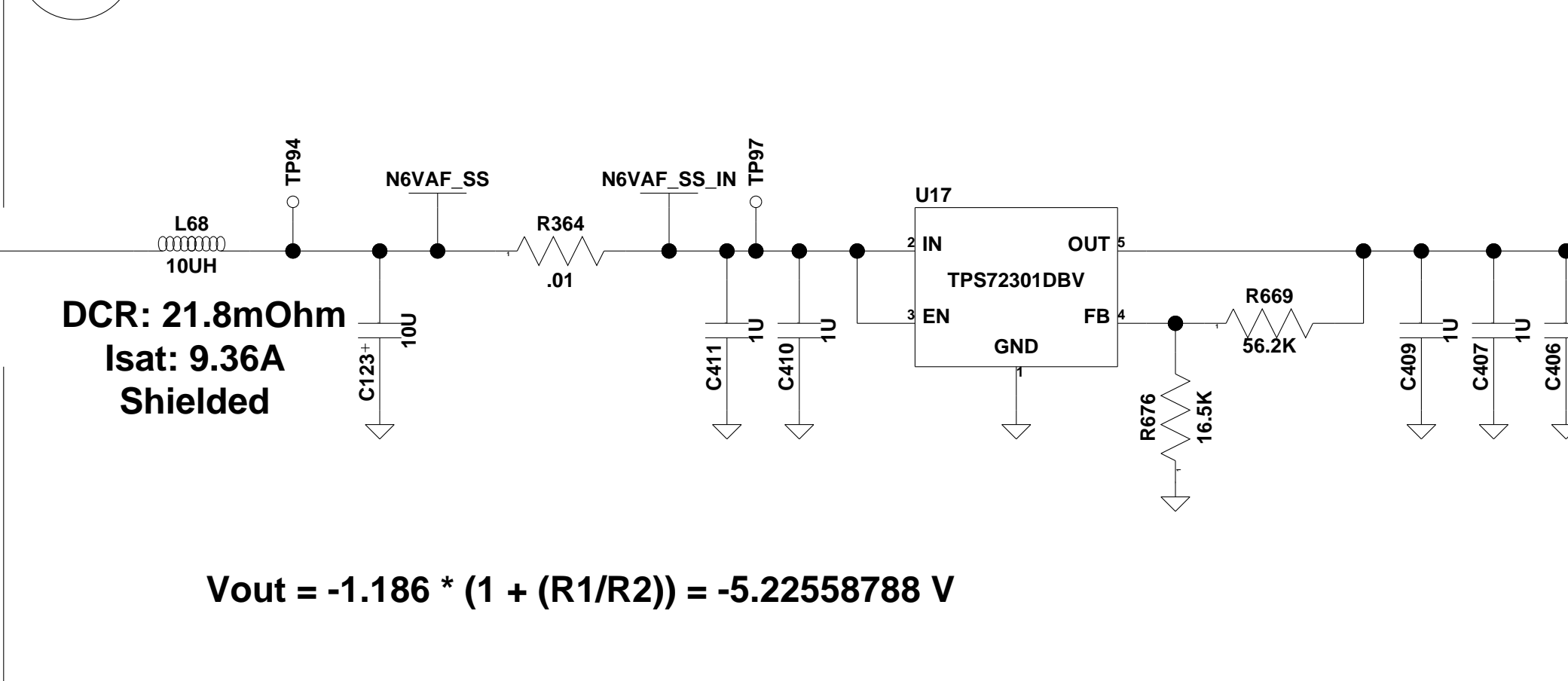
C +1.8V Analog Supply Regulation



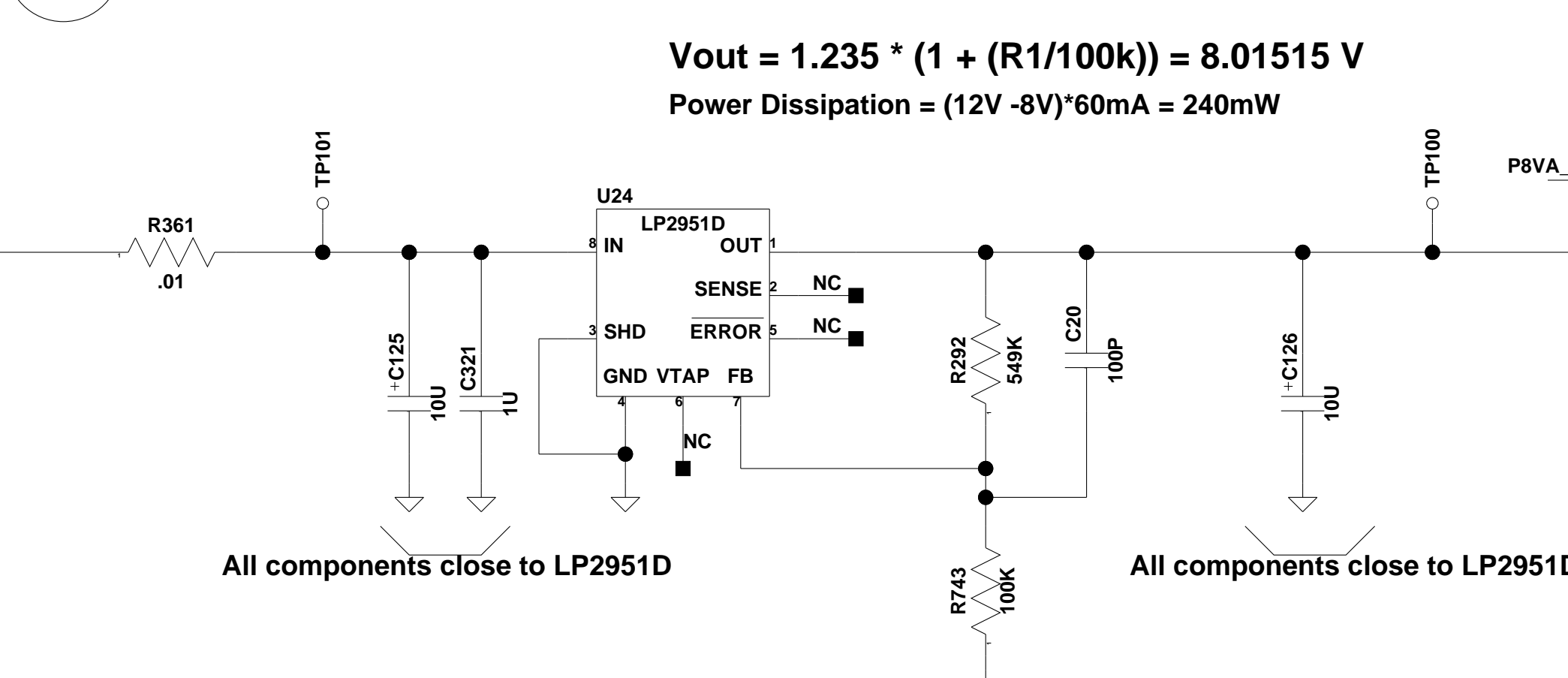
D -6V Analog Supply Regulation



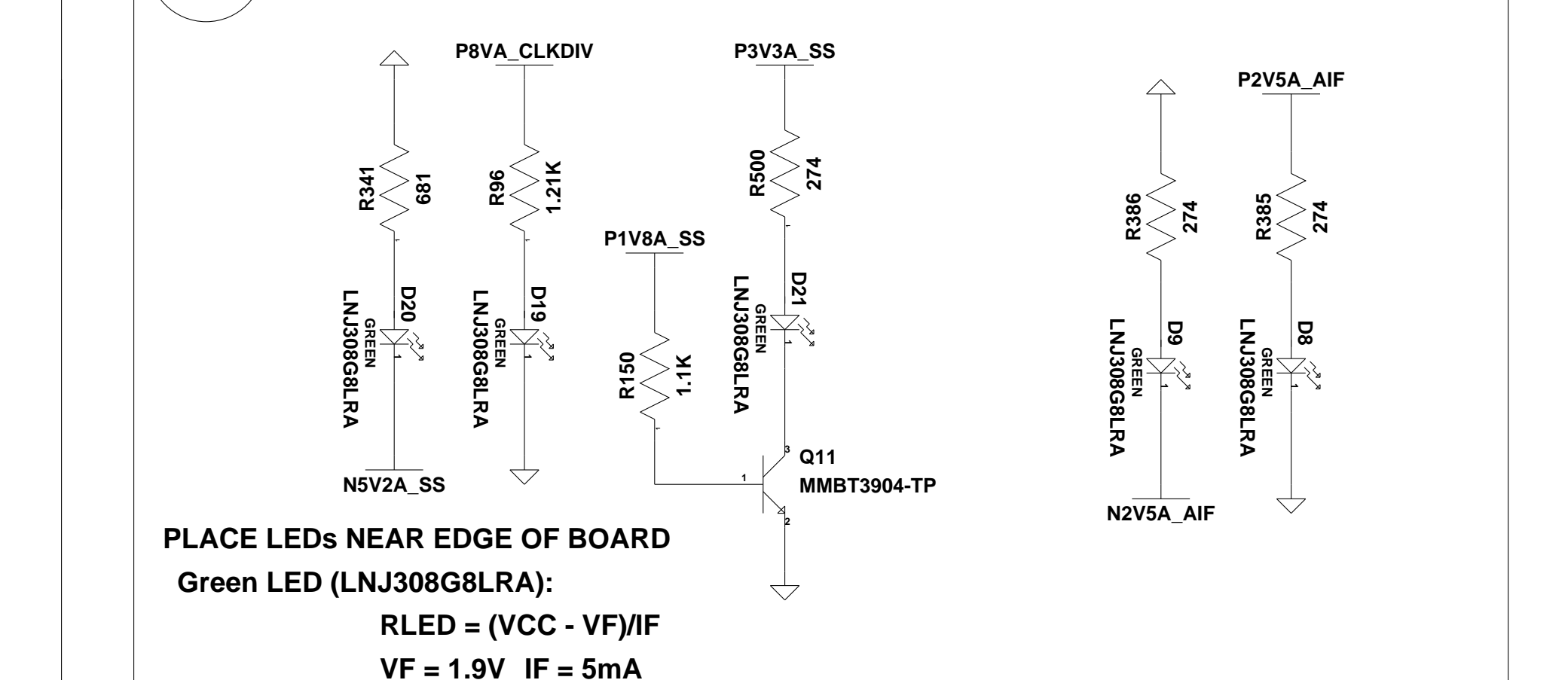
E -5.2V Analog Supply Regulation



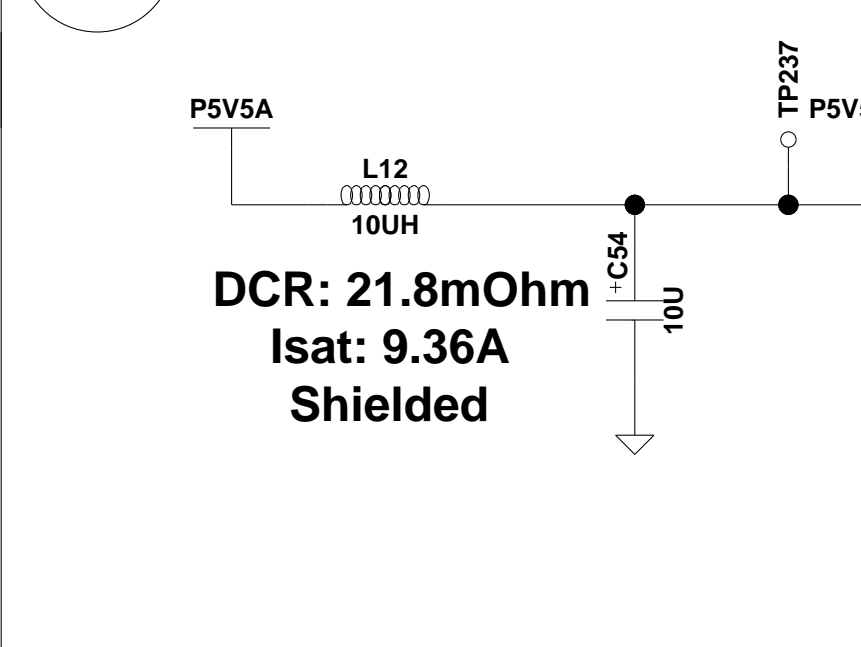
F +8V Analog Supply Regulation



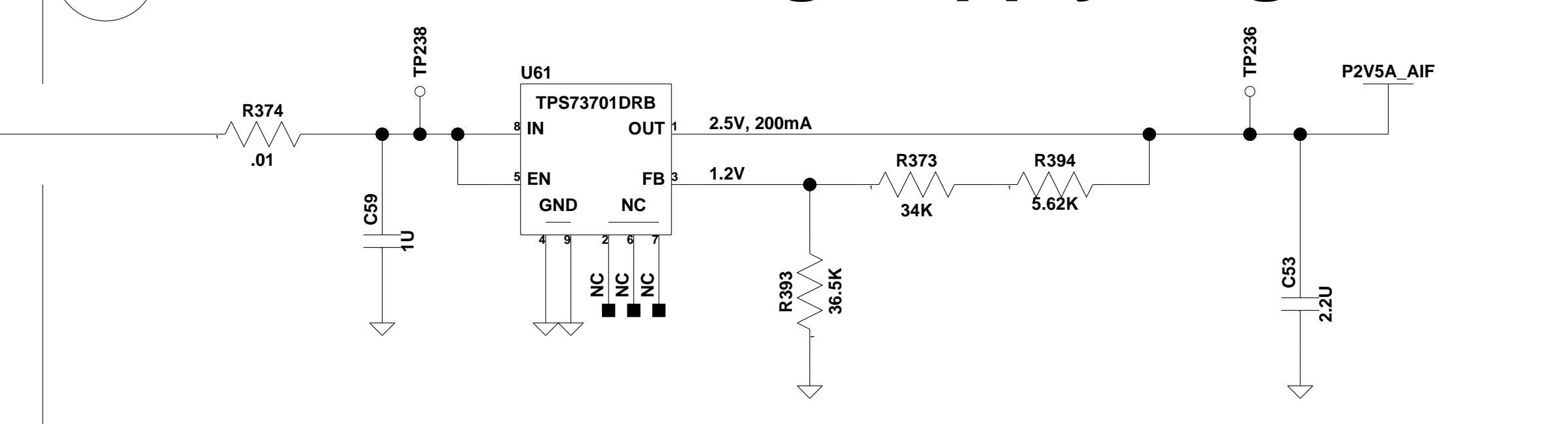
G POWER LEDs



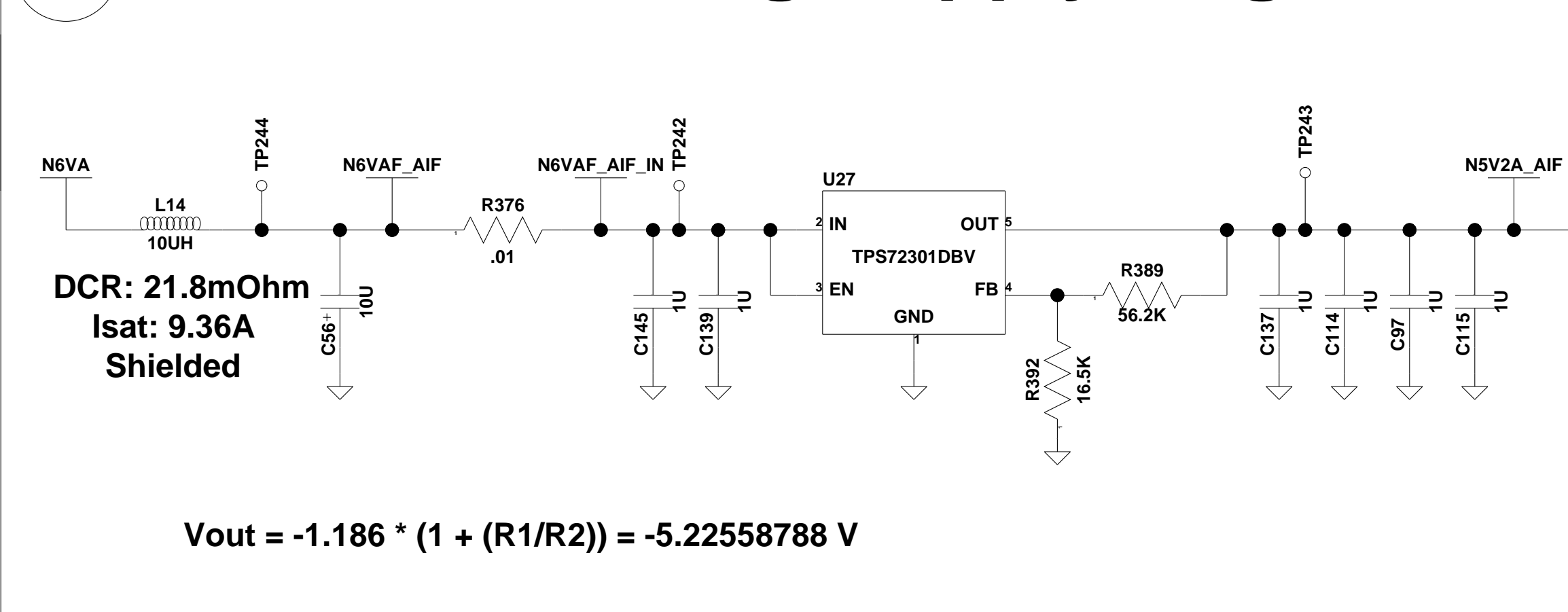
H +5.5V Filter



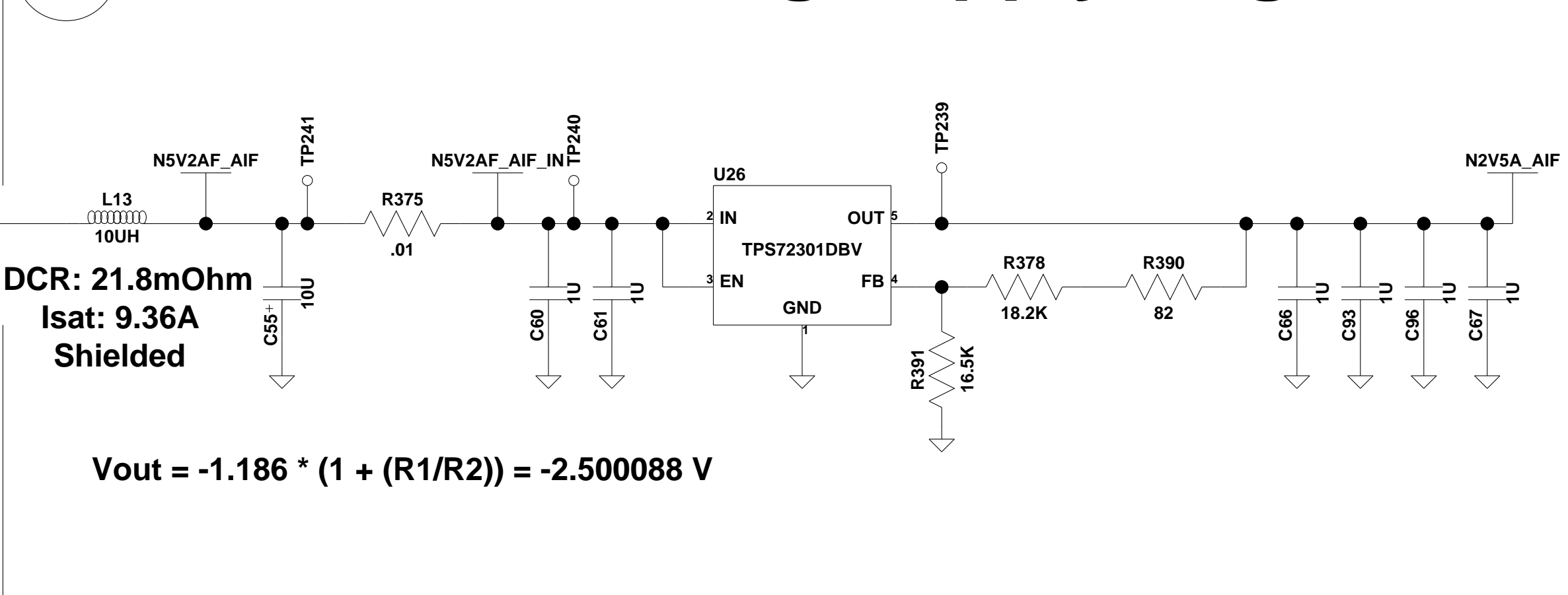
I +2.5V AIF Analog Supply Regulation



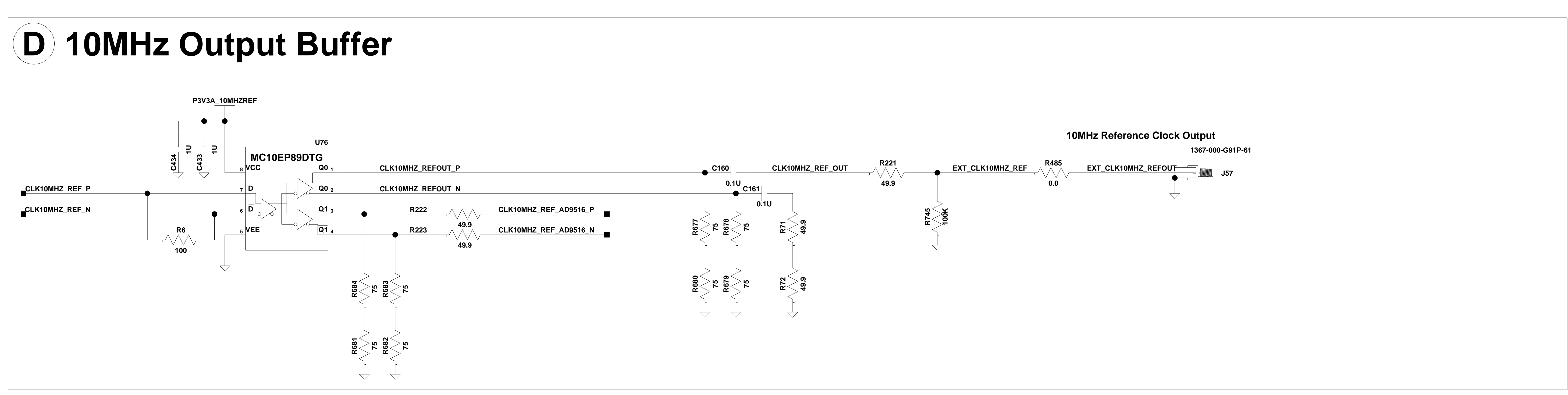
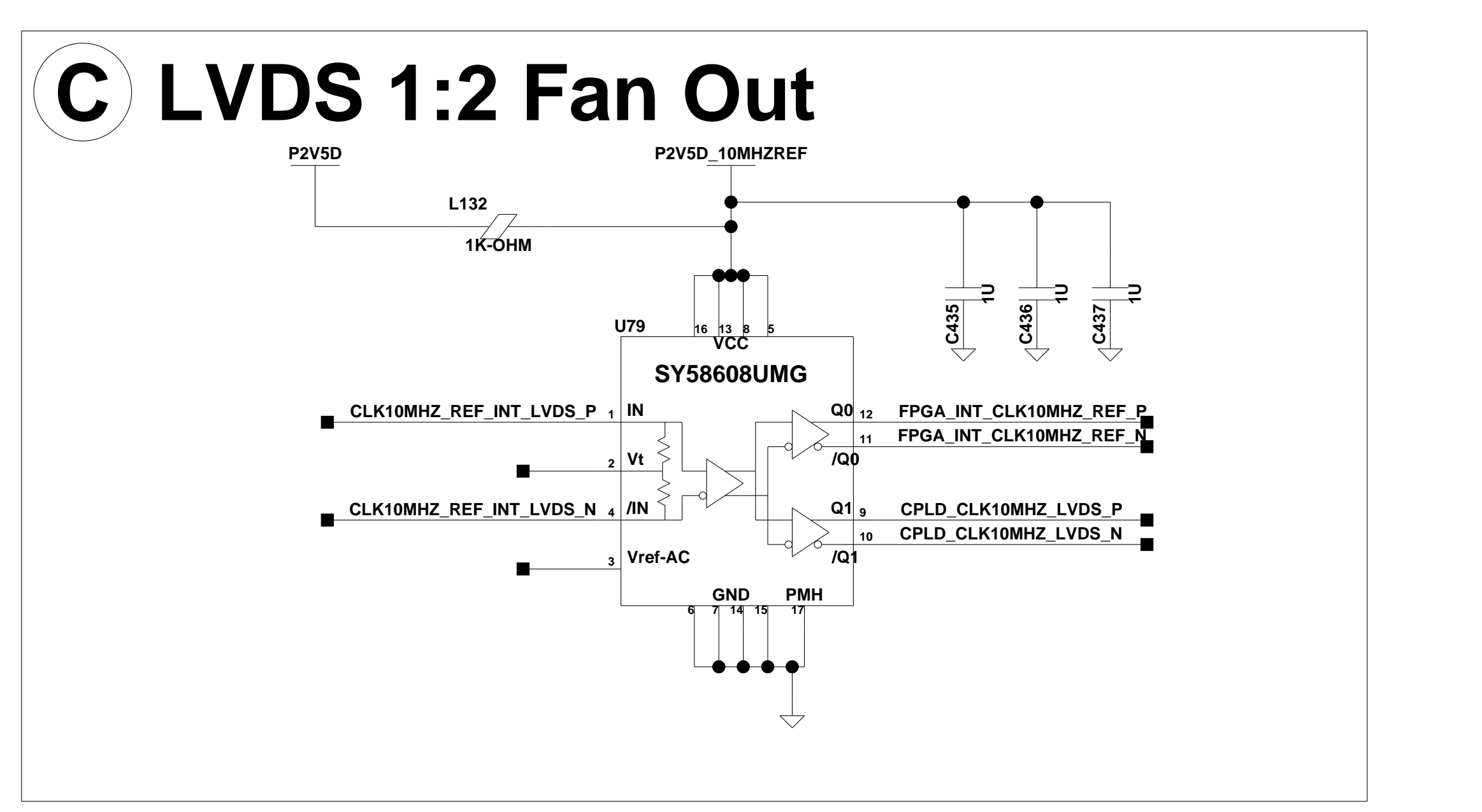
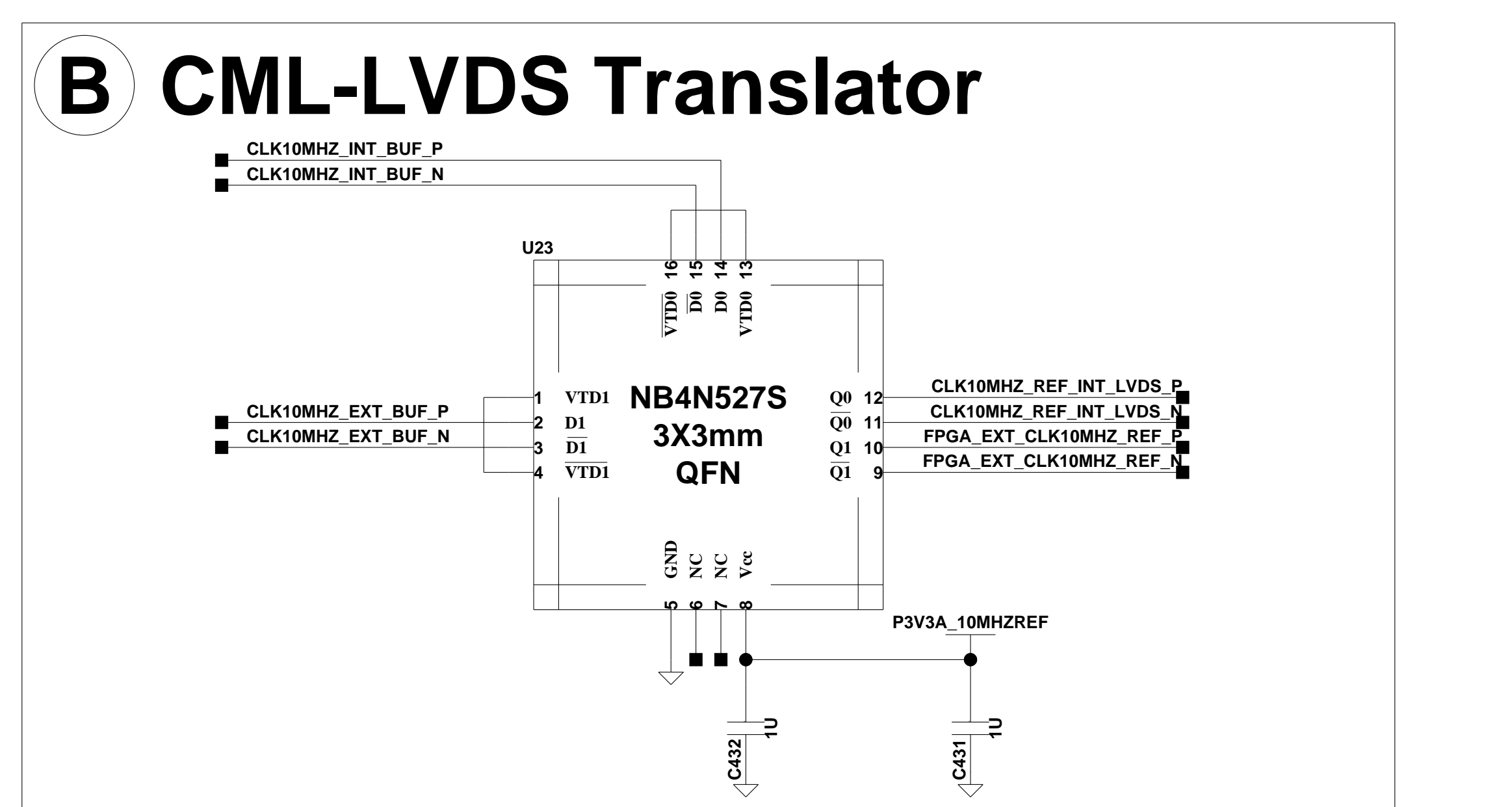
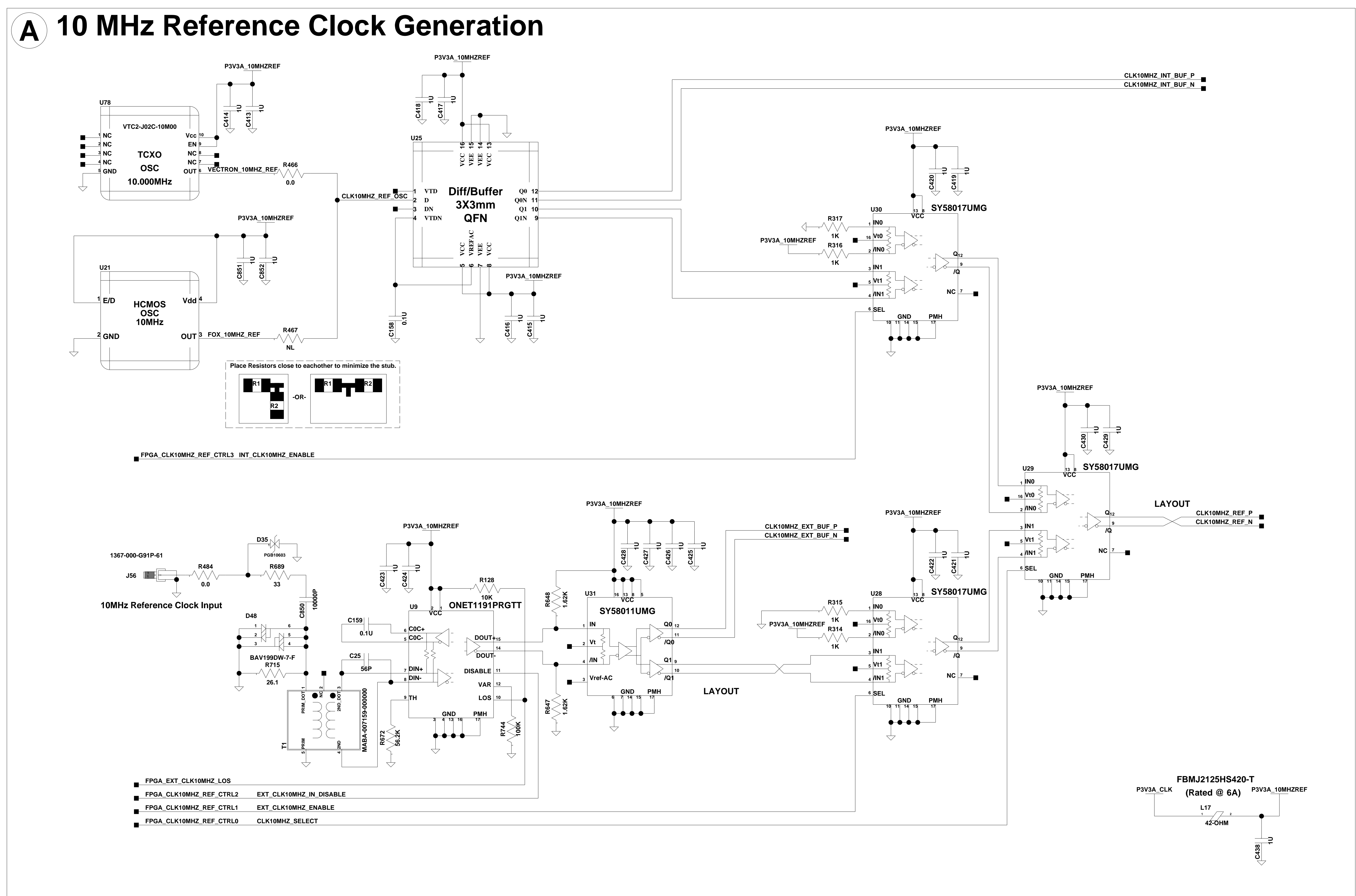
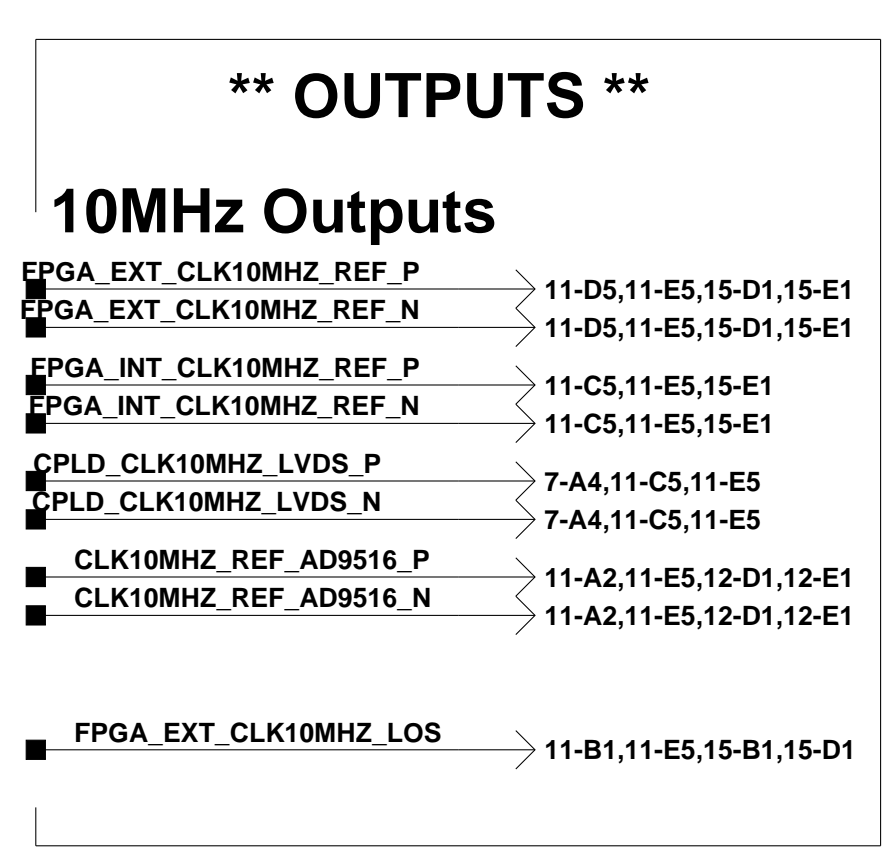
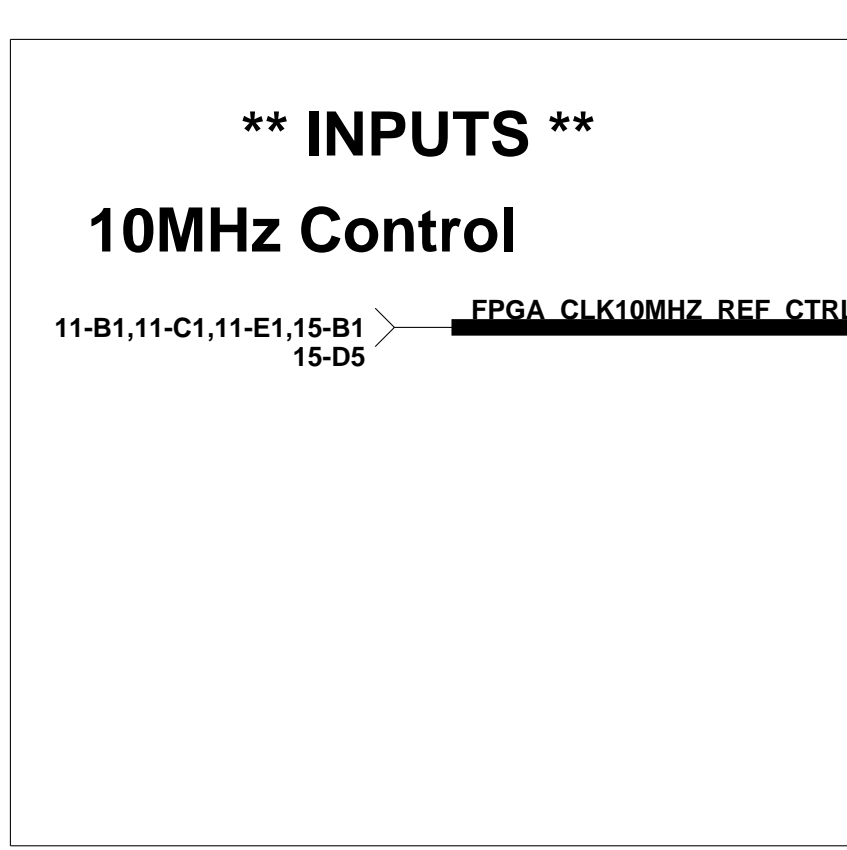
J -5.2V AIF Analog Supply Regulation



K -2.5V AIF Analog Supply Regulation



10MHz Reference Clock Generation



VLSI Computation LAB

Title: 10MHZ REFERENCE CLOCK GENERATION

File: MEAS_MAIN_BOARD

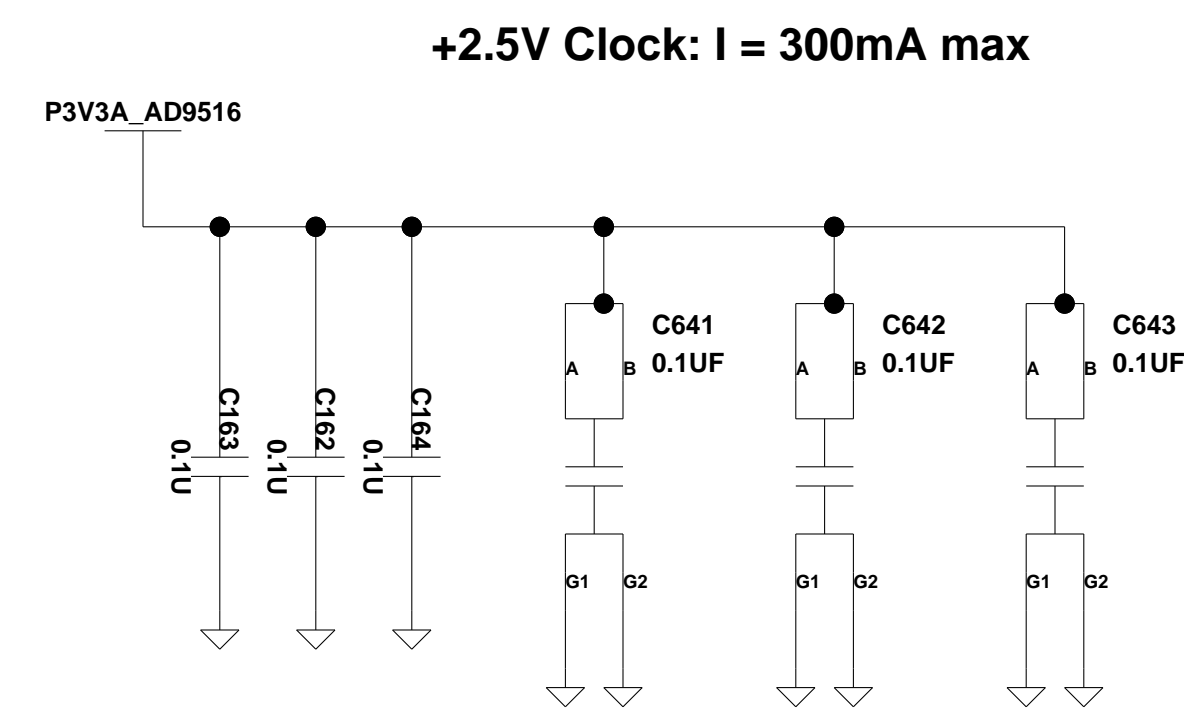
Created by: JEREMY W. WEBB Date: 4-20-2009 13:35

Modified by: Date:

PCB NO: PCBNUMBER=342 Size: E Sheet: 4 SHEET TOTAL=4 REVISION:

HIGH-SPEED CLOCK GENERATION

A AD9516 LVPECL Power Supply Decoupling



+2.5V Clock: I = 300mA max

** OUTPUTS **

High-Speed Clock Outputs (LVPECL)

- FPGA ASAP_CLKIN_P → 12-B3,12-E5,22-E1,22-E3
- FPGA ASAP_CLKIN_N → 12-B3,12-E5,22-E1,22-E3
- FPGA DSP_CLKIN_P → 12-A3,12-E5,22-E1,22-E3
- FPGA DSP_CLKIN_N → 12-A3,12-E5,22-E1,22-E3
- AIF_ADC_CLKIN_P → 12-B2,12-E5,33-C3
- AIF_ADC_CLKIN_N → 12-B2,12-E5,33-C3
- SS_DAC_CLKIN_P → 12-A2,12-E5,34-E1
- SS_DAC_CLKIN_N → 12-A2,12-E5,34-E1

High-Speed Clock Outputs (LVDS)

- FPGA_SRAM_CLK_P → 12-C3,12-E5,22-E1,22-E3
- FPGA_SRAM_CLK_N → 12-C3,12-E5,22-E1,22-E3
- FPGA_SDRAM_CLK_P → 12-C3,12-E5,22-E1,22-E3
- FPGA_SDRAM_CLK_N → 12-C3,12-E5,22-E1,22-E3

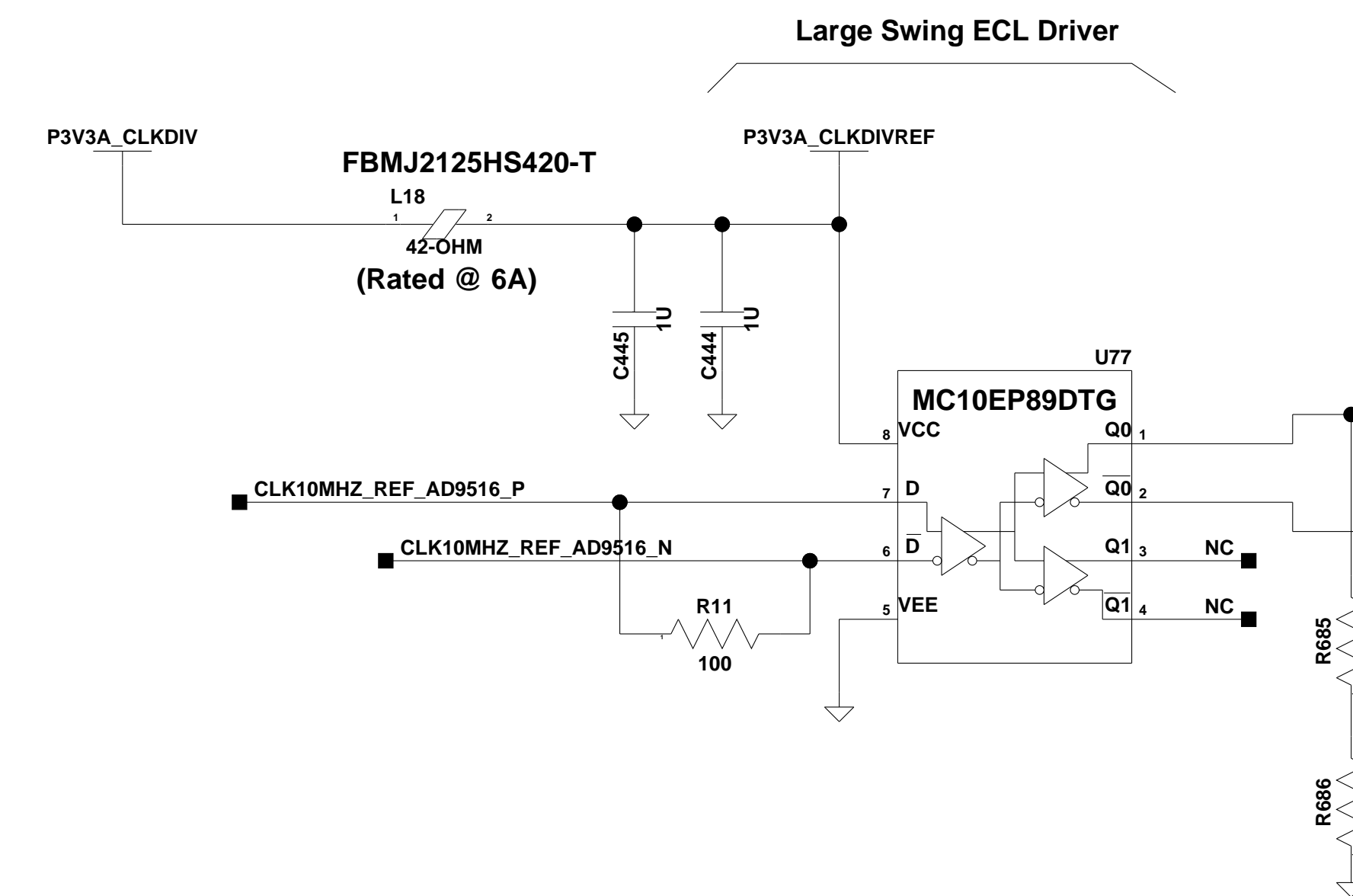
AD9516 Control

- FPGA_AD9516_SDO → 12-E5,15-C3,15-D1

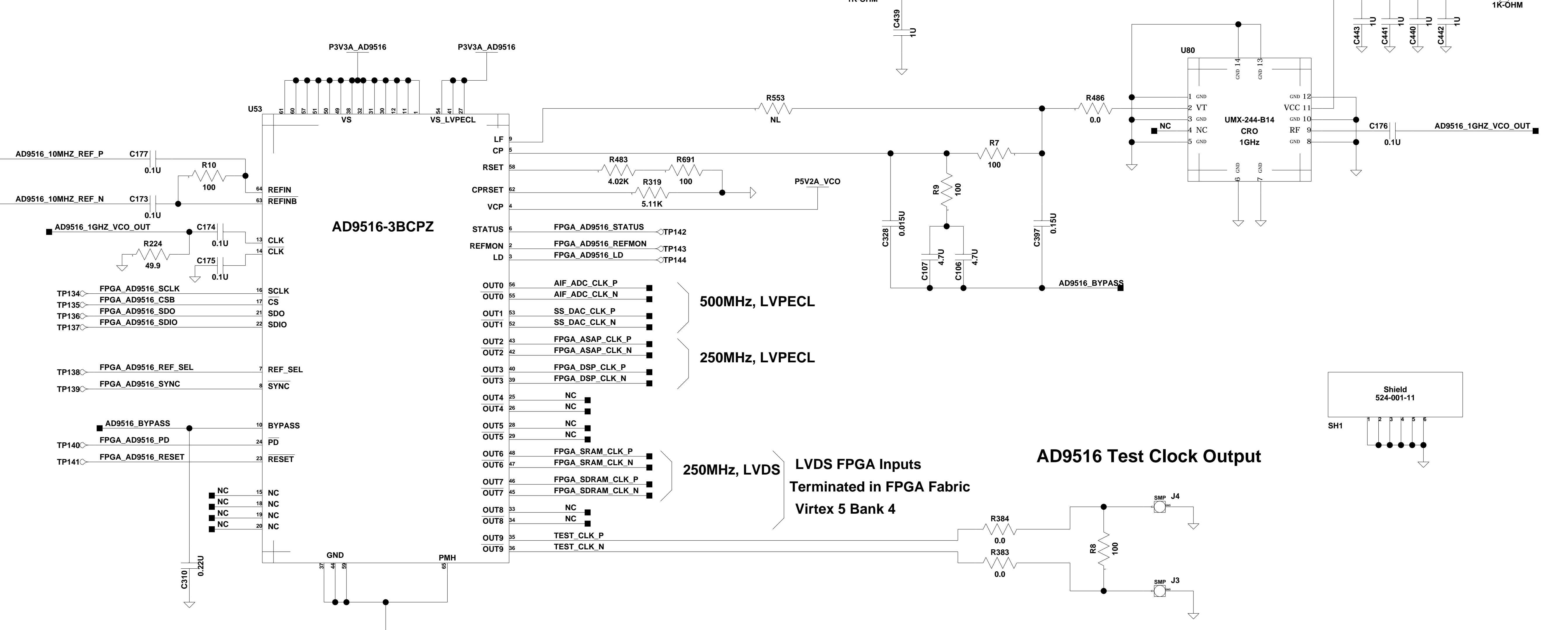
AD9516 Status Signals

- FPGA_AD9516_STATUS → 12-E5,15-C3,15-D1
- FPGA_AD9516_REFMON → 12-E5,15-C3,15-D1
- FPGA_AD9516_LD → 12-D5,15-C3,15-D1

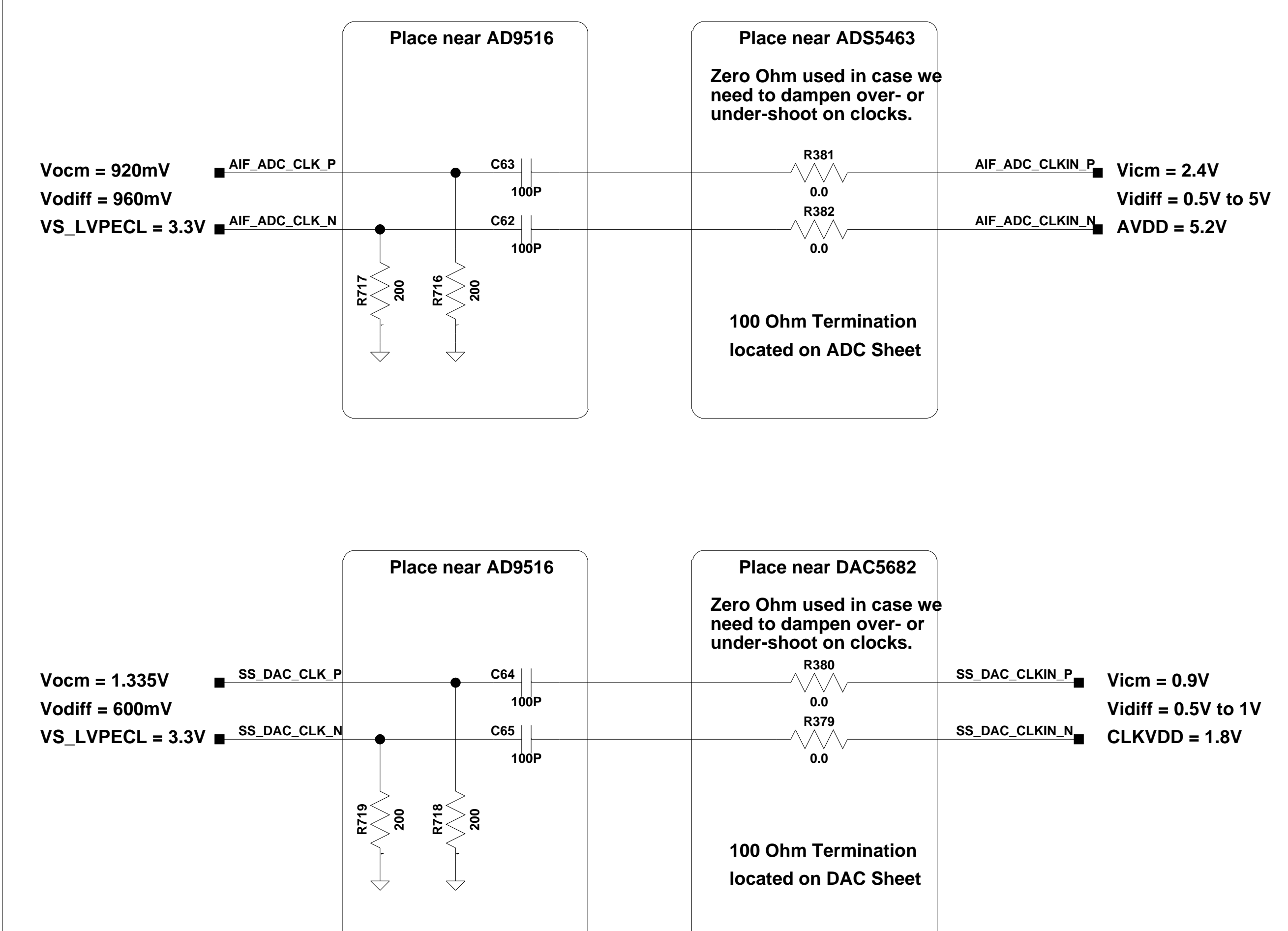
B 10 MHz Reference Clock Buffer



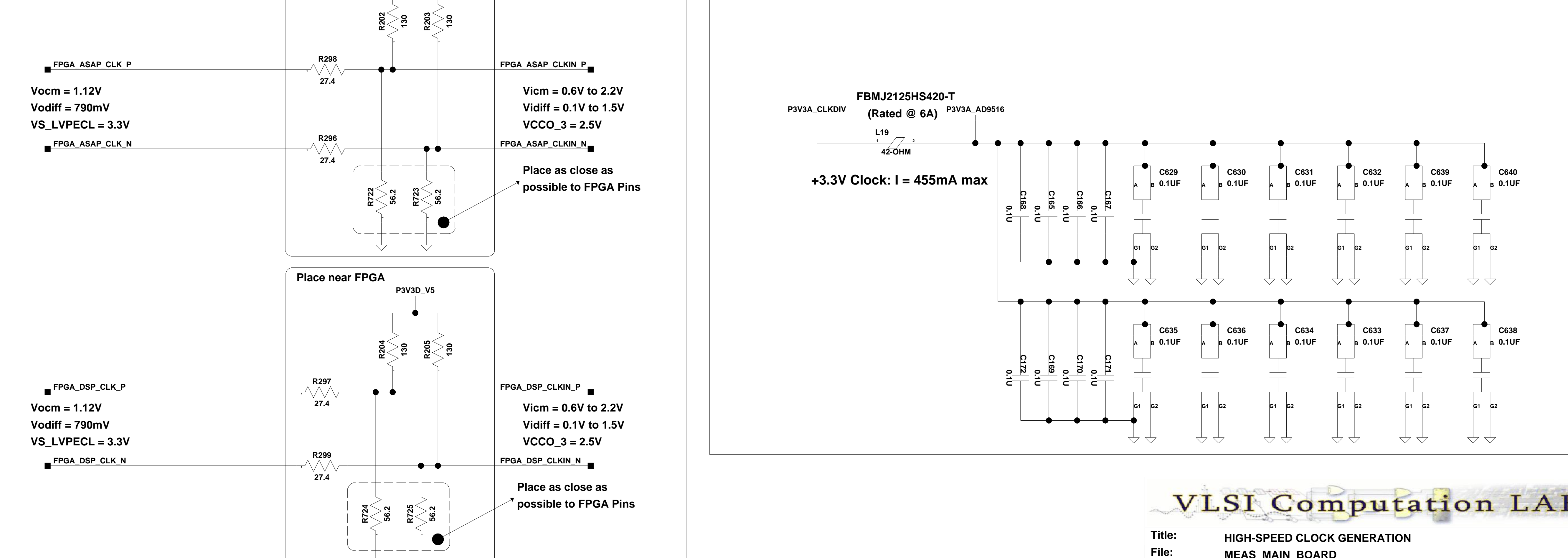
C AD9516 High-Speed Clock Generation PLL



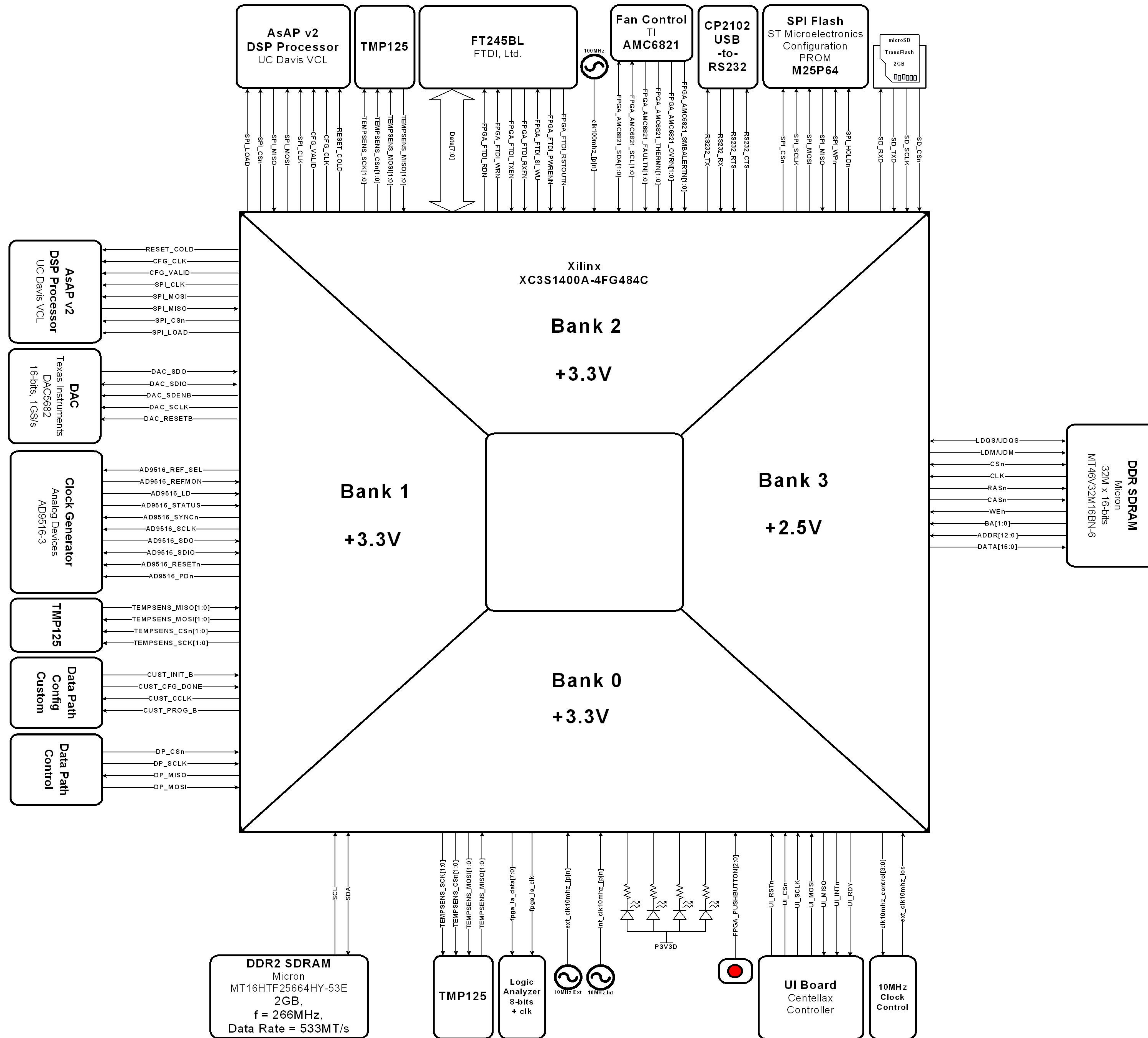
D AD9516 LVPECL Clock Terminations



E AD9516 Main Power Supply Decoupling



Control FPGA Digital Design



Xilinx Spartan-3A Control FPGA Configuration

**** INPUTS ****

CPU Interrupts
 14-D2,14-E1,17-A2,17-D5 → FPGA_UI_PROG0

AMC6821 Fan #2 Control
 6-B1,14-D4,14-E1 → FPGA_AMC6821_FAN2_OVRN

**** OUTPUTS ****

CPU Interrupts
 FPGA_UI_PROG1 → 14-D2,14-E5,17-A2,17-E1
 FPGA_UI_PROG2 → 14-E3,14-E5,17-A2,17-E1

AMC6821 Fan #2 Control
 FPGA_AMC6821_FAN2_SDA → 6-A4,14-D4,14-E5
 FPGA_AMC6821_FAN2_SCK → 6-A4,14-D4,14-E5

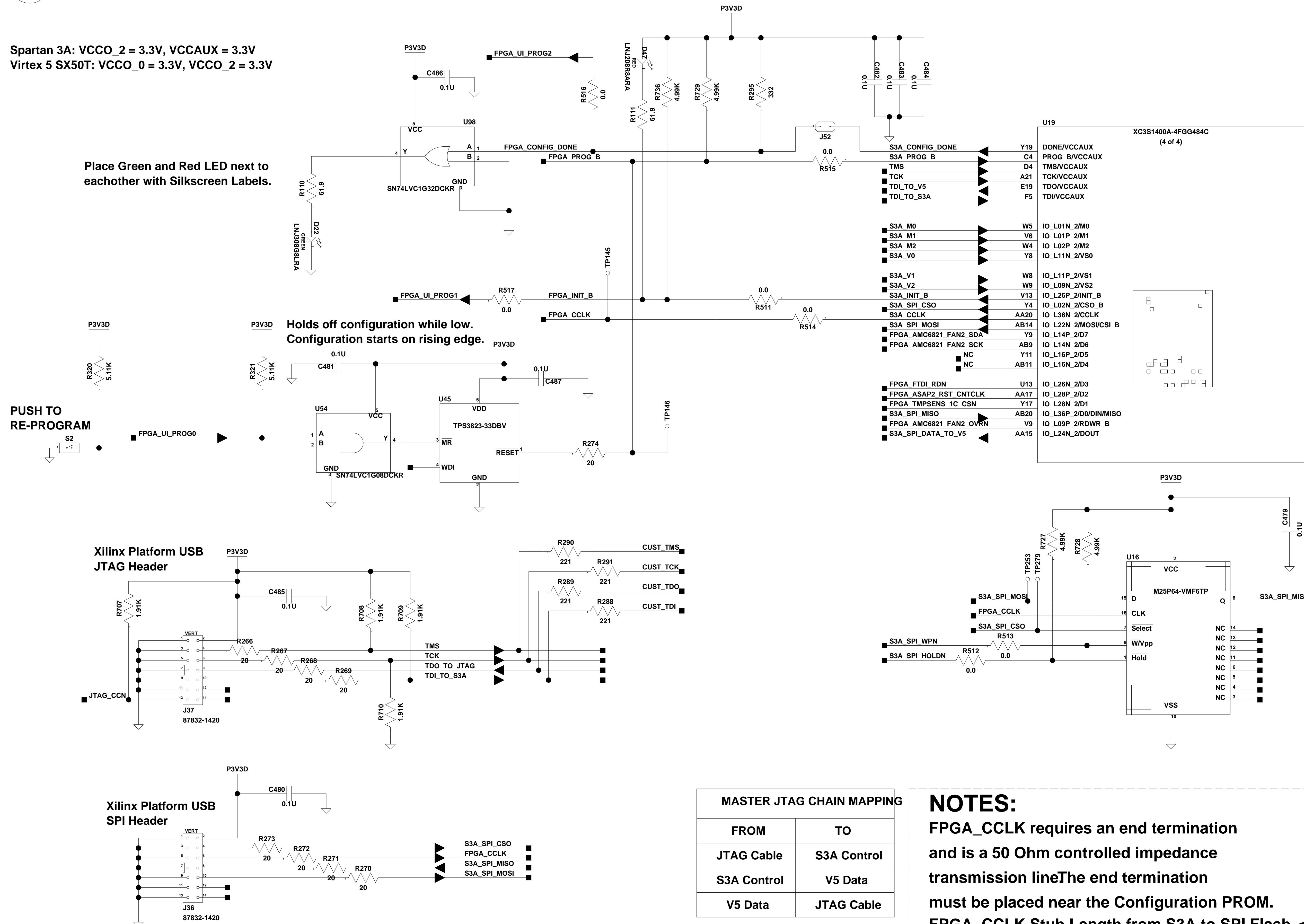
FT245BL USB Interface
 FPGA_FTDI_RDN → 14-D4,14-E5,17-B5,17-D1

AsAP 2 Config Input
 FPGA_ASAP2_RST_CNTCLK → 14-D4,14-E5,40-D1,40-E1

Temp Sensor Col. 1
 FPGA_TMPSENS_1C_CSN → 14-D4,14-E5,20-E1,20-E2

A Configuration SPI Flash PROM / JTAG Interface

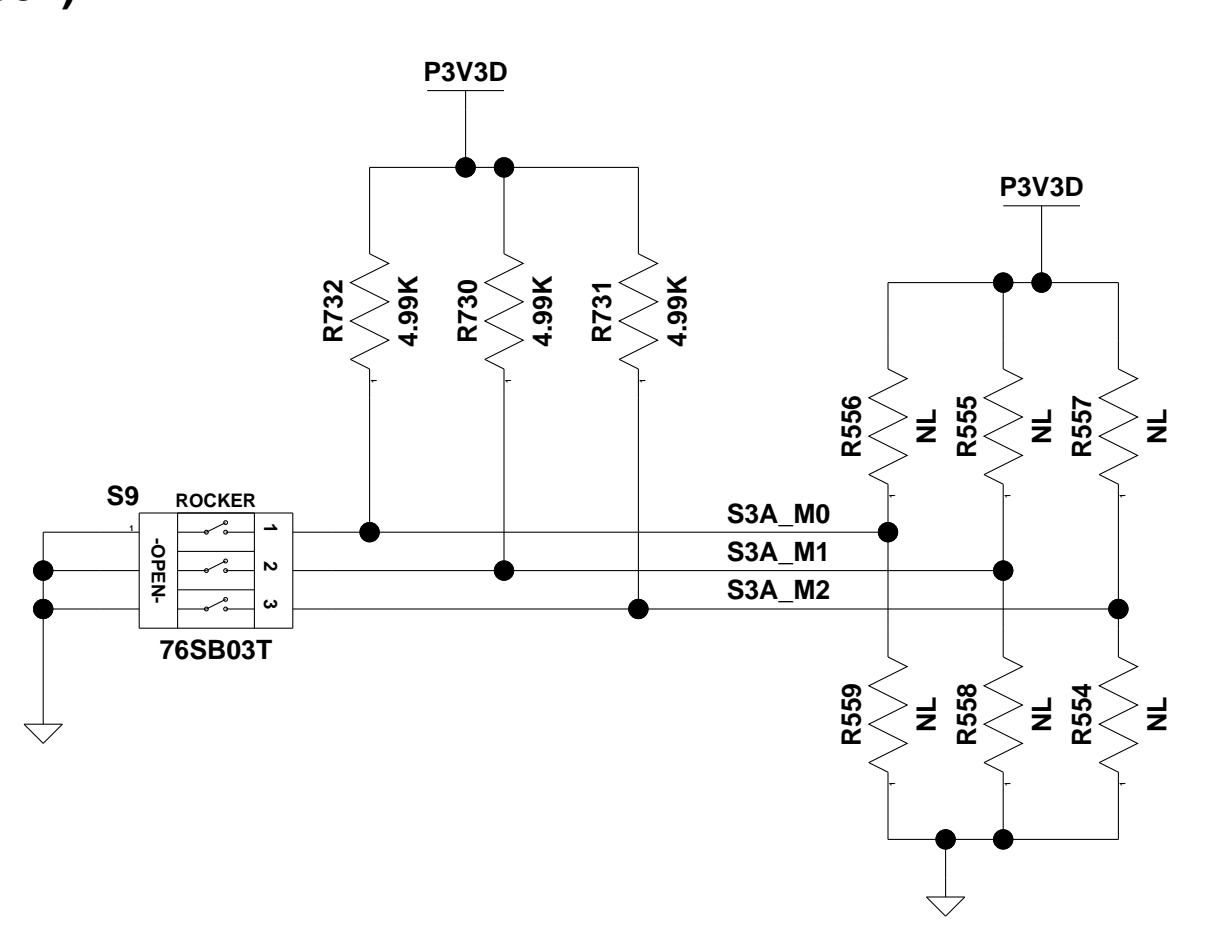
Spartan 3A: VCCO_2 = 3.3V, VCCAUX = 3.3V
 Virtex 5 SX50T: VCCO_0 = 3.3V, VCCO_2 = 3.3V



B Spartan-3A FPGA CONFIG MODE

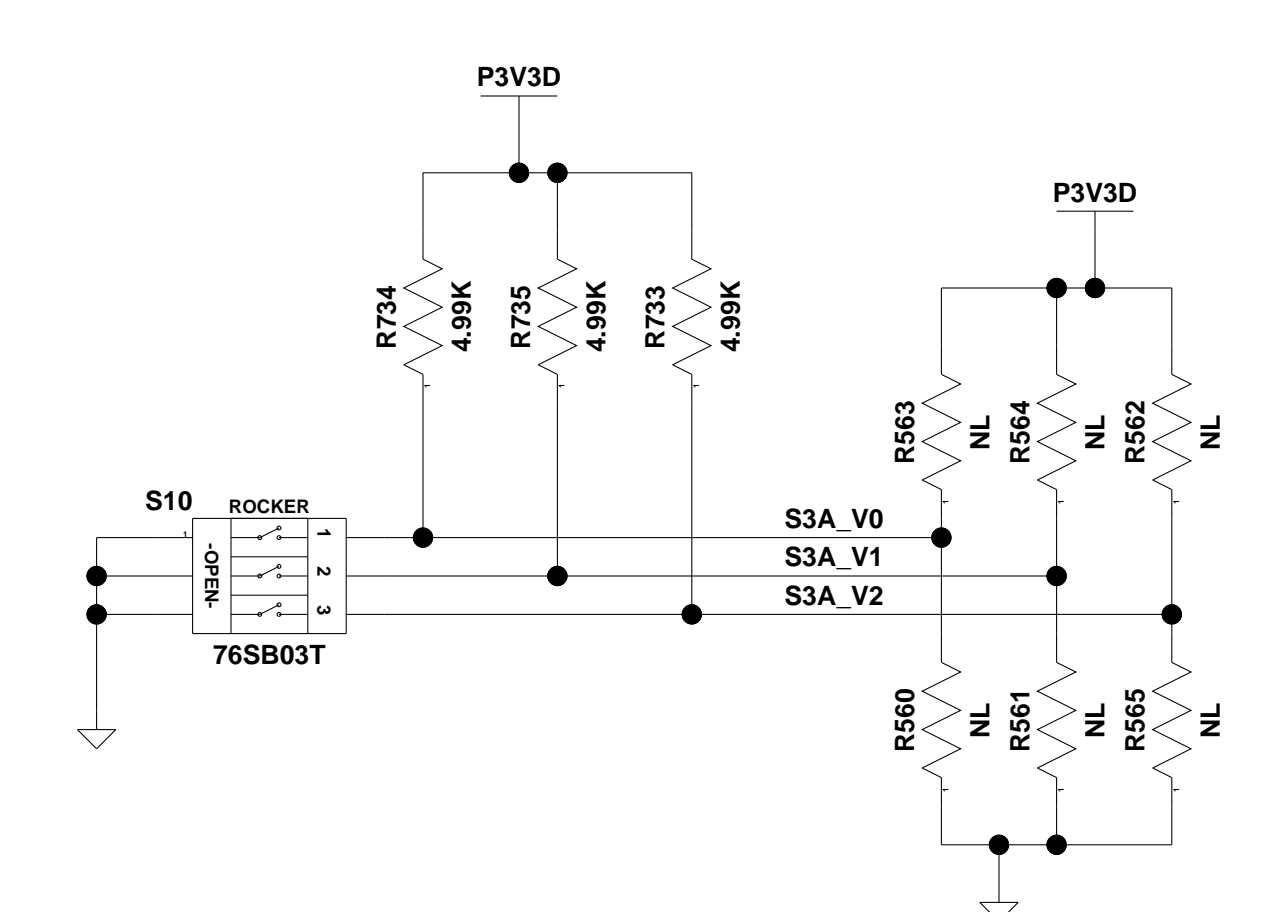
For more information see Xilinx Spartan 3A Configuration Guide (UG332)

CONFIG MODE	M2	M1	M0	DATA WIDTH	CCLK Direction
Master Serial	0	0	0	1 bit	Output
Master SPI	0	0	1	1 bit	Output
Master BPI-Up	0	1	0	8, 16 bits	Output
RSVD	0	1	1	RSVD	RSVD
RSVD	1	0	0	RSVD	RSVD
JTAG	1	0	1	1 bit	Input (TCK)
Slave Parallel	1	1	0	8, 16, 32 bits	Input
Slave Serial	1	1	1	1 bit	Input



C Spartan-3A FPGA SPI MODE

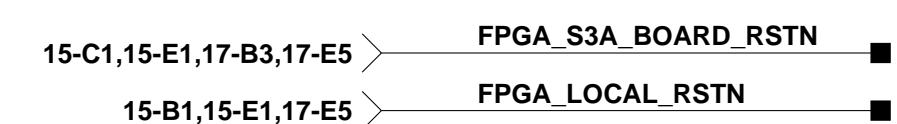
VS2	VS1	VS0	READ CMD	HEX CMD CODE
1	1	1	Fast Read	0x0B
1	0	1	Read	0x03
1	1	0	Read Array	0xE8
OTHERS			RESERVED	



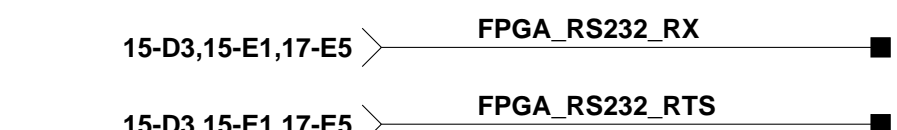
Xilinx Spartan-3A Control FPGA I/O

*** INPUTS ***

Board Reset



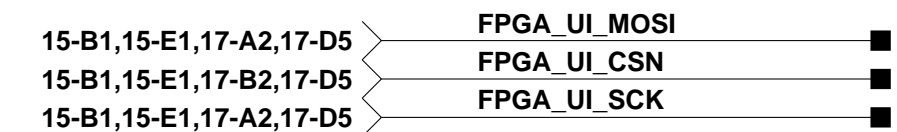
USB to RS-232 Interface



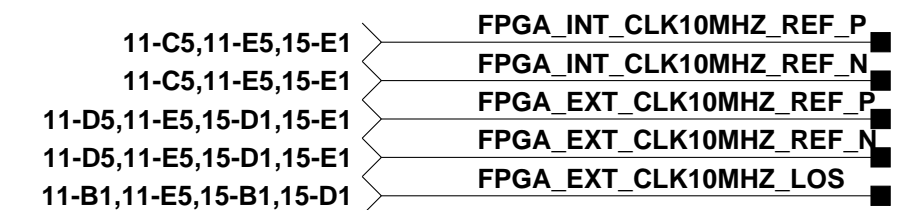
Debug Push Buttons



CPU Interface



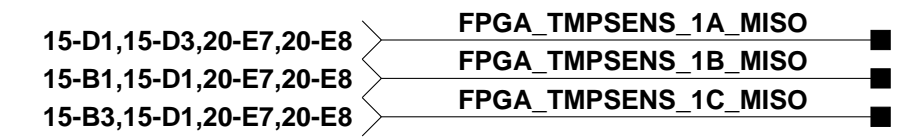
10MHz Reference Clock



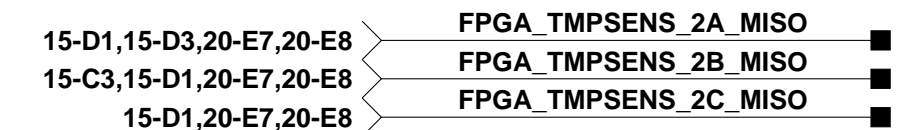
MicroSD Interface



Temp Sensor Col. 1



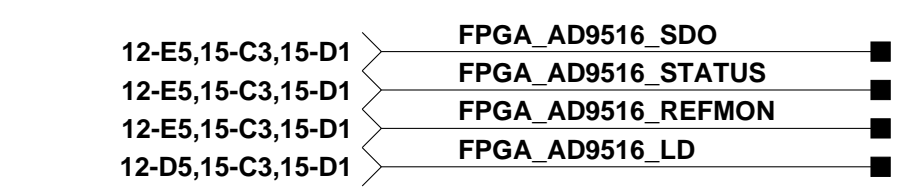
Temp Sensor Col. 2



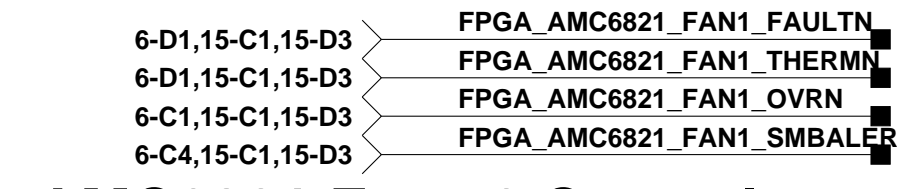
DAC5682 Control



AD9516 Control



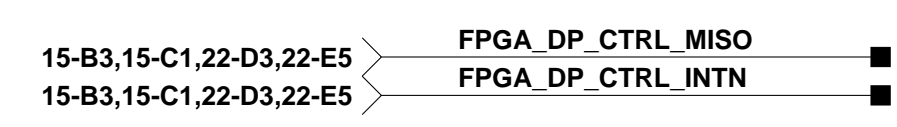
AMC6821 Fan #1 Control



AMC6821 Fan #2 Control



Data Path FPGA Control



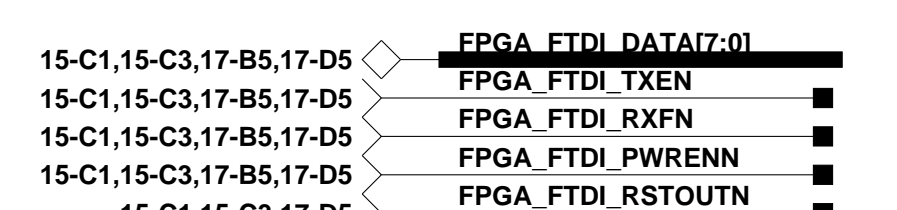
AsAP 1 Config Output



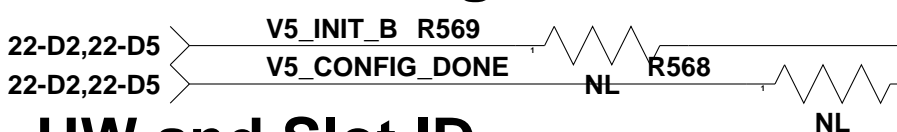
AsAP 2 Config Output



FT245BL USB Interface



Custom Configuration



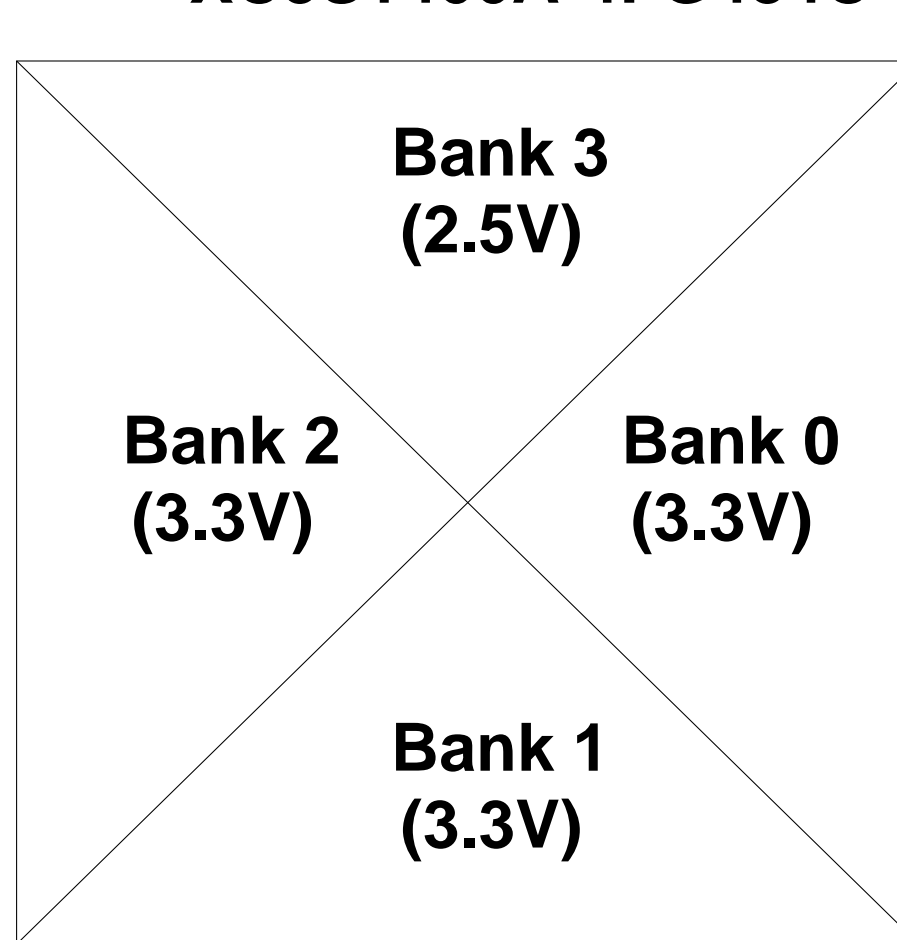
HW and Slot ID



Reach Display Interface

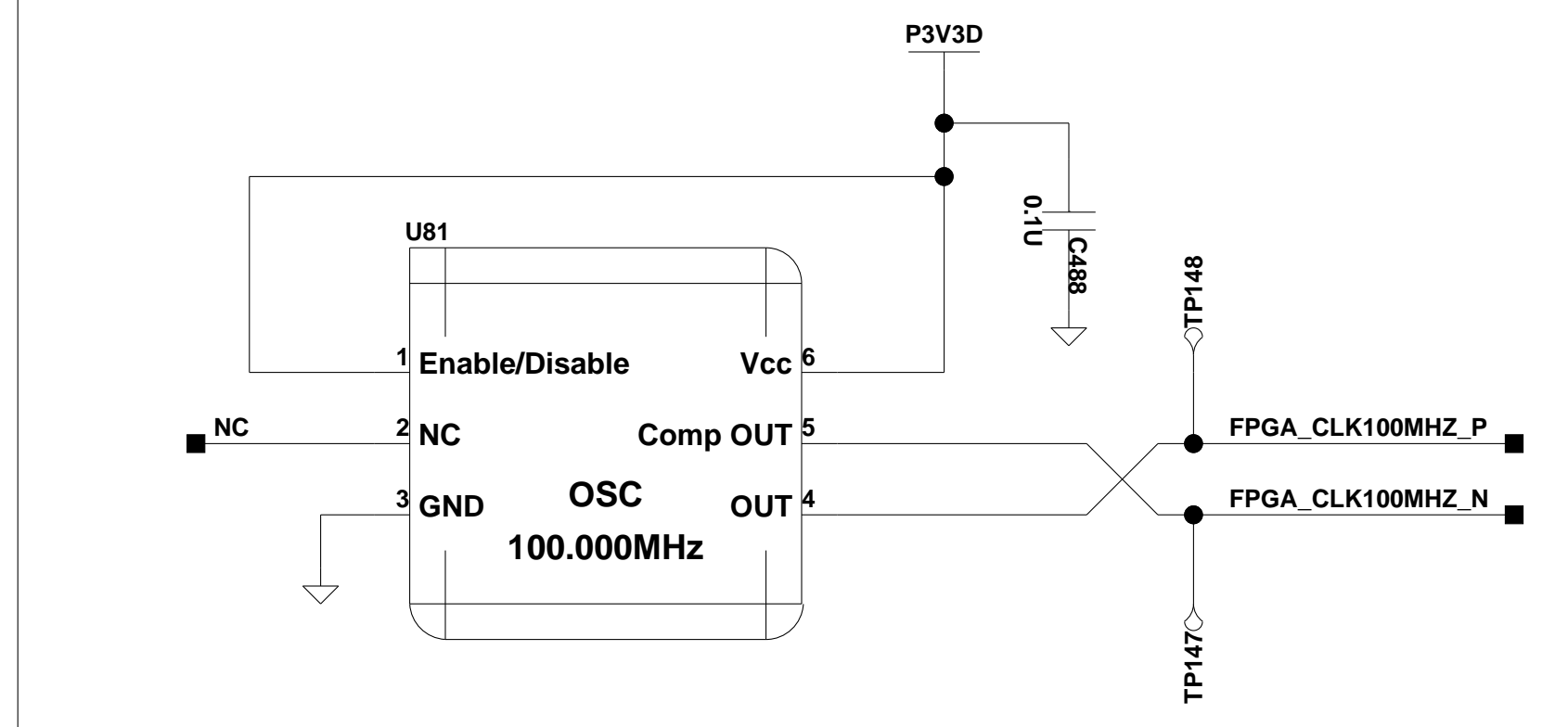


XC3S1400A-4FG484C

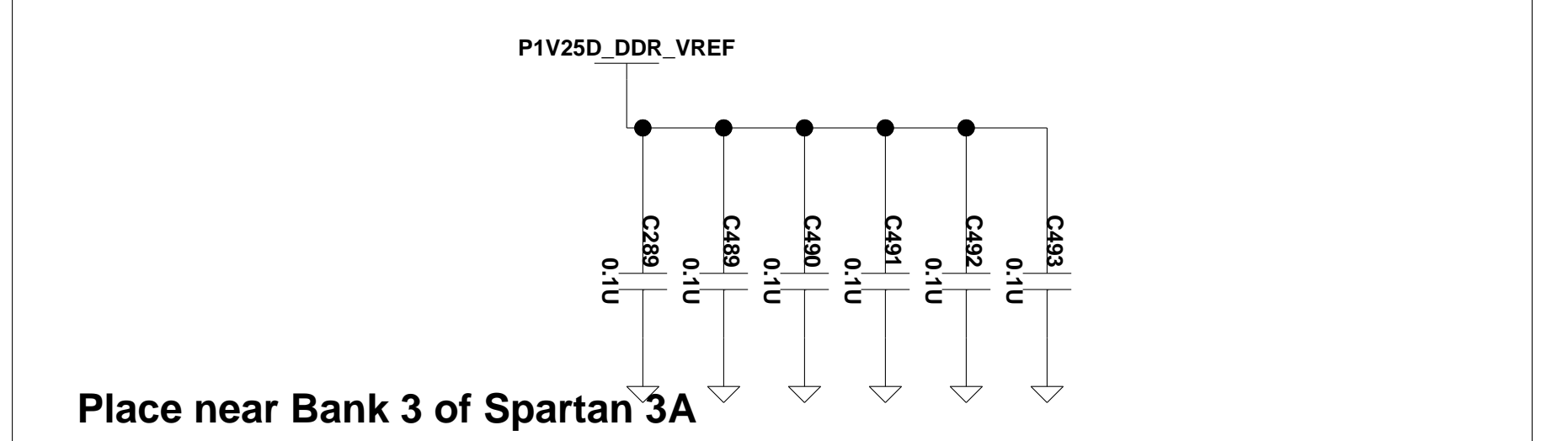


Bank 0 (3.3V): Clock Path FPGA/Logic Analyzer
 Bank 1 (3.3V): SPI Device Interfaces
 Bank 2 (3.3V): SPI Device Interfaces
 Bank 3 (2.5V): uBlaze SDRAM

B 100MHz Digital Clock



C VREF Decoupling Capacitors



*** OUTPUTS ***

DDR SDRAM Interface



Custom Configuration



CPU Interrupts



Logic Analyzer Clk/Data



10MHz Clock Control



USB to RS-232 Interface



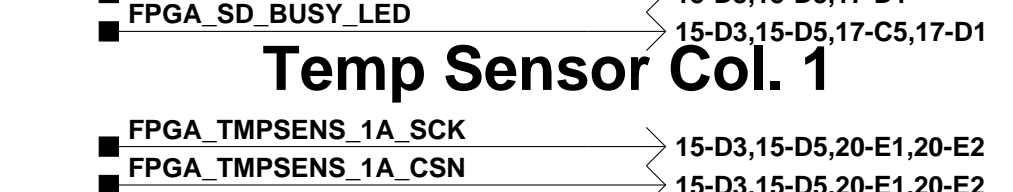
Debug LEDs



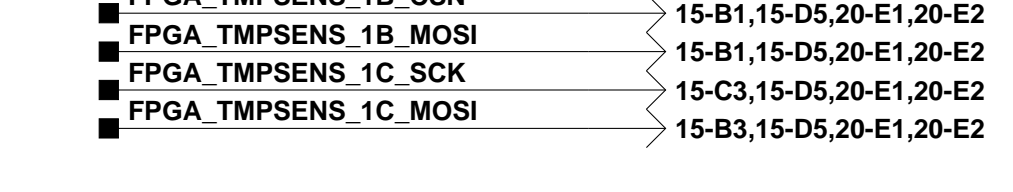
MicroSD Interface



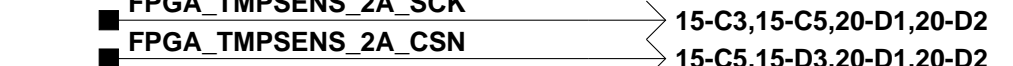
Temp Sensor Col. 1



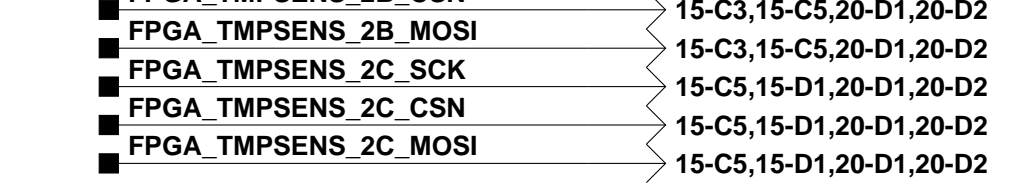
Temp Sensor Col. 2



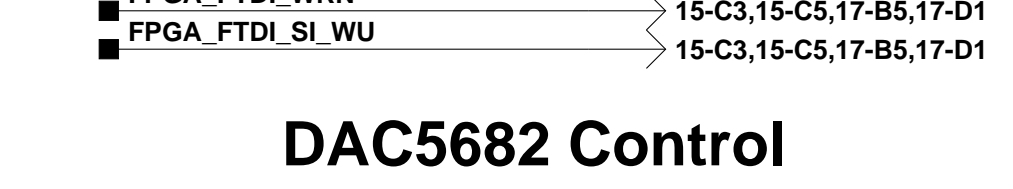
FT245BL USB Interface



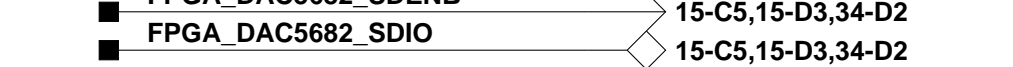
DAC5682 Control



AD9516 Control



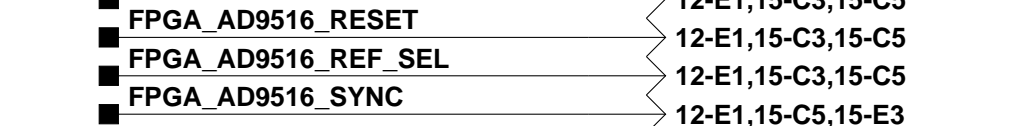
DDR2 SDRAM SODIMM Control



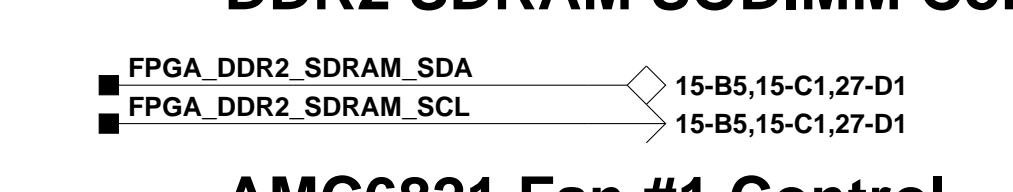
AMC6821 Fan #1 Control



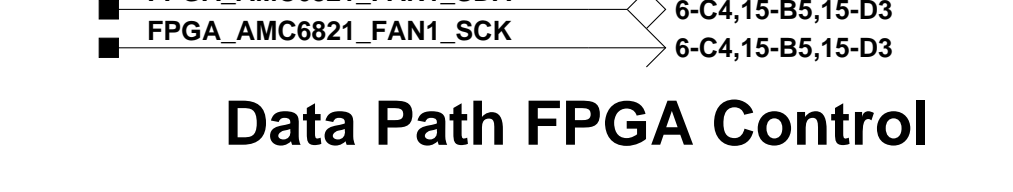
Data Path FPGA Control



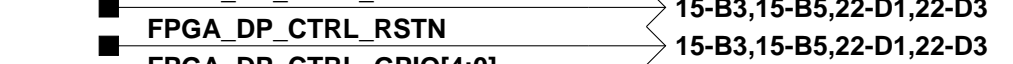
AsAP 1 Config Input



AsAP 2 Config Input



Reach Display Interface

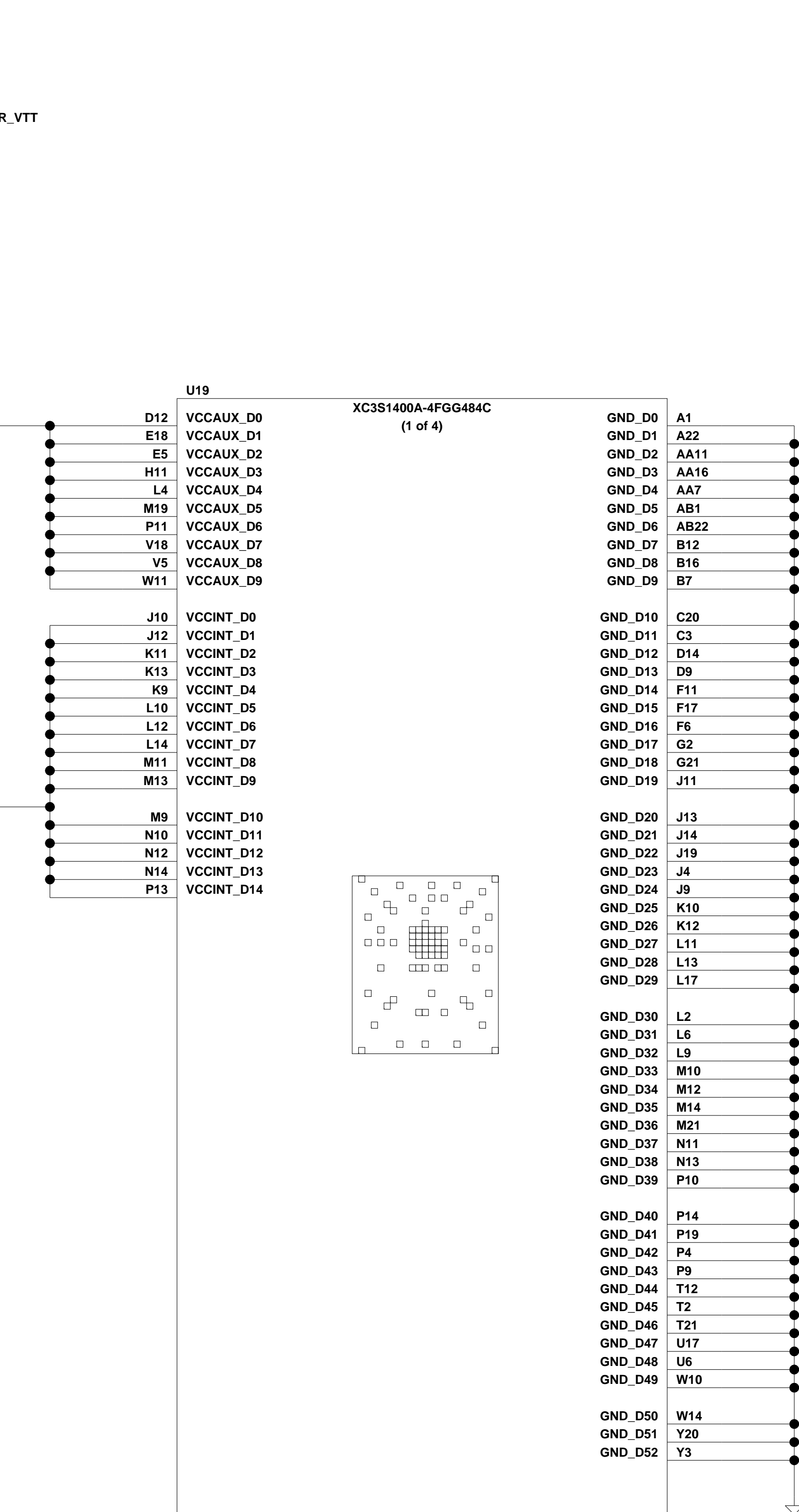
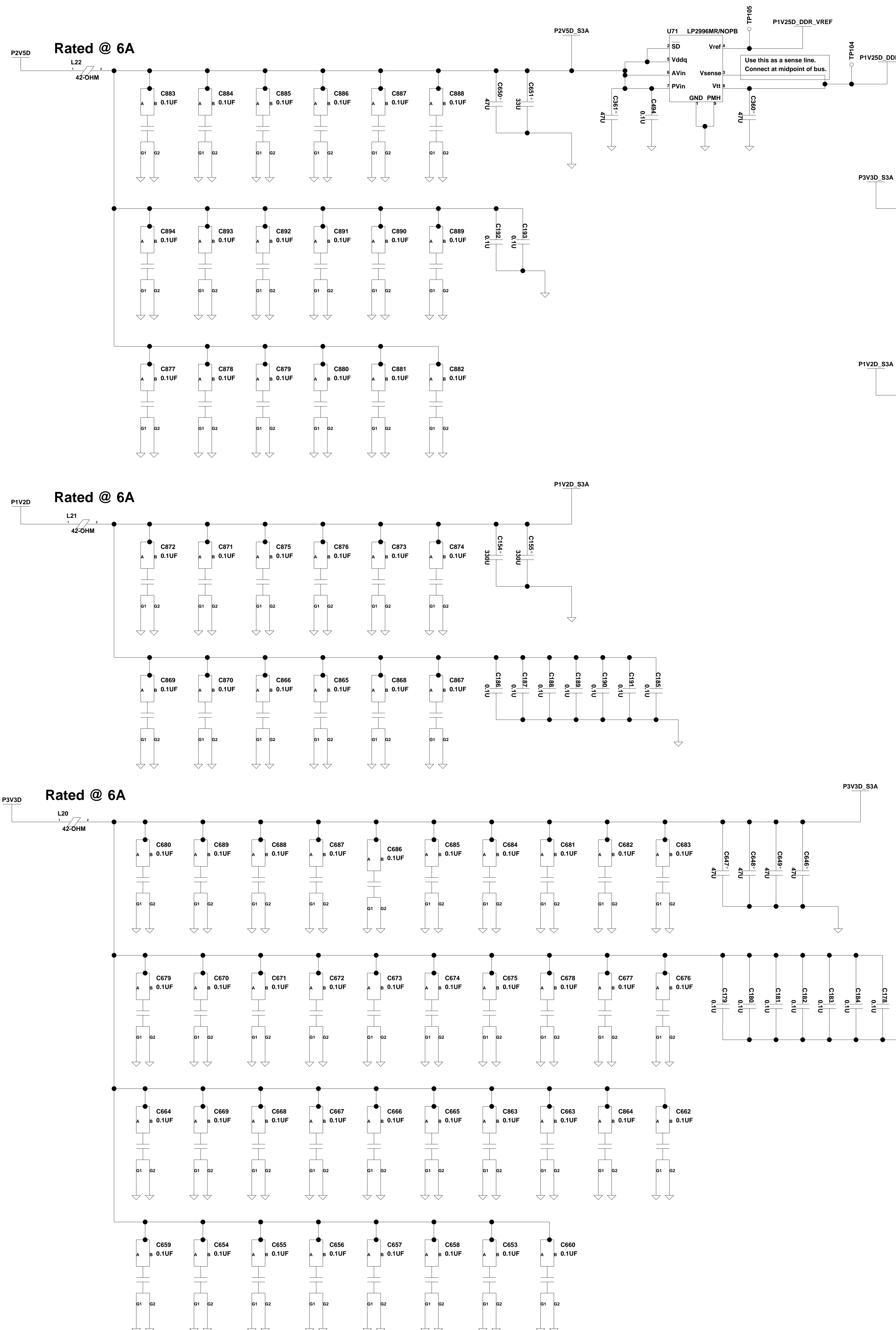


VLSI Computation LAB

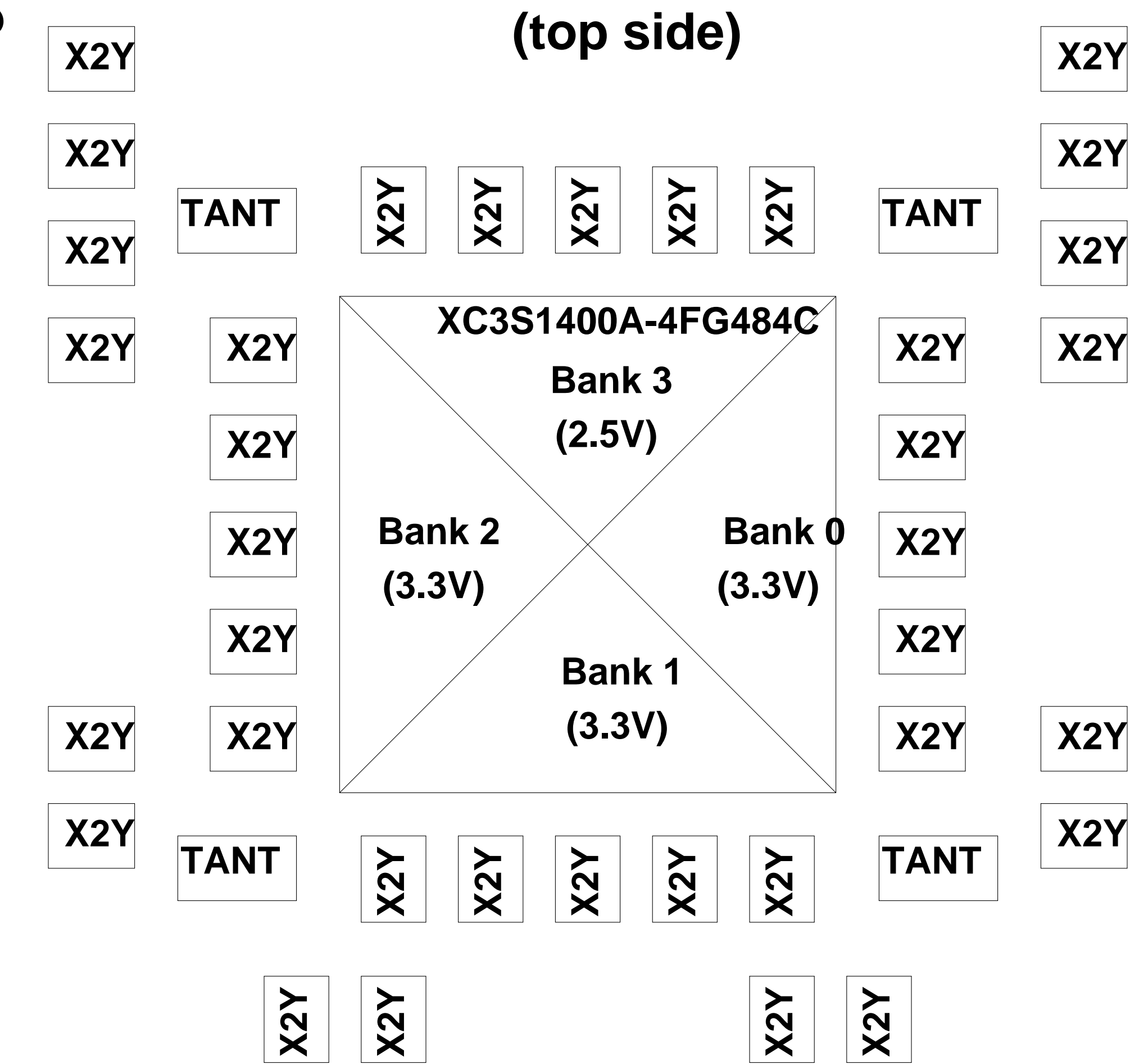
Title: XILINX SPARTAN-3A CONTROL FPGA I/O
 File: MEAS_MAIN_BOARD
 Created by: JEREMY W. WEBB
 Modified by: JEREMY W. WEBB
 PCB NO: 342

Date: 4-20-2009 13:35
 Date: JEREMY W. WEBB
 Size: E Sheet 15 of 43 REV: 001

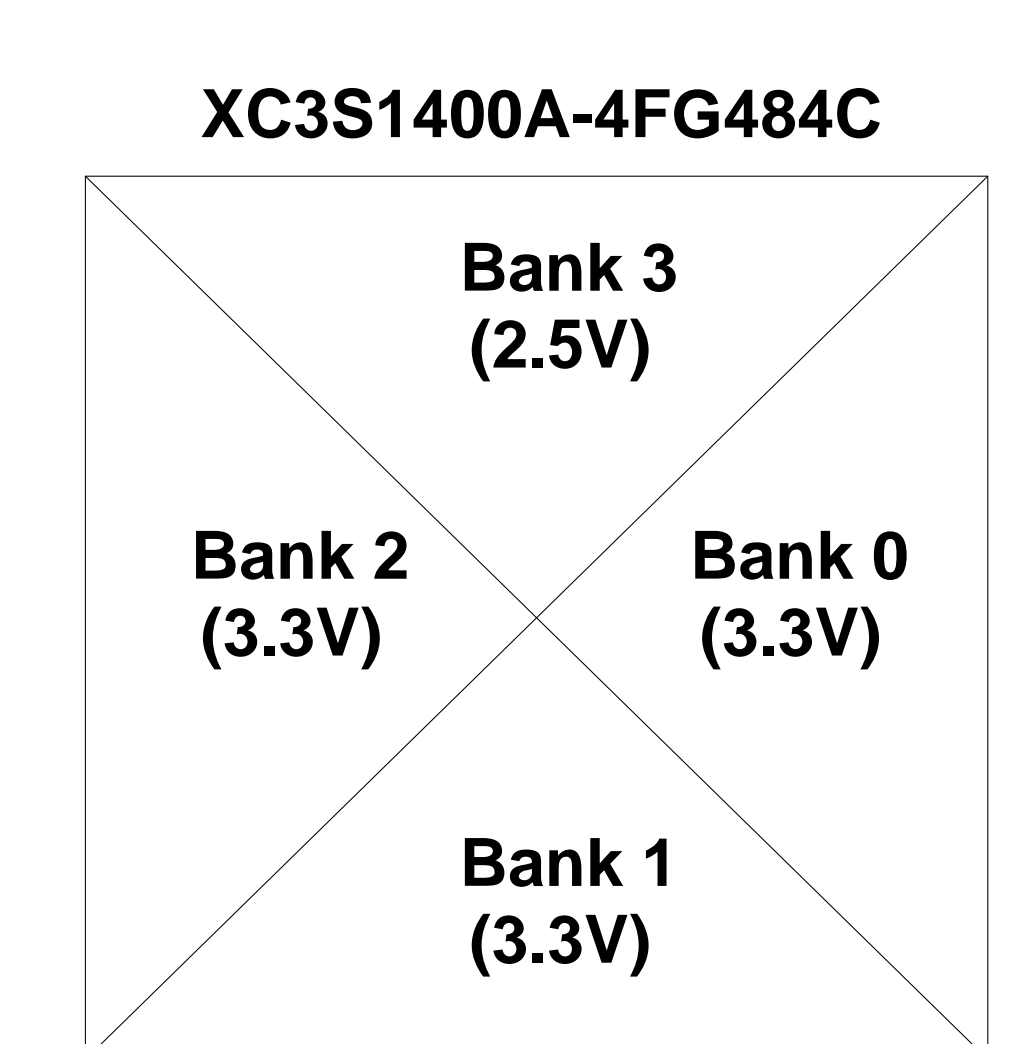
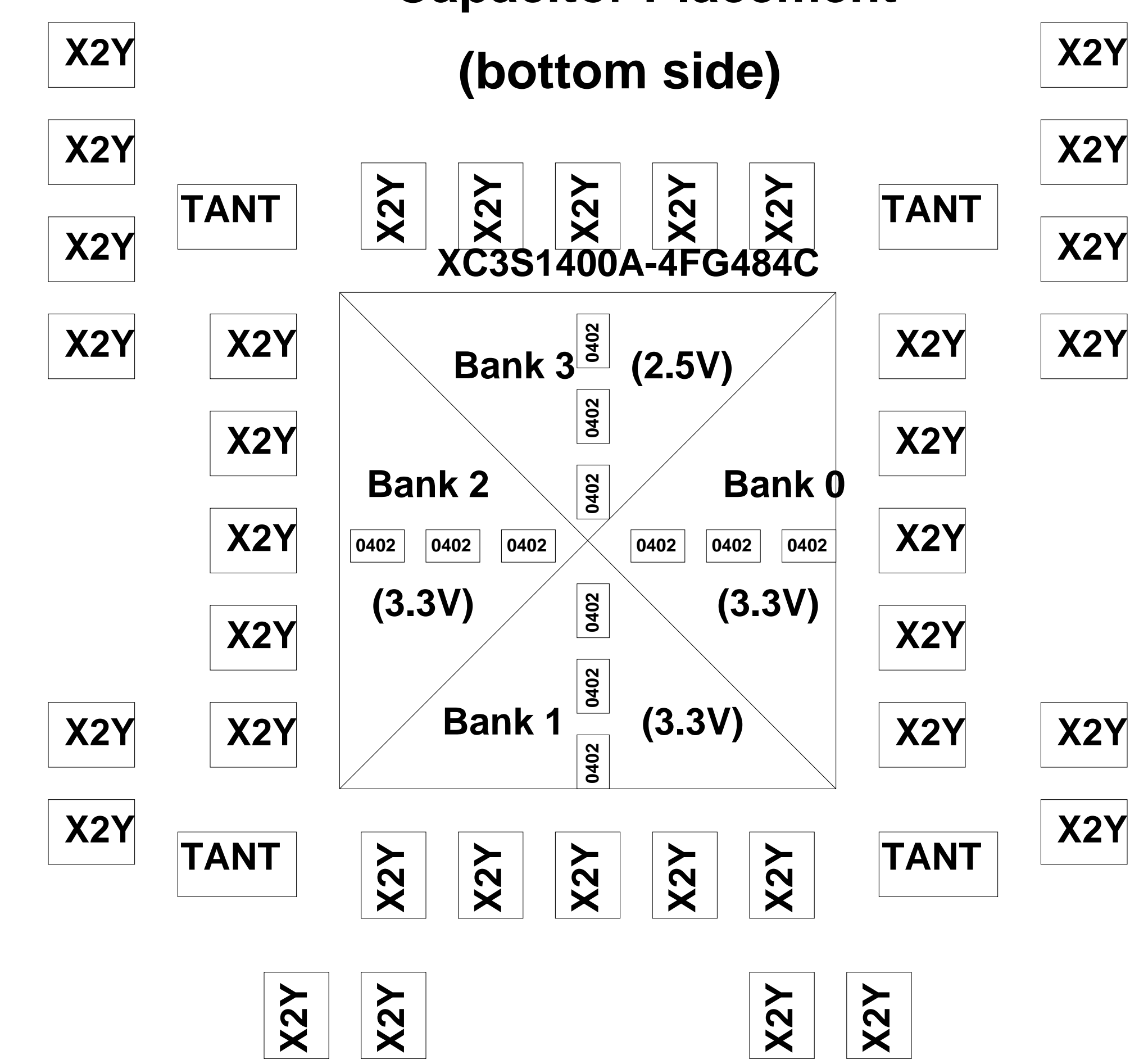
Xilinx Spartan-3A Control FPGA Power Supplies



Capacitor Placement (top side)

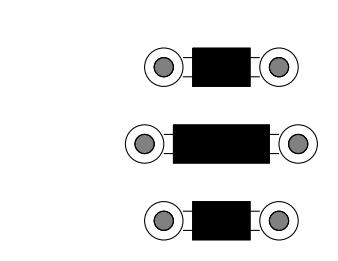


Capacitor Placement (bottom side)

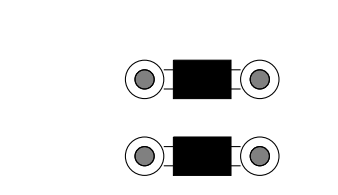


Bank 0 (3.3V): UI, 10MHz, LEDs, ...
 Bank 1 (3.3V): SPI Device Interfaces
 Bank 2 (3.3V): FTDI, AsAP #2, microSD, Fan Ctrl, ...
 Bank 3 (2.5V): uBlaze SDRAM

X2Y Capacitor Via Placement



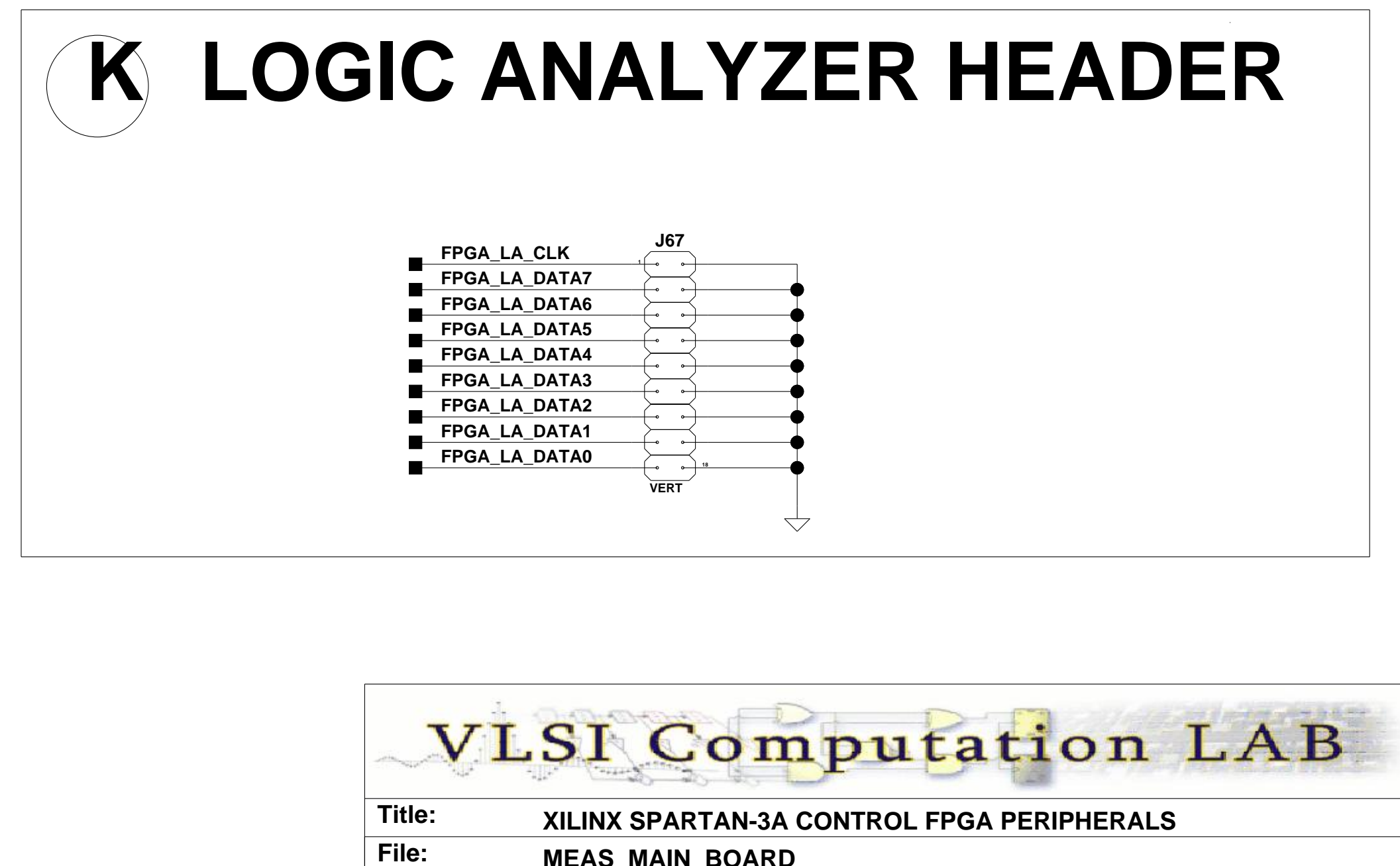
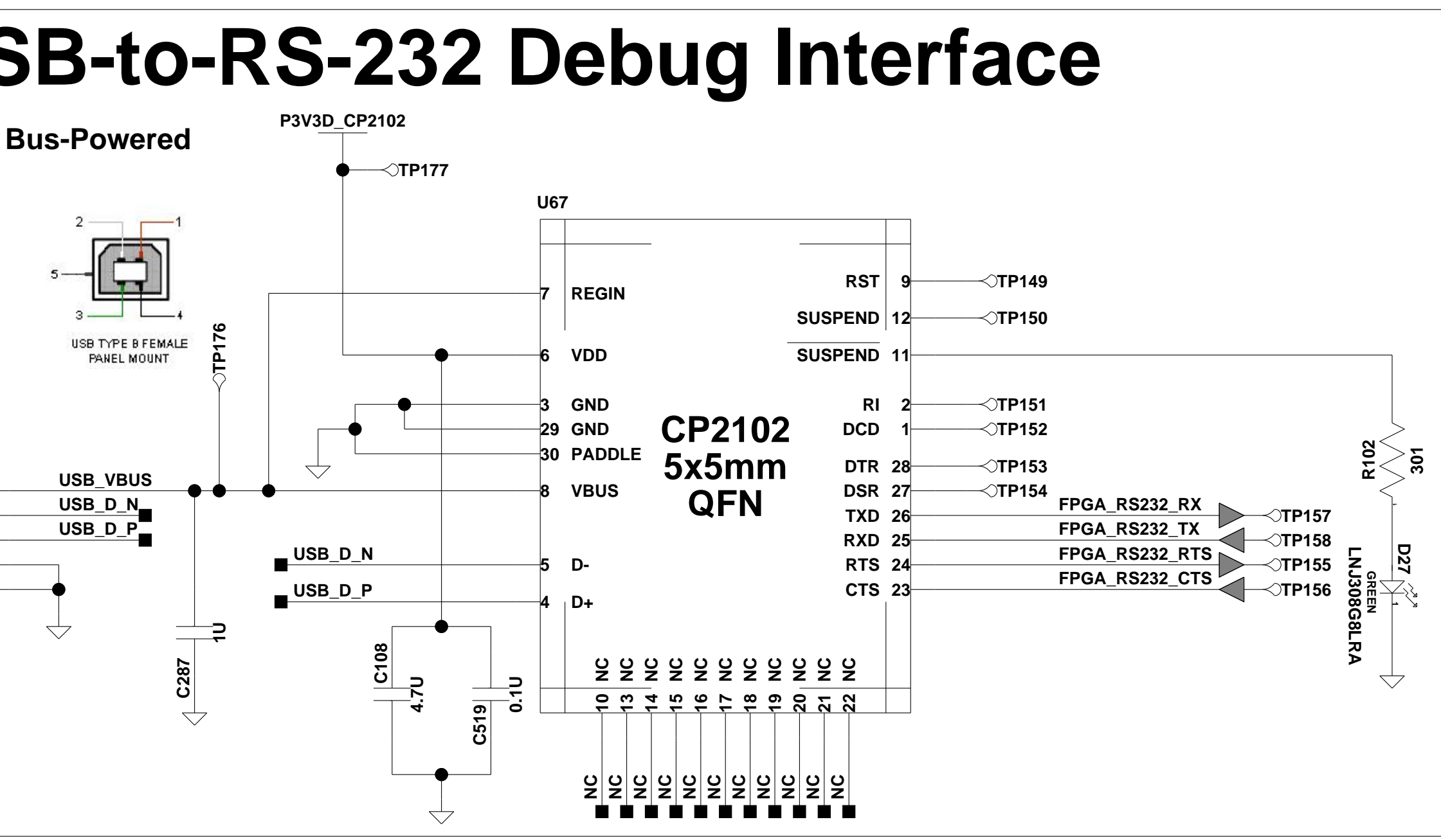
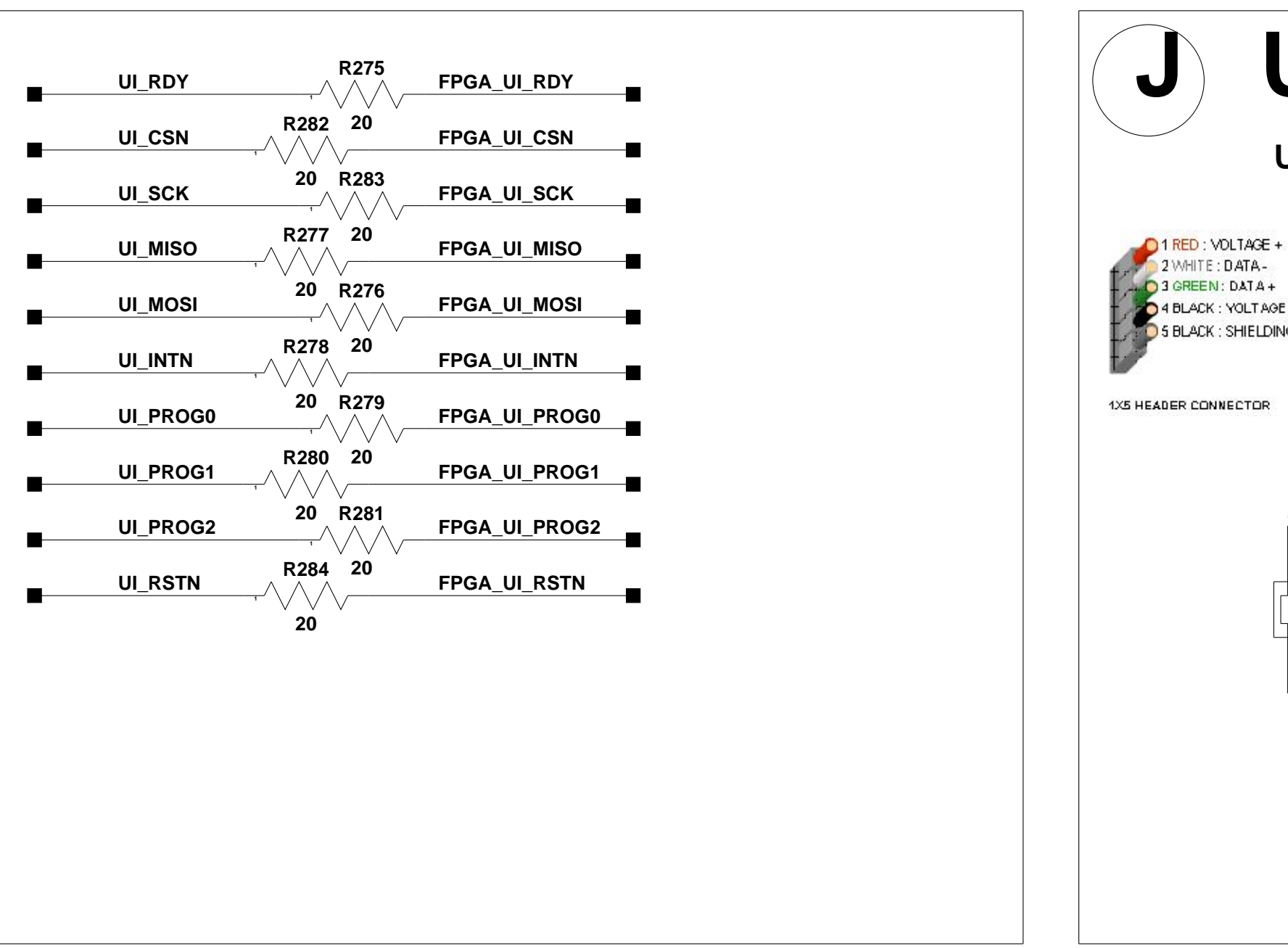
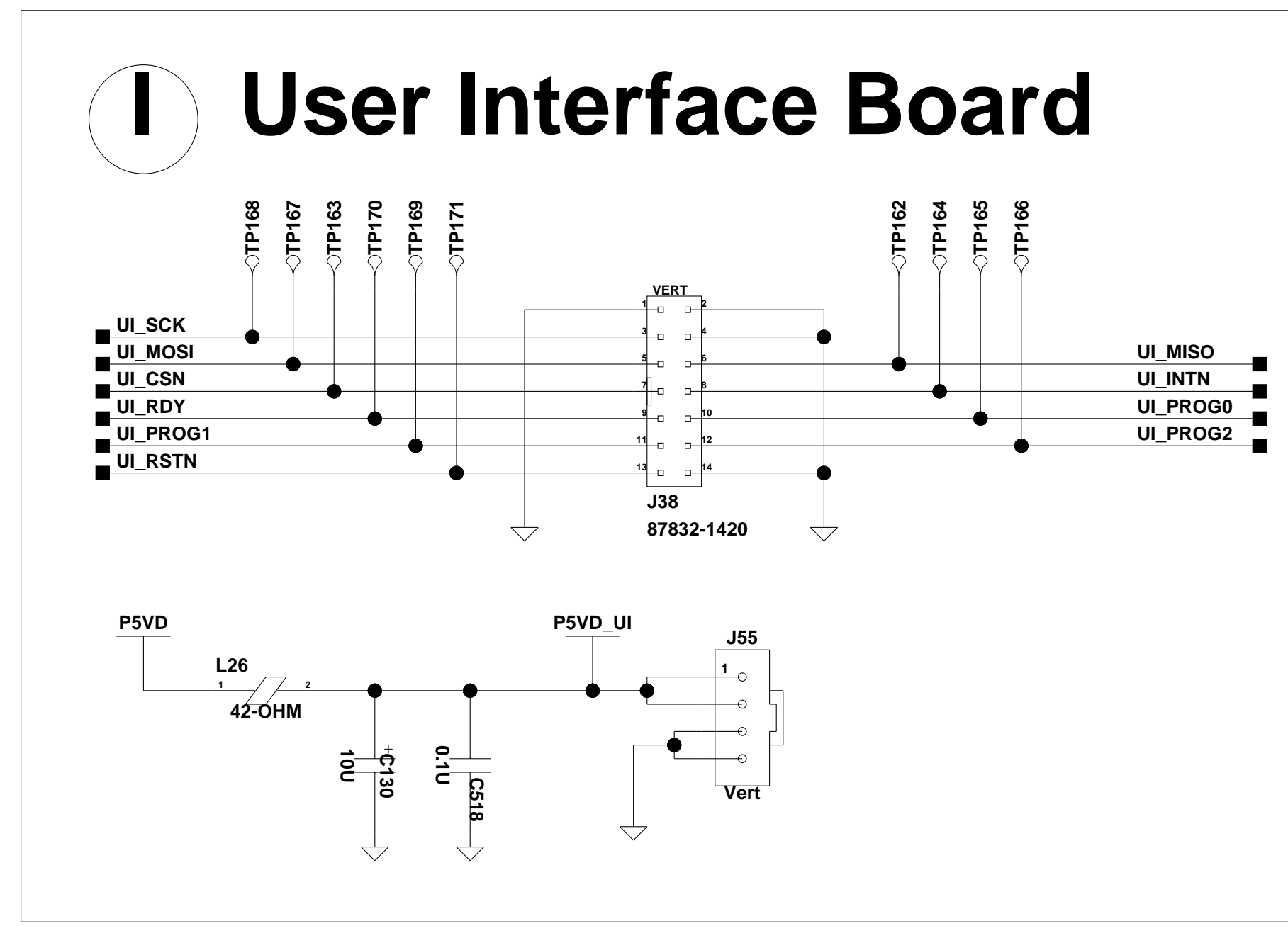
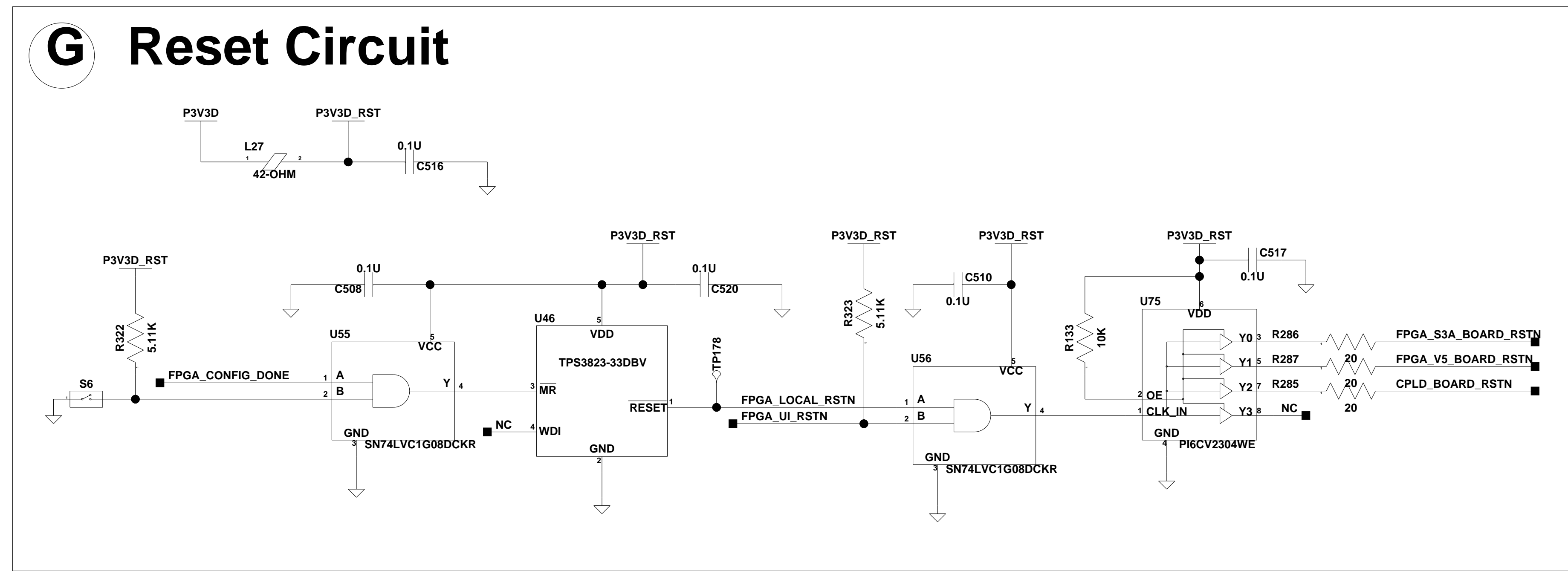
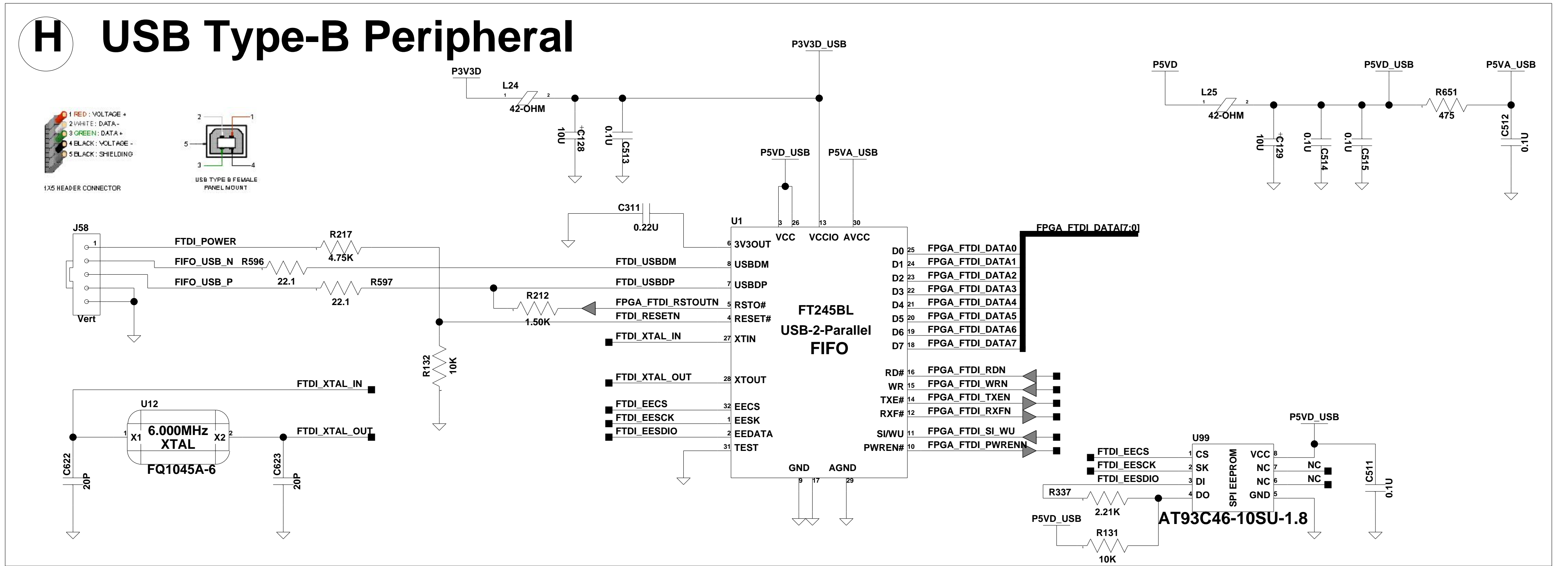
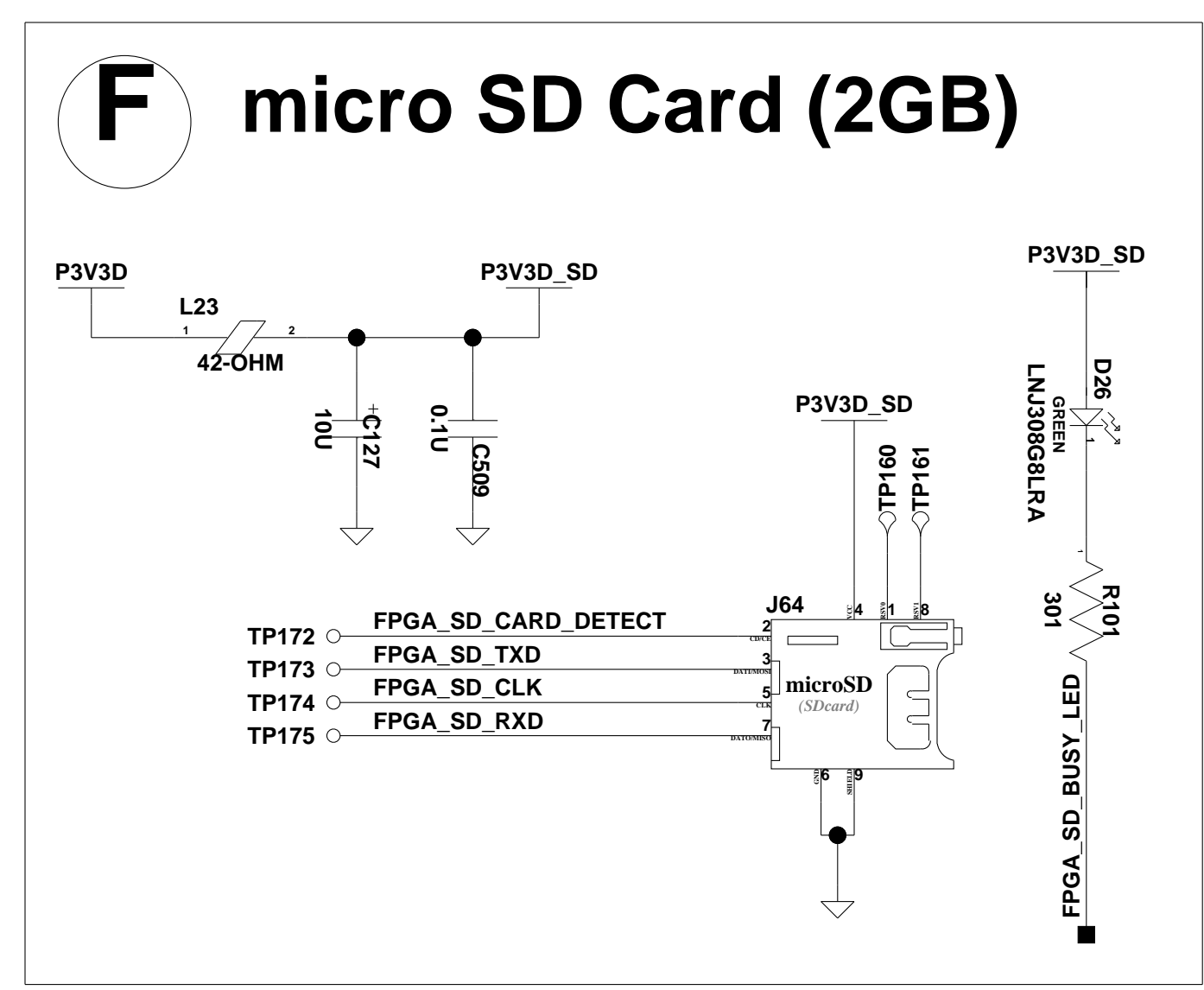
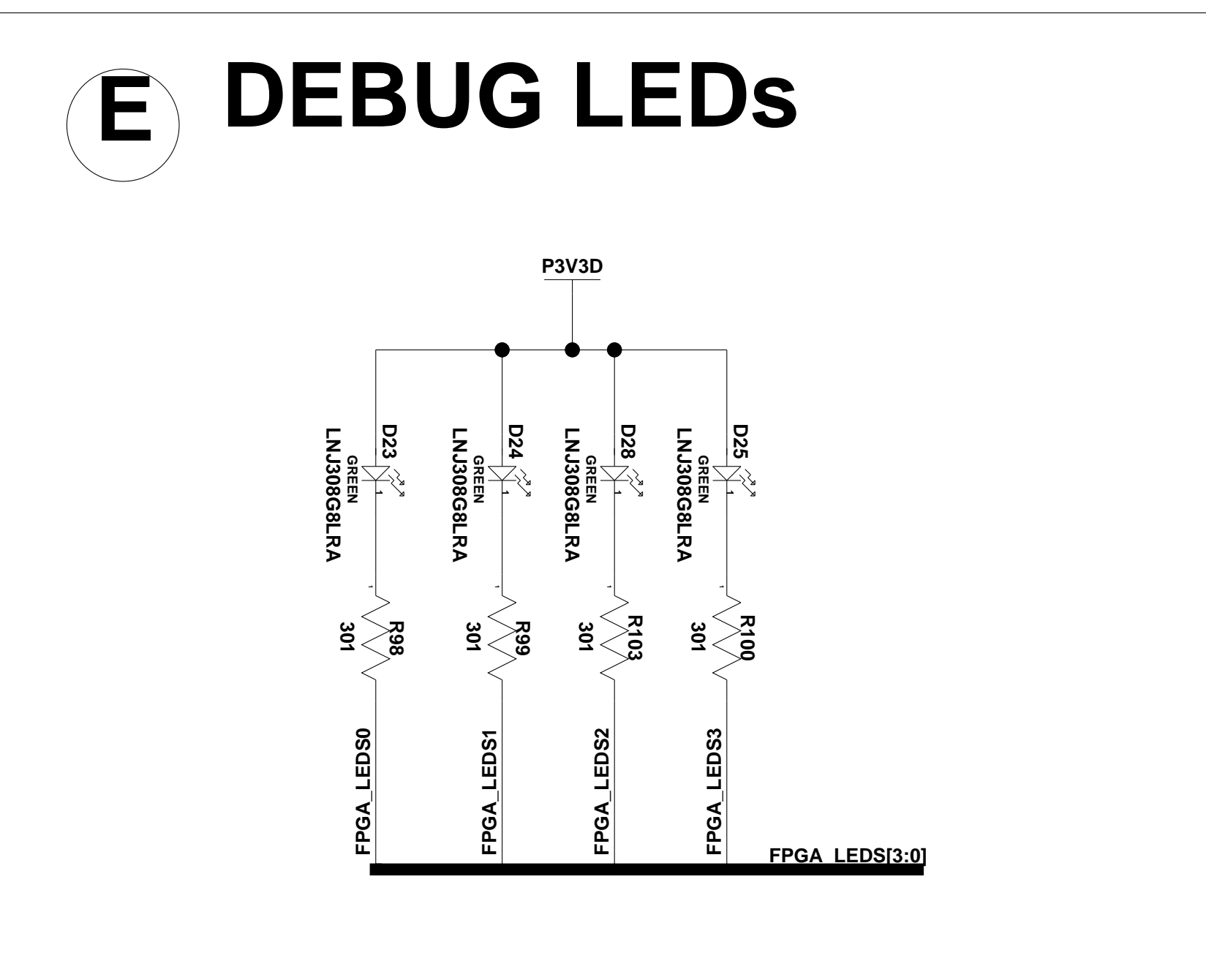
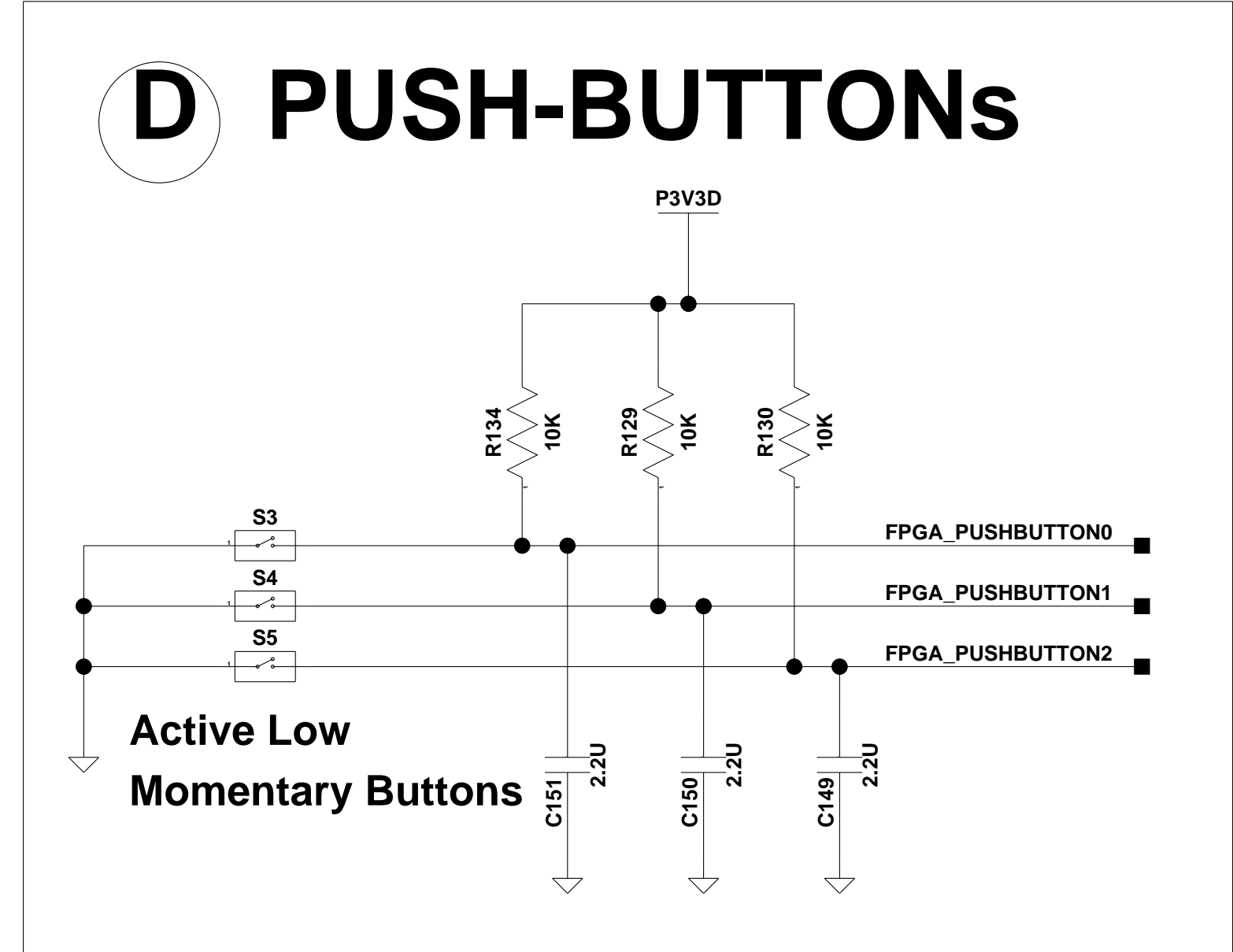
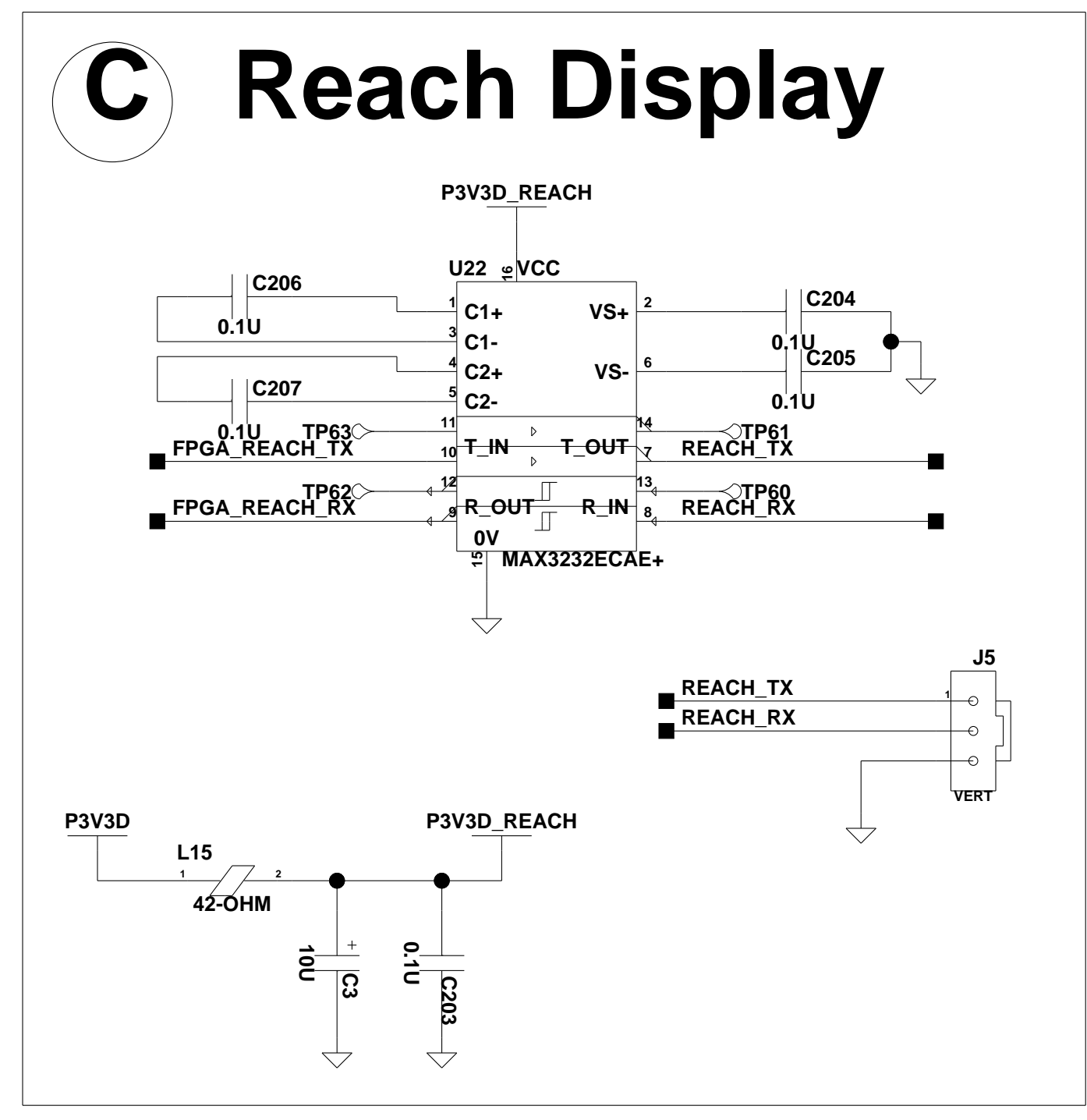
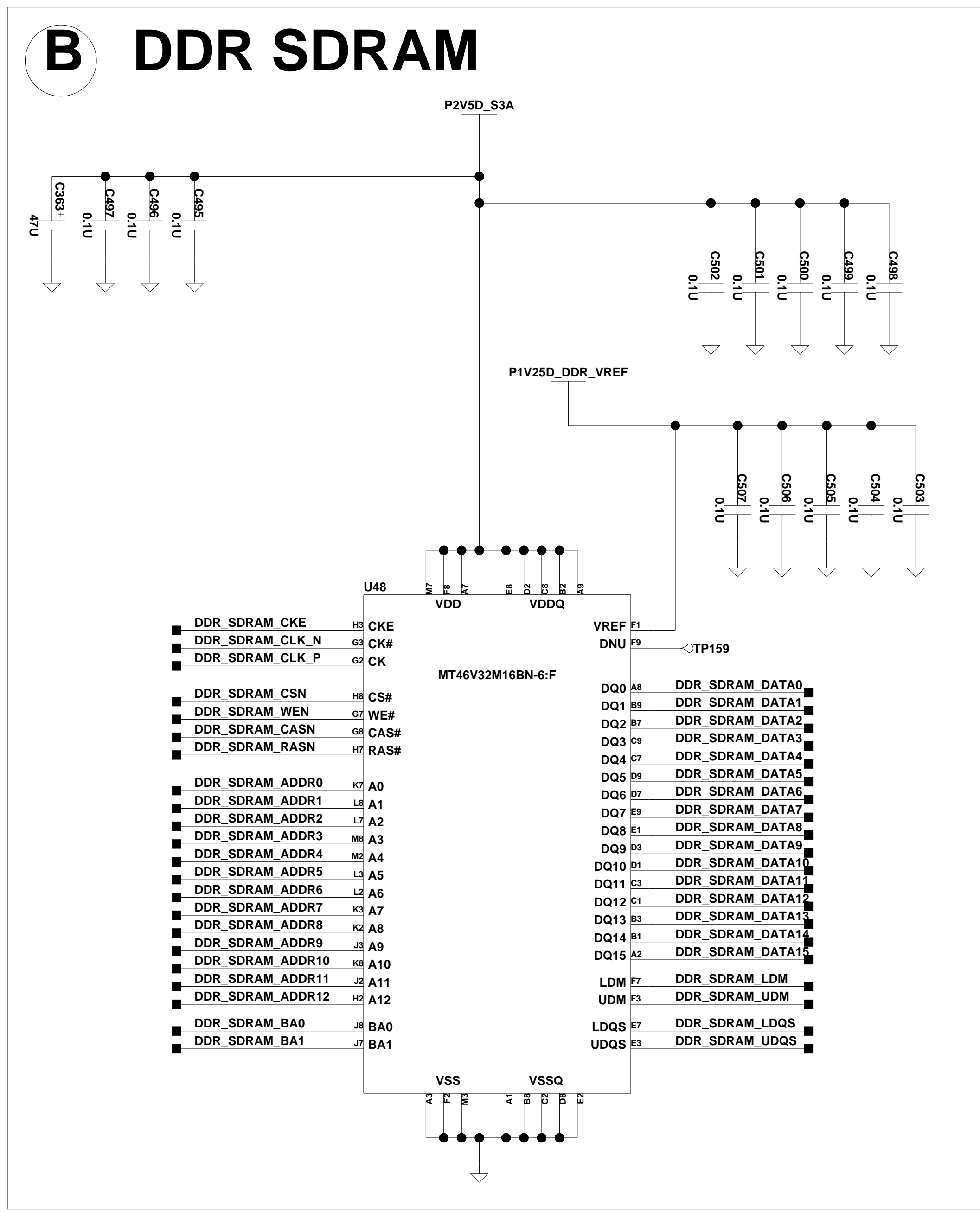
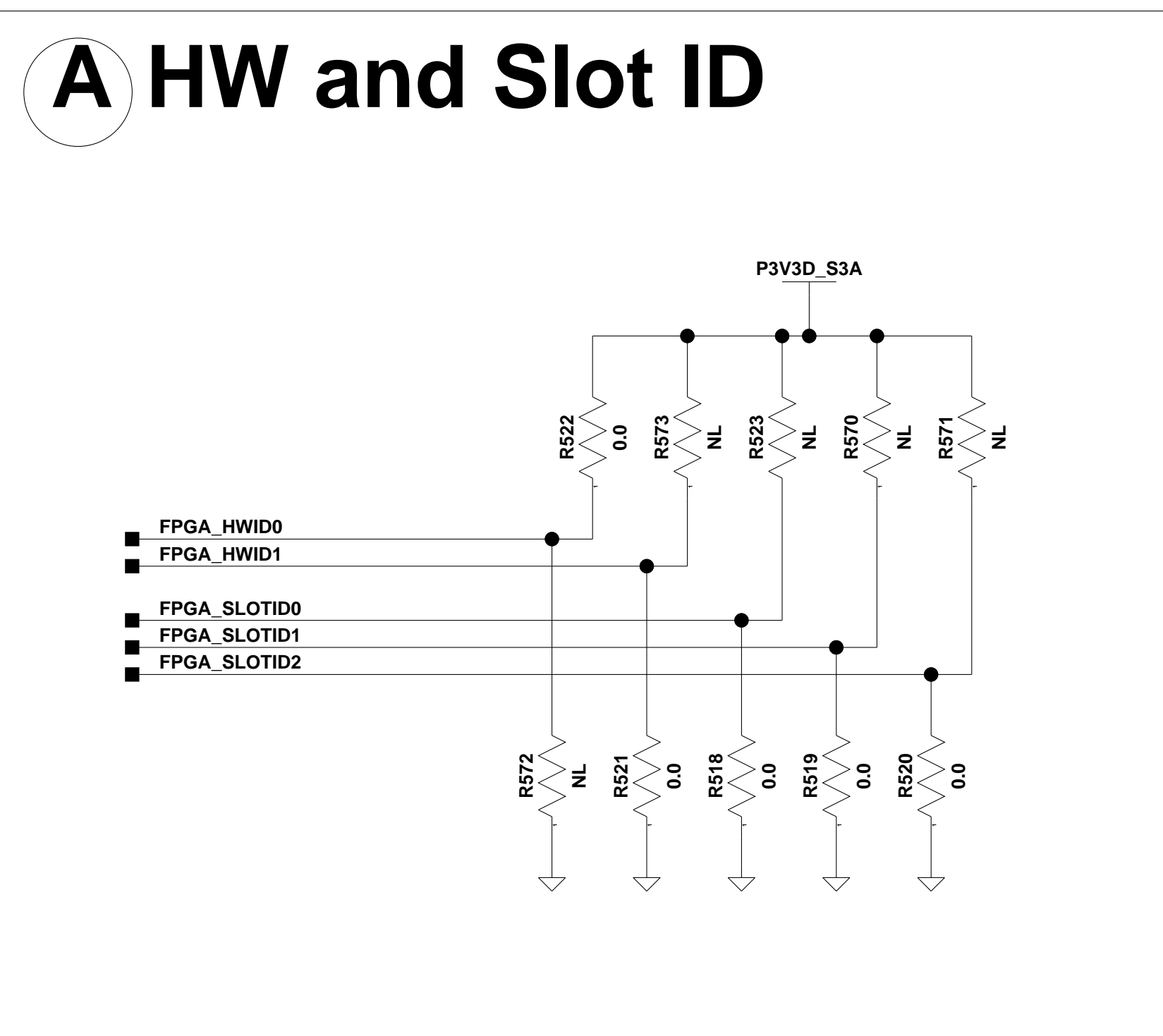
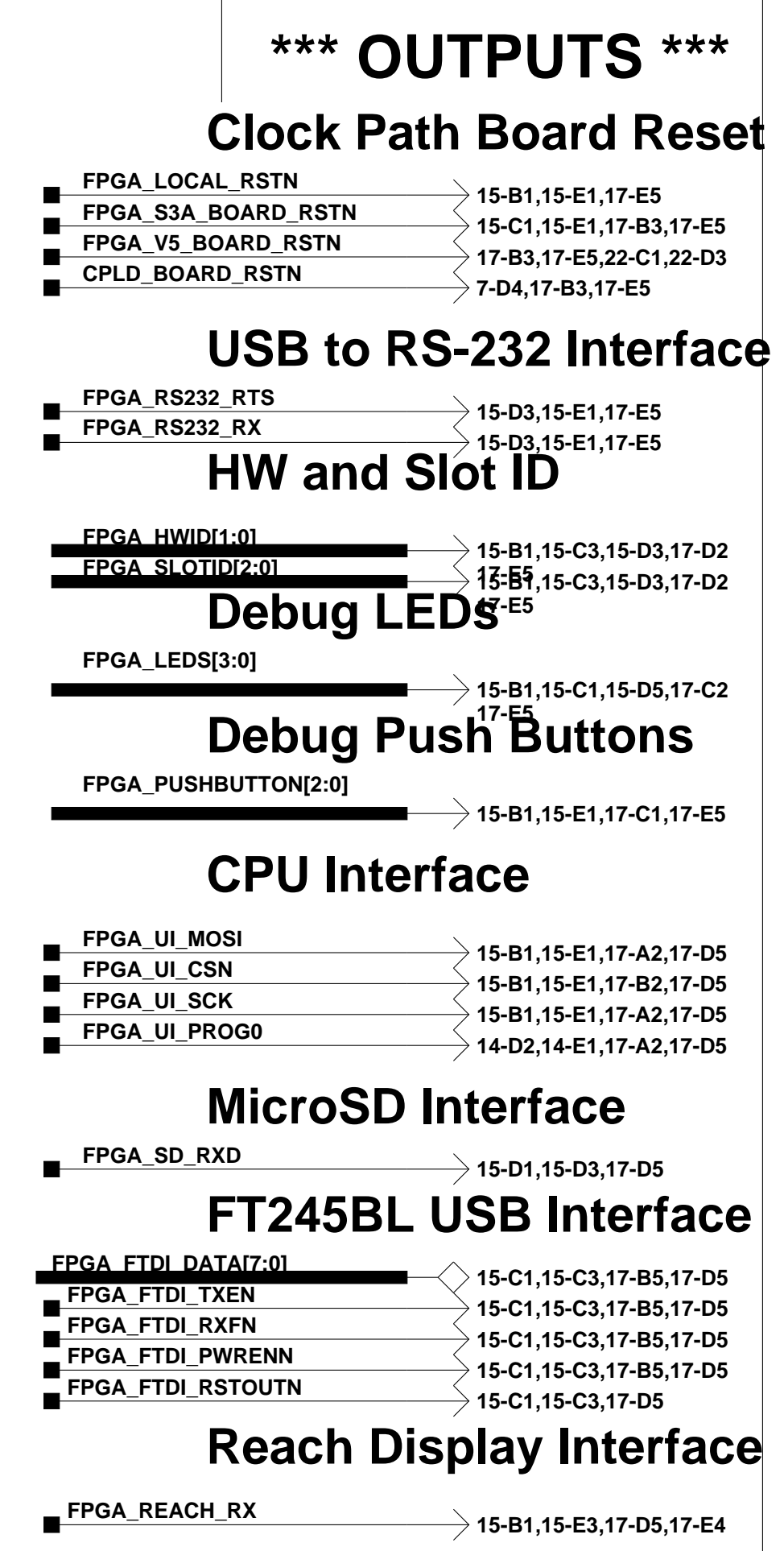
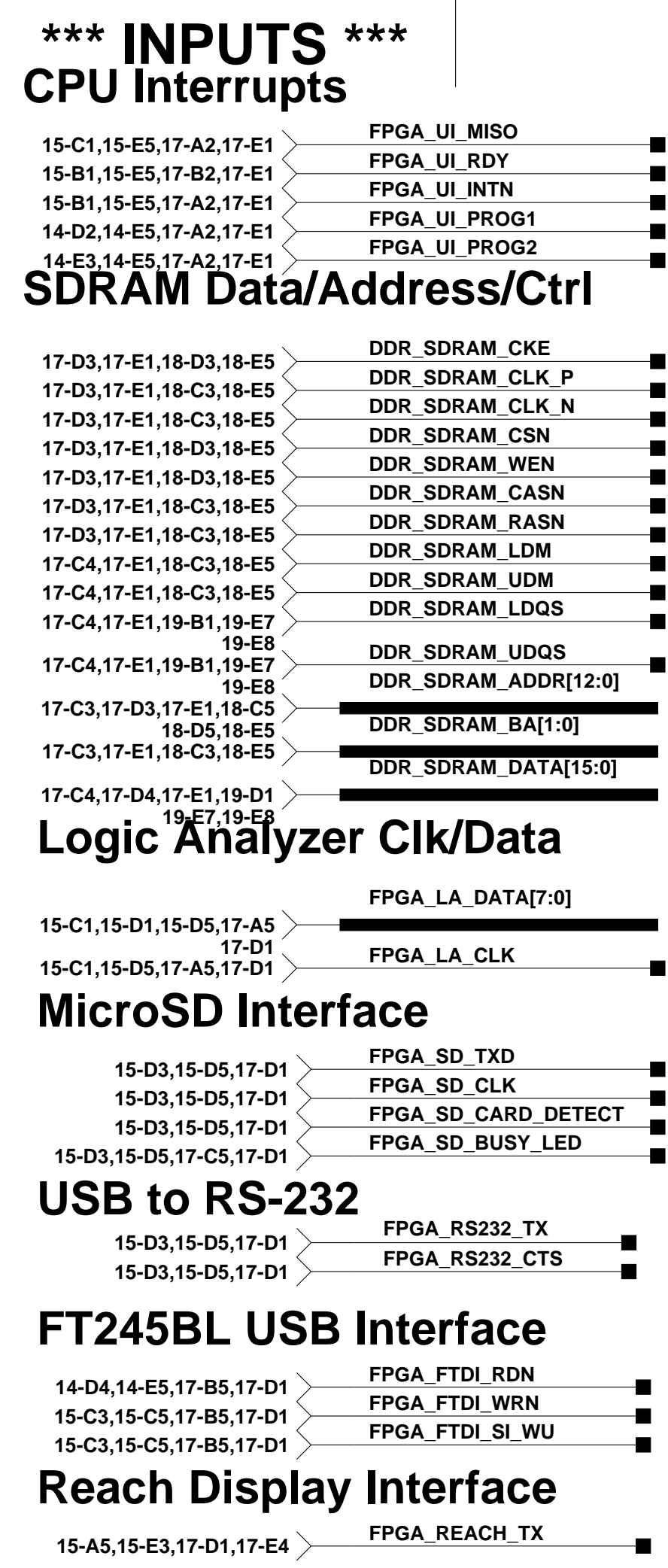
Tantalum/O402 Via Placement



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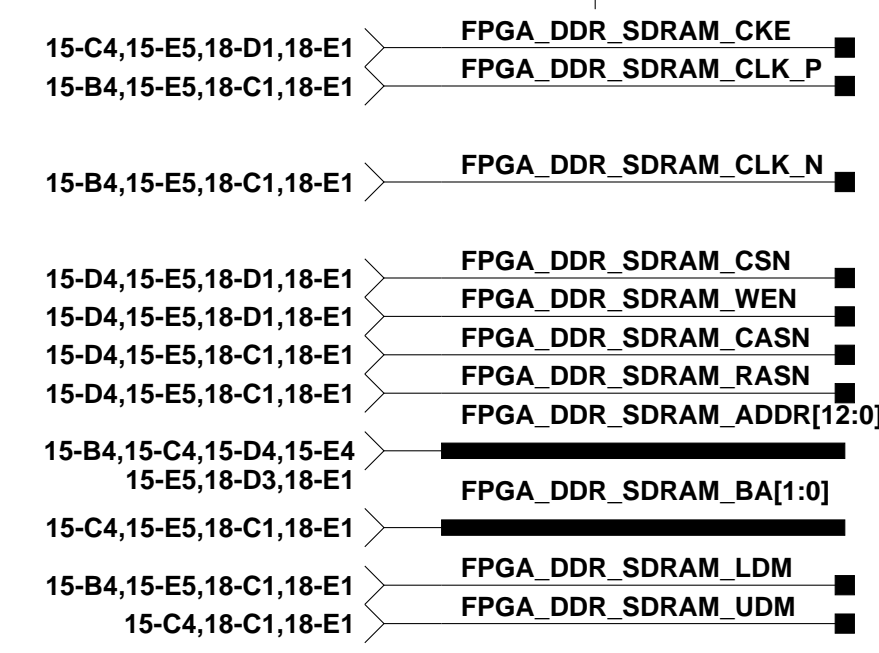
Title:	XILINX SPARTAN-3A CONTROL FPGA POWER SUPPLIES		
File:	MEAS_MAIN_BOARD		
Created by:	JEREMY W. WEBB	Date:	3-27-2009 12:24
Modified by:		Date:	
PCB NO:	342	Size:	E
Sheet	16	of	43
REV:	001		

Xilinx Spartan-3A Control FPGA Peripherals

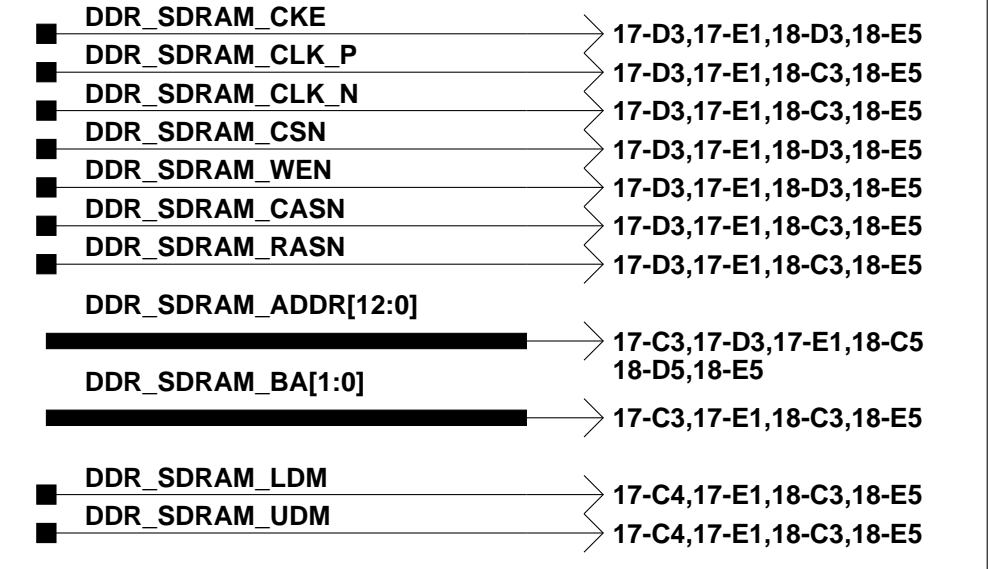


DDR SDRAM Address and Control Terminations

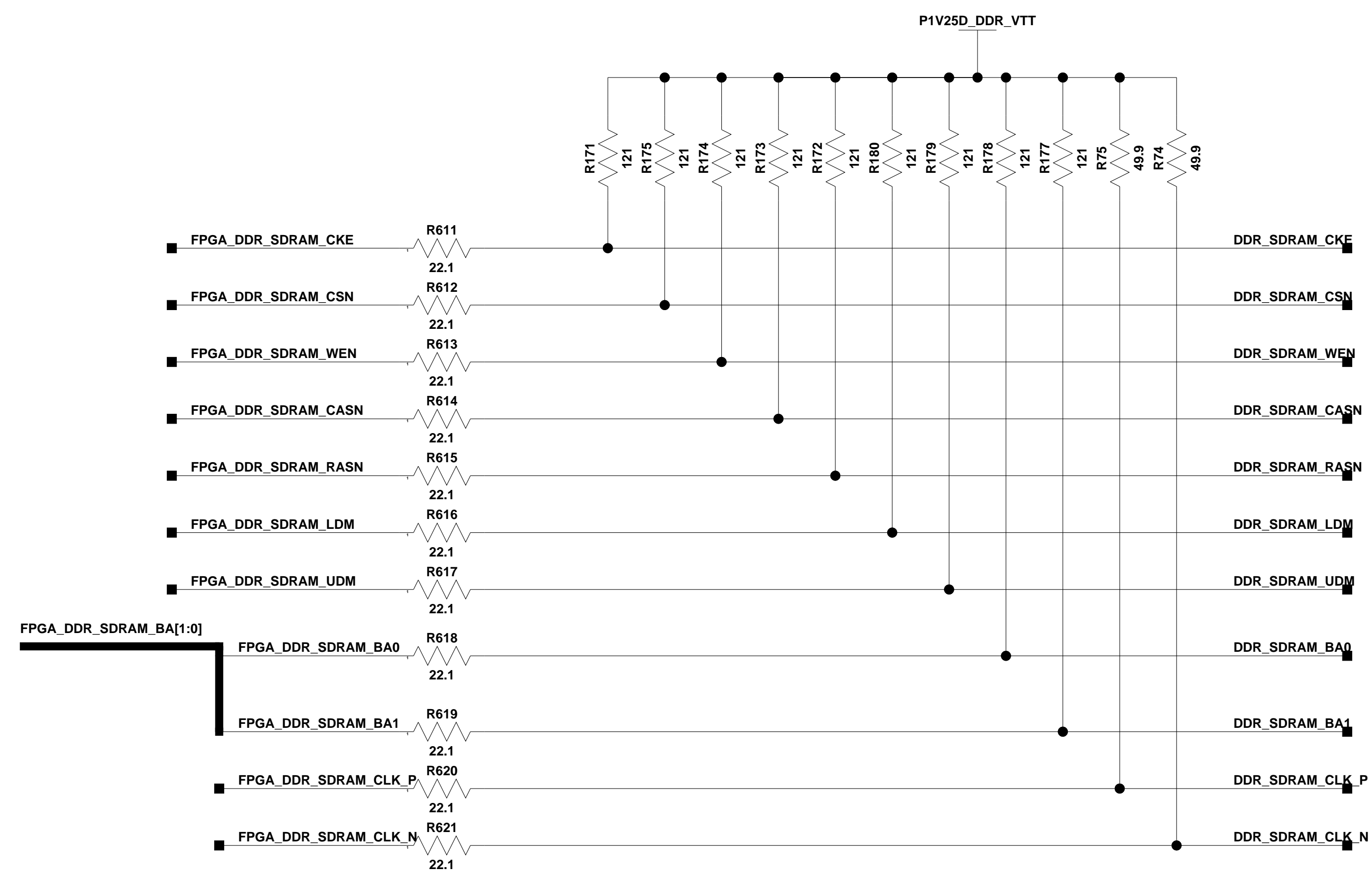
*** INPUTS ***



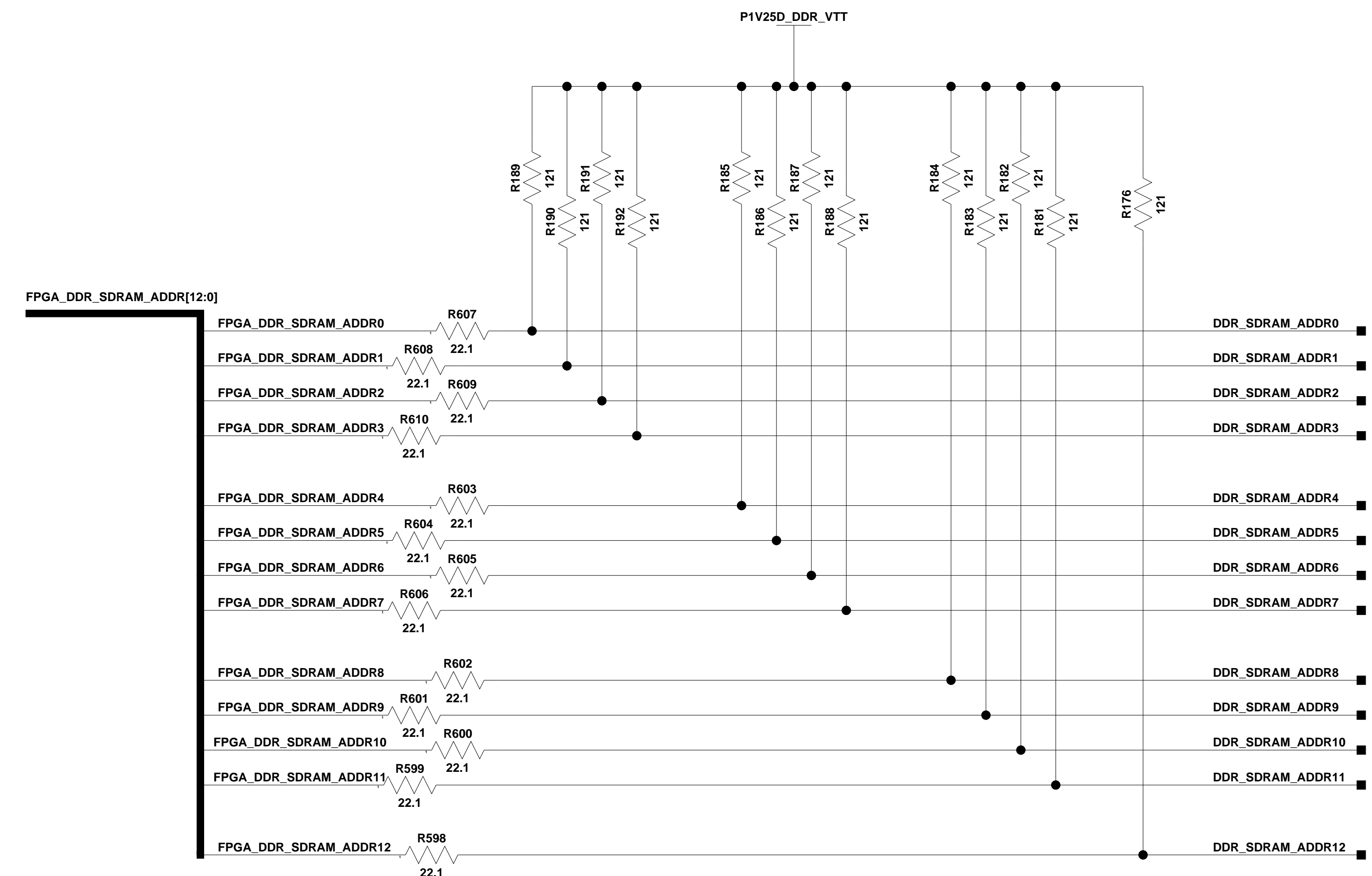
*** OUTPUTS ***



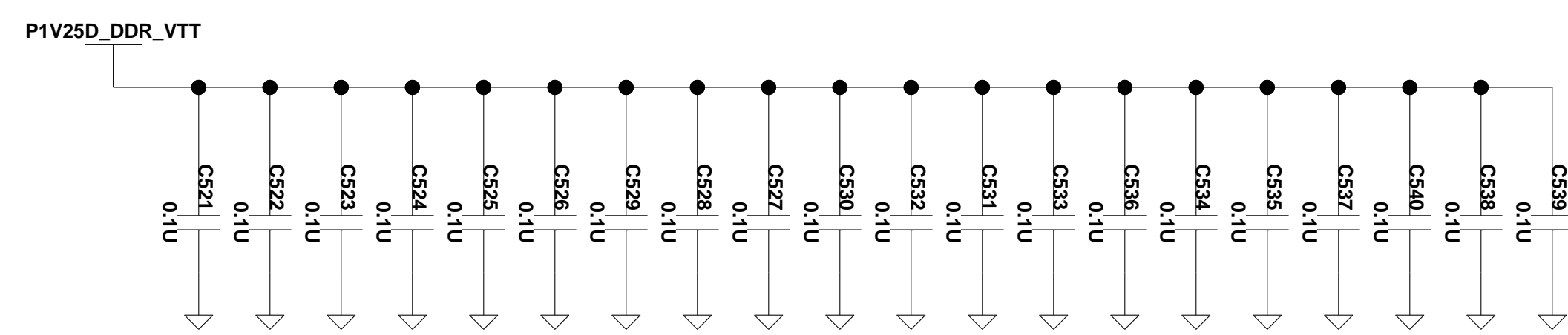
A DDR SDRAM Control Terminations



B DDR SDRAM Address Terminations



C VTT Termination Decoupling Capacitors



Place near DDR SDRAM Terminations

Address/Control Termination Placement:

Place parallel terminations just beyond the SDRAM.

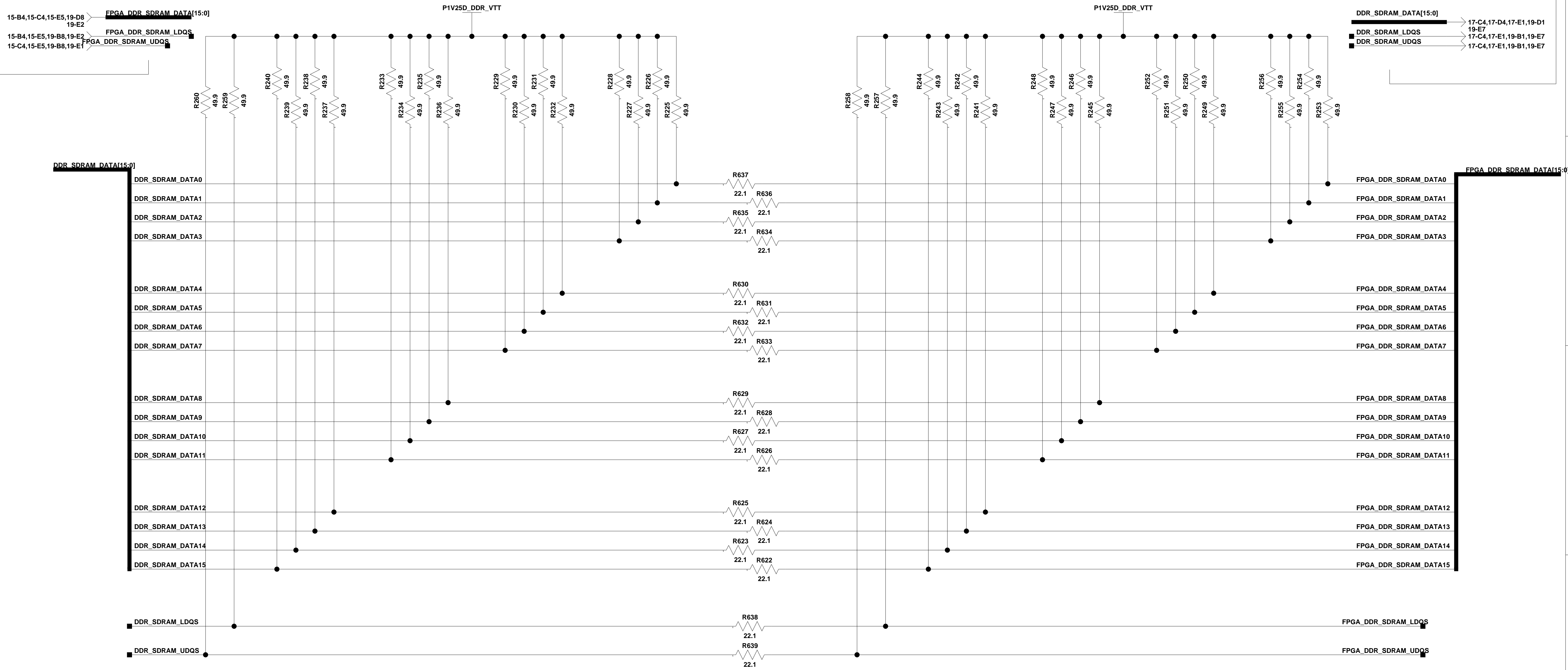
Place the series terminations close to the Spartan 3A FPGA



*** INPUTS ***

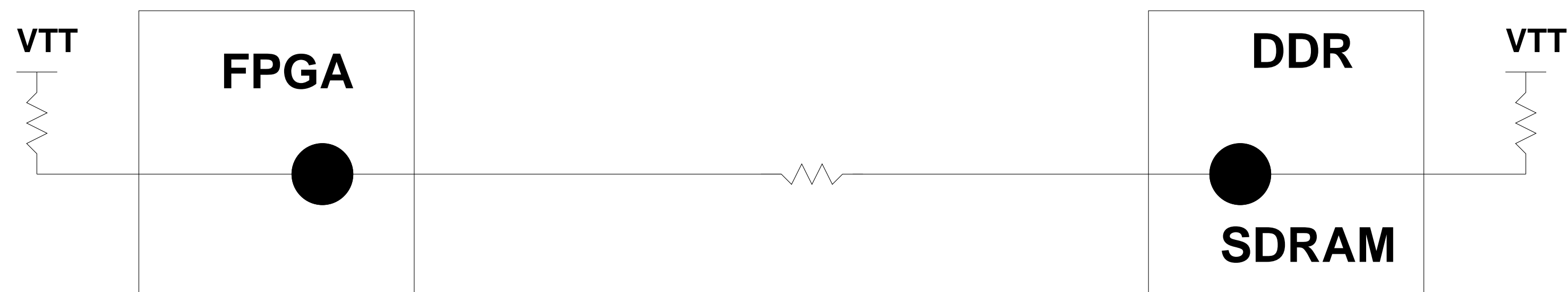
*** OUTPUTS ***

DDR SDRAM Data Terminations



Data/DQS Termination Placement:

Place parallel terminations just beyond the SDRAM and FPGA.
Place the series terminations in between the Spartan 3A FPGA and SDRAM



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VLSI Computation LAB			
Title: DDR SDRAM DATA TERMINATIONS			
File: MEAS_MAIN_BOARD			
Created by: JEREMY W. WEBB	Date: 4-20-2009_13:35		
Modified by:	Date:		
PCB NO: 342	Size: D	Sheet 19 of 43	REV: 001

Digital Temperature Sensors

*** INPUTS ***

Temp Sensor Col. 1

15-D3,15-D5,20-E2	FPGA_TMPSENS_1A_SCK
15-D3,15-D5,20-E2	FPGA_TMPSENS_1A_CSN
15-D3,15-D5,20-E2	FPGA_TMPSENS_1A_MISO
15-B1,15-D5,20-E2	FPGA_TMPSENS_1B_SCK
15-B1,15-D5,20-E2	FPGA_TMPSENS_1B_CSN
15-B1,15-D5,20-E2	FPGA_TMPSENS_1B_MISO
15-C3,15-D5,20-E2	FPGA_TMPSENS_1C_SCK
14-D4,14-E5,20-E2	FPGA_TMPSENS_1C_CSN
15-B3,15-D5,20-E2	FPGA_TMPSENS_1C_MISO

Temp Sensor Col. 2

15-C3,15-C5,20-D2	FPGA_TMPSENS_2A_SCK
15-C5,15-D3,20-D2	FPGA_TMPSENS_2A_CSN
15-C5,15-D3,20-D2	FPGA_TMPSENS_2A_MISO
15-C3,15-C5,20-D2	FPGA_TMPSENS_2B_SCK
15-C3,15-C5,20-D2	FPGA_TMPSENS_2B_CSN
15-C3,15-C5,20-D2	FPGA_TMPSENS_2B_MISO
15-C5,15-D1,20-D2	FPGA_TMPSENS_2C_SCK
15-C5,15-D1,20-D2	FPGA_TMPSENS_2C_CSN
15-C5,15-D1,20-D2	FPGA_TMPSENS_2C_MISO

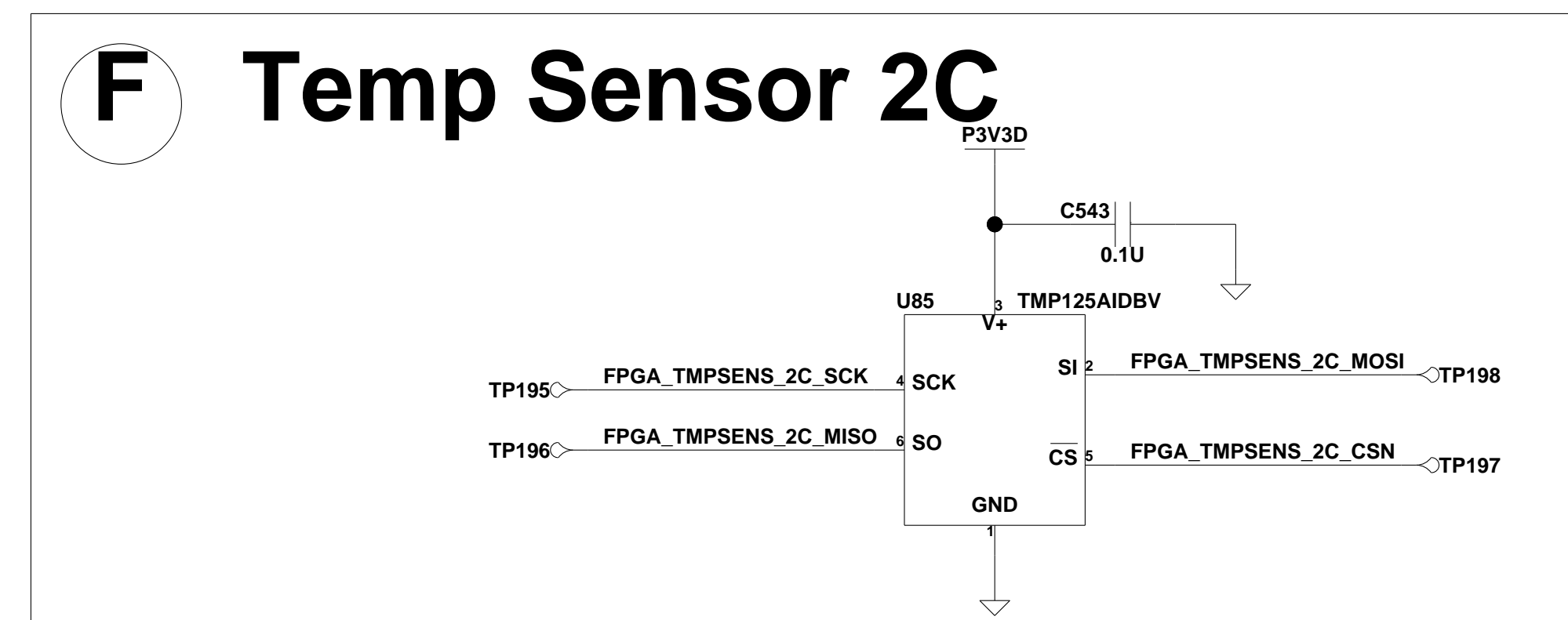
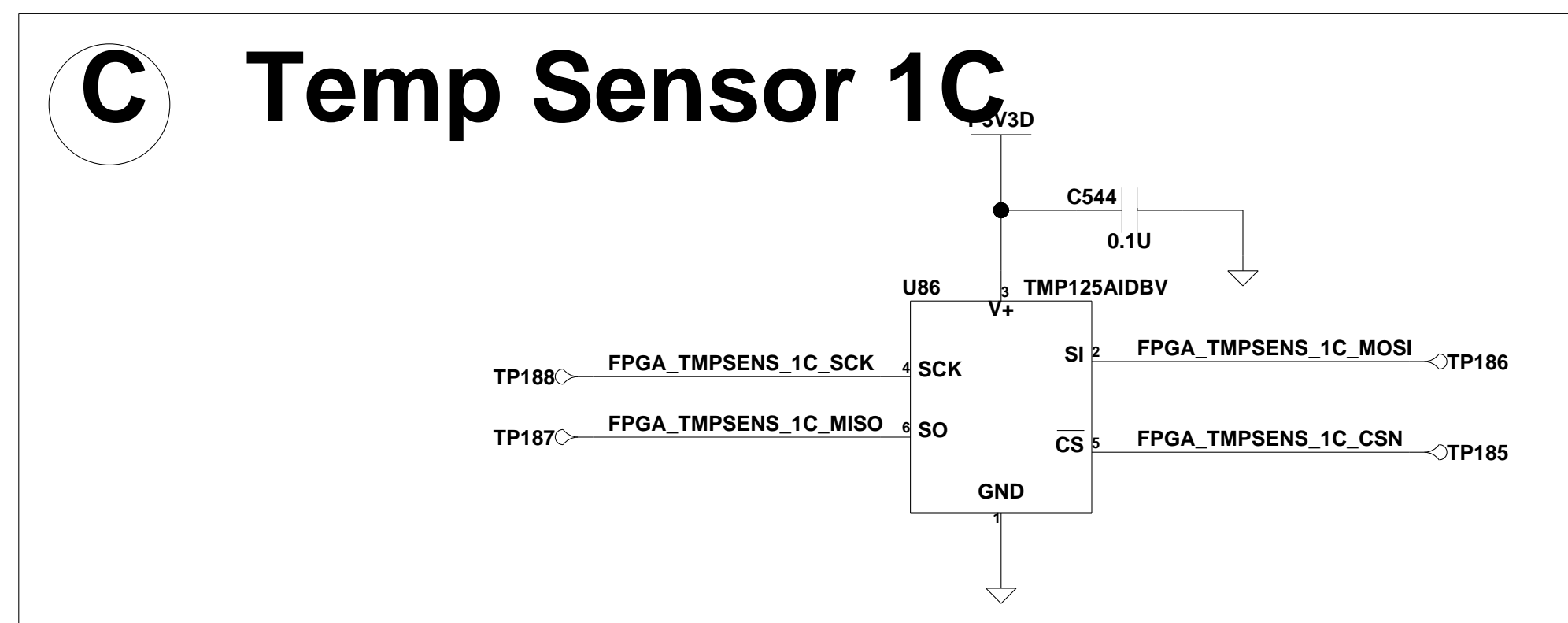
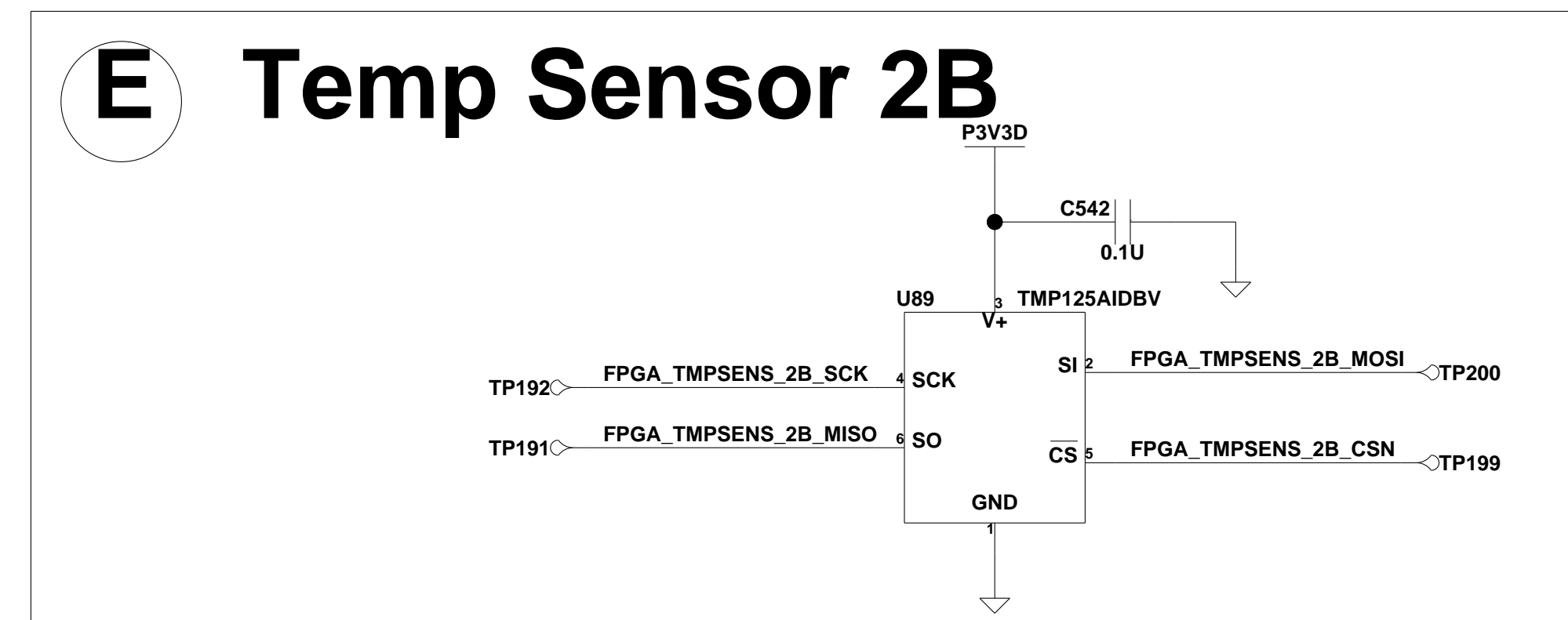
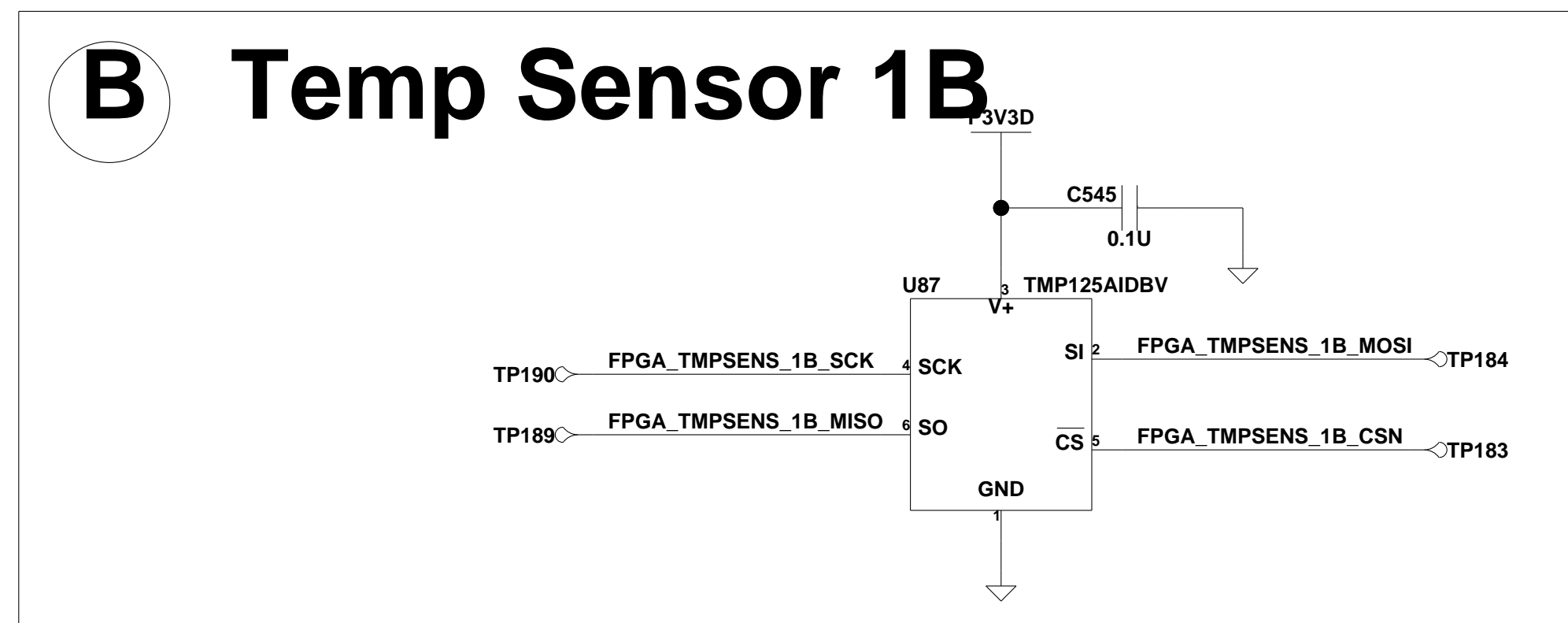
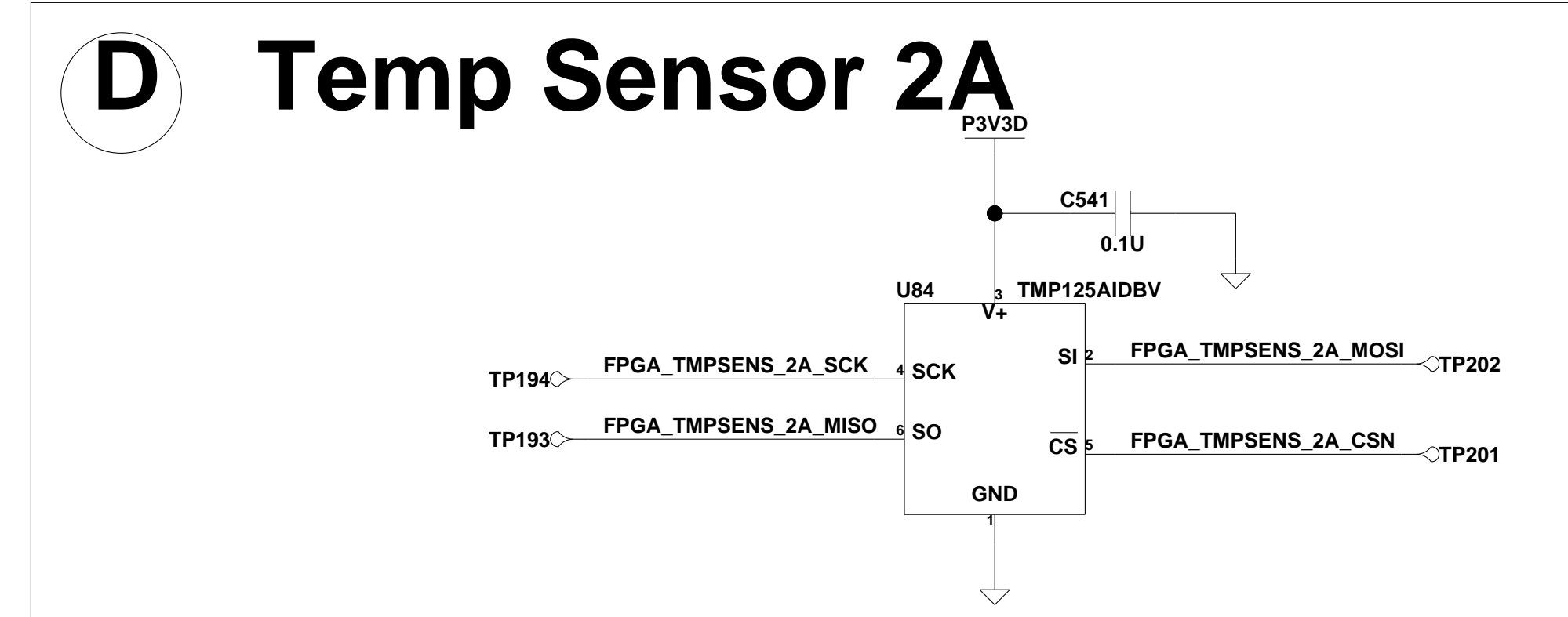
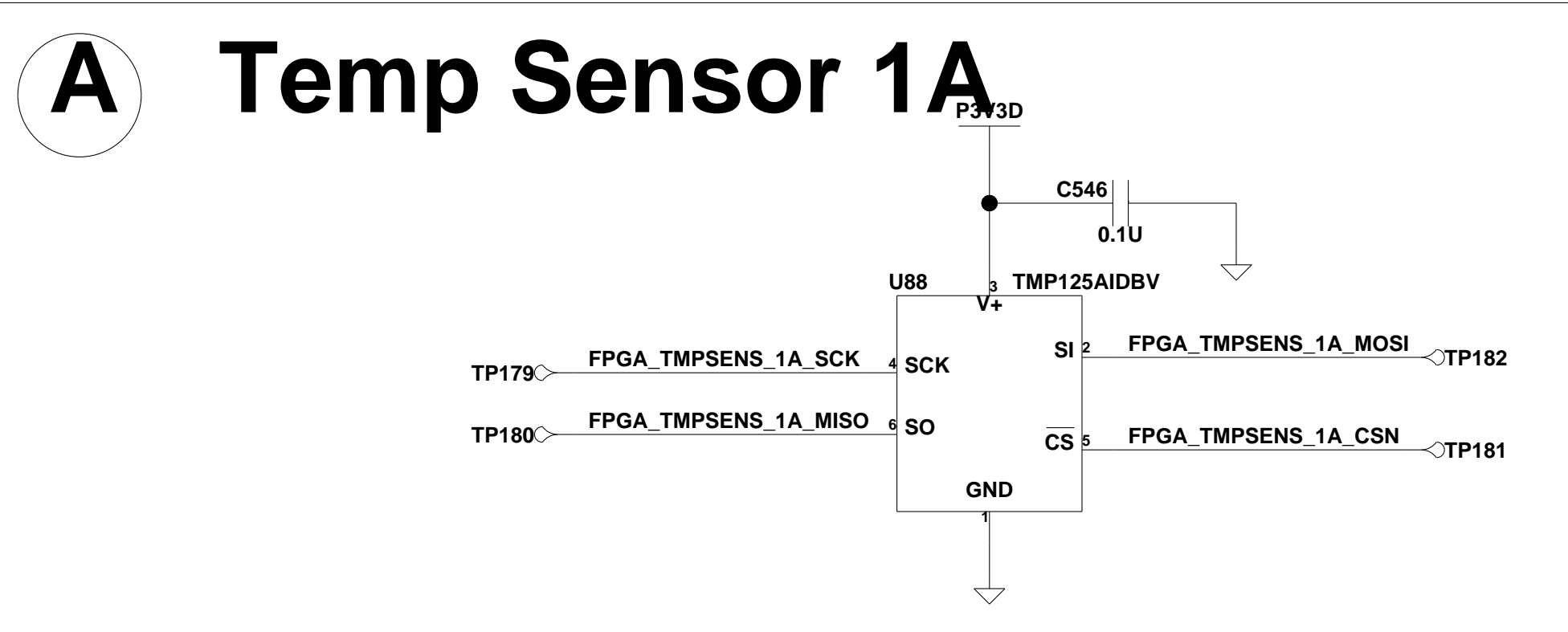
*** OUTPUTS ***

Temp Sensor Col. 1

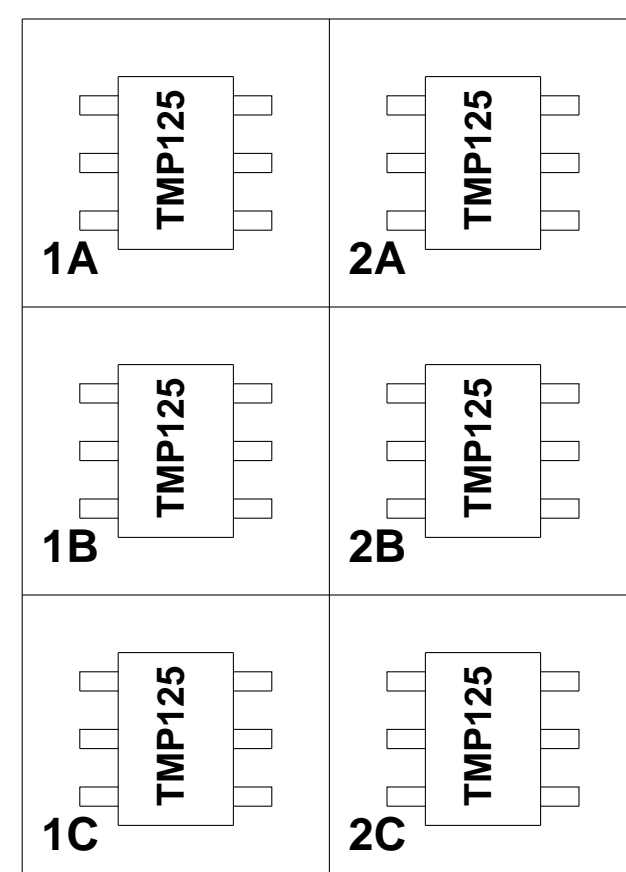
FPGA_TMPSENS_1A_MISO	15-D1,15-D3,20-E7
FPGA_TMPSENS_1B_MISO	15-B1,15-D1,20-E7
FPGA_TMPSENS_1C_MISO	15-B3,15-D1,20-E7

Temp Sensor Col. 2

FPGA_TMPSENS_2A_MISO	15-D1,15-D3,20-E7
FPGA_TMPSENS_2B_MISO	15-C3,15-D1,20-E7
FPGA_TMPSENS_2C_MISO	15-D1,20-E7



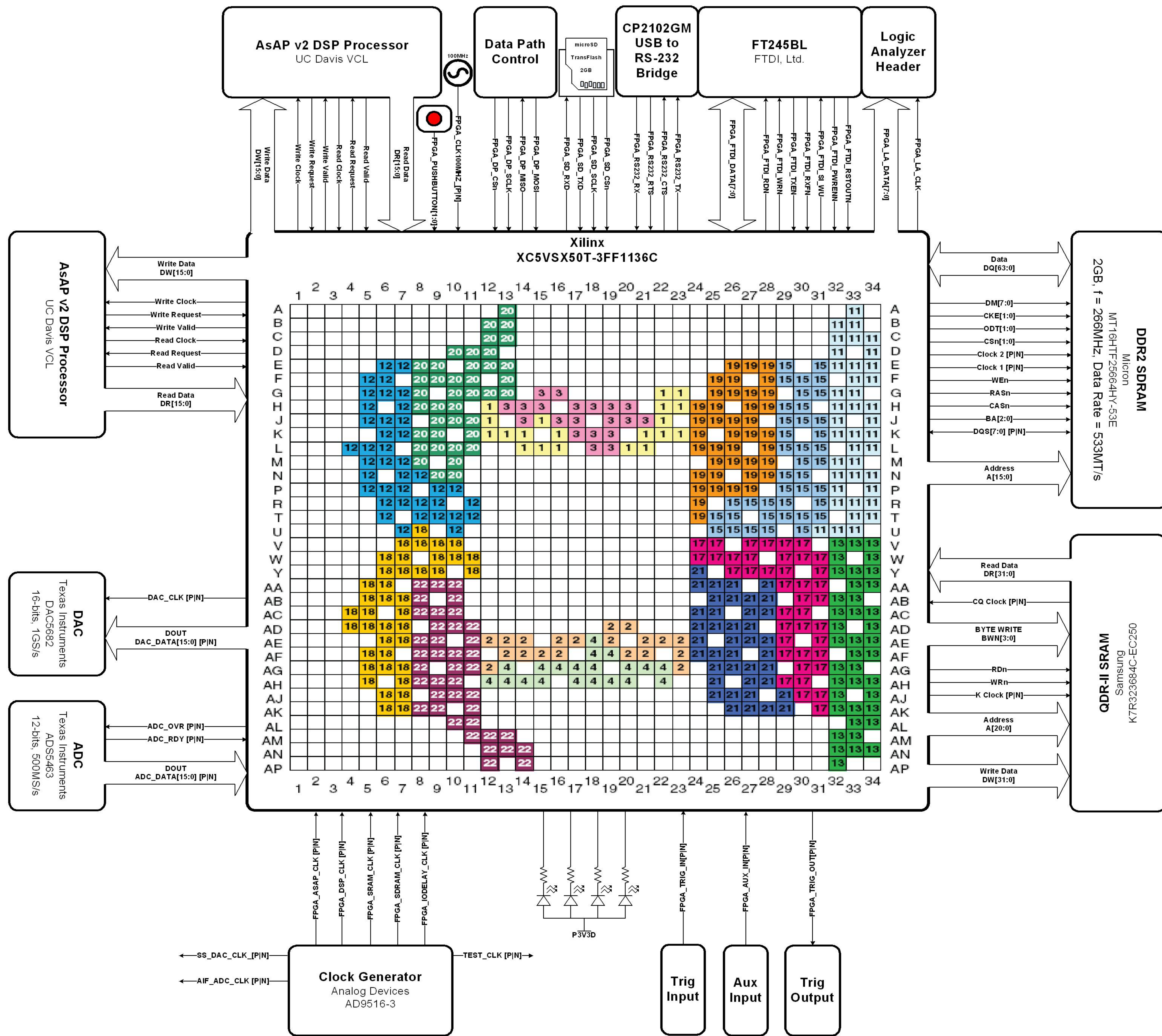
Temp sensors will be placed on a 2x3 Grid on the bottom side of the Measurement board.



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Title: DIGITAL TEMPERATURE SENSORS			
File: MEAS_MAIN_BOARD			
Created by: JEREMY W. WEBB	Date: 4-20-2009_13:35		
Modified by:	Date:		
PCB NO: 342	Size: D	Sheet 20 of 43	REV: 001

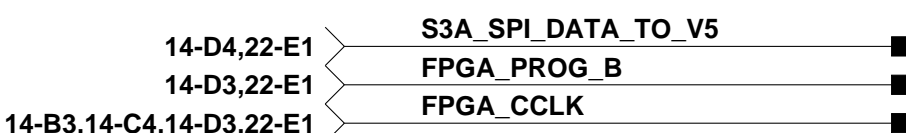
Data Path FPGA Digital Design



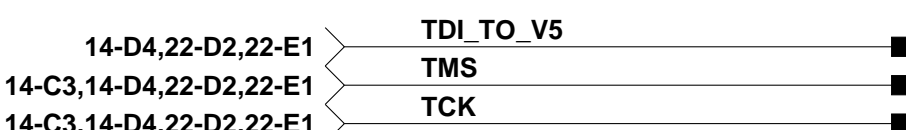
Xilinx Virtex-5 SX50T Configuration

** INPUTS **

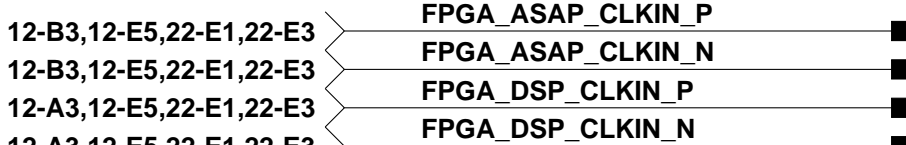
SPI Configuration



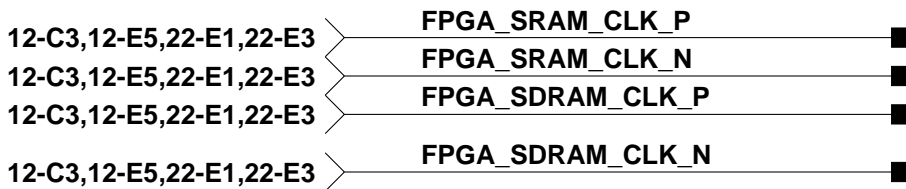
JTAG Configuration



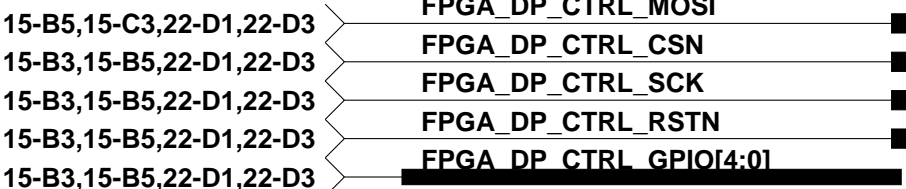
LVPECL Clocks



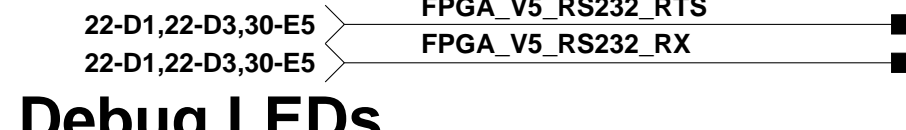
LVDS Clocks



Data Path FPGA Control



USB to RS-232 Interface



Debug LEDs



Debug Push Buttons



MicroSD Interface



100MHz FPGA Clock



Auxiliary Input



Trigger Input



FT245BL USB Interface



Custom Configuration

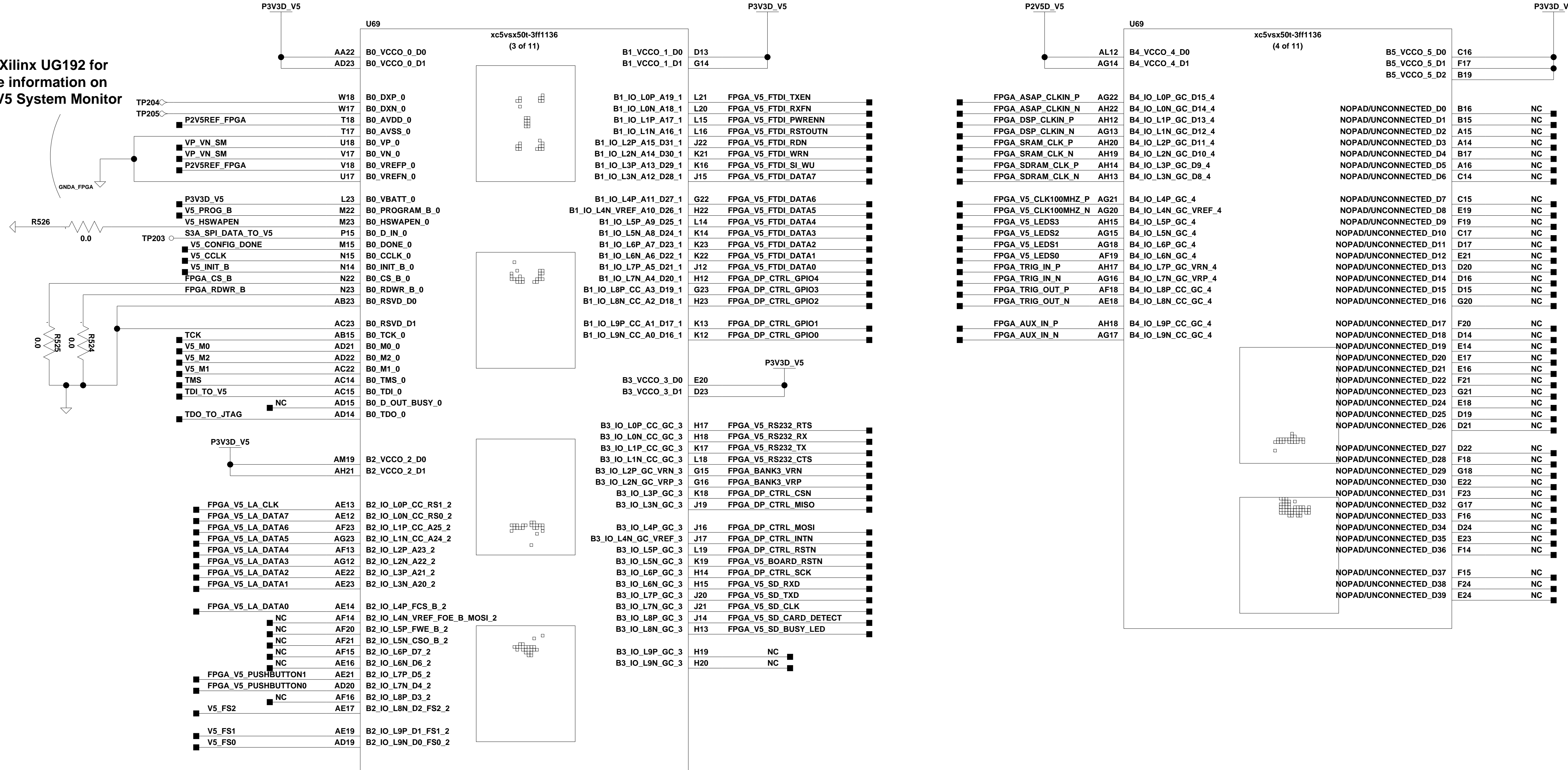


Board Reset



Spartan 3A: VCCO_2 = 3.3V, VCCAUX = 3.3V
Virtex 5 SX50T: VCCO_0 = 3.3V, VCCO_2 = 3.3V

See Xilinx UG192 for more information on the V5 System Monitor



** OUTPUTS **

SPI Configuration



JTAG Configuration



Data Path FPGA Control



MicroSD Interface



USB to RS-232



Trigger Output



FT245BL USB Interface



Custom Configuration



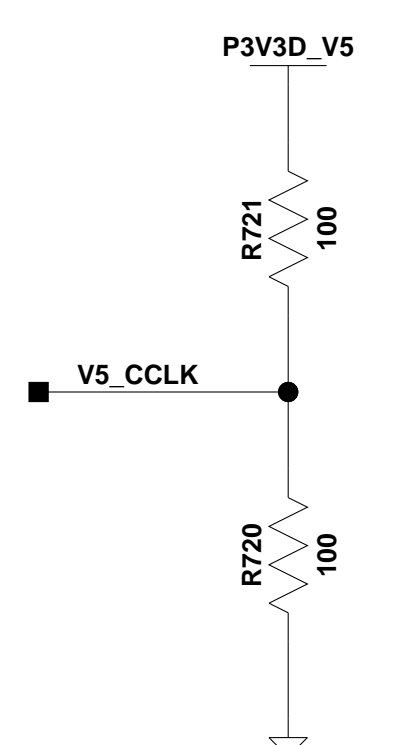
Logic Analyzer



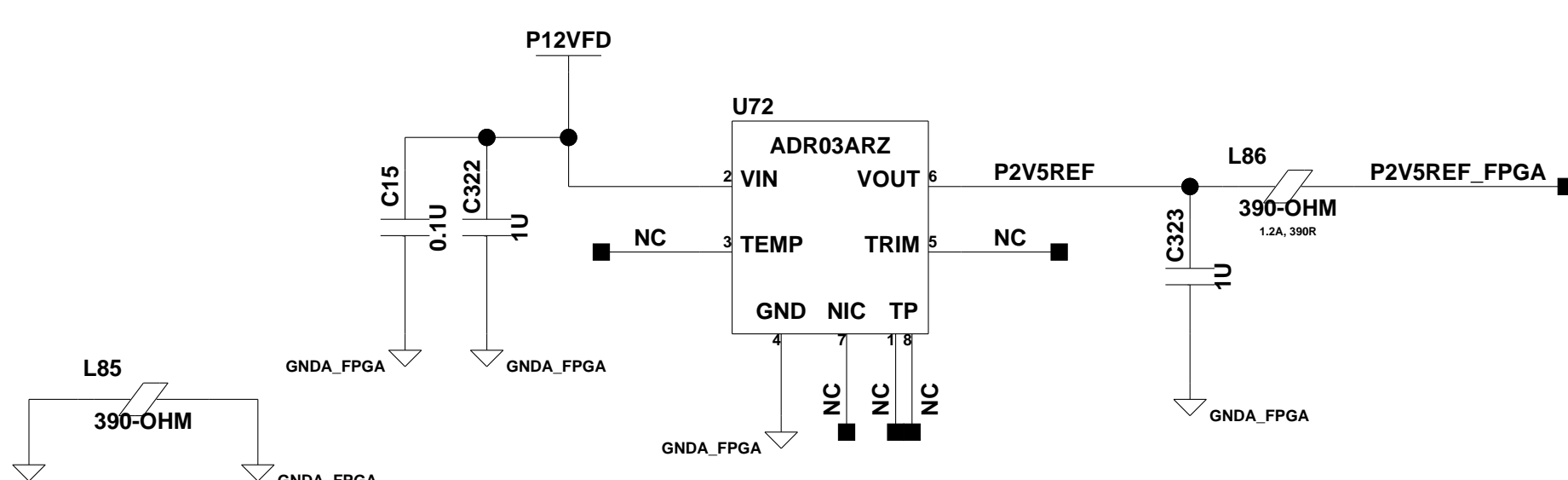
B Virtex-5 SX50T CCLK

NOTES:

FPGA_CCLK requires an end termination and is a 50 Ohm controlled impedance transmission line. The end termination must be placed near the Configuration PROM. FPGA_CCLK Stub Length from S3A to SPI Flash < 12.5 mm



C System Monitor Precision Referenced

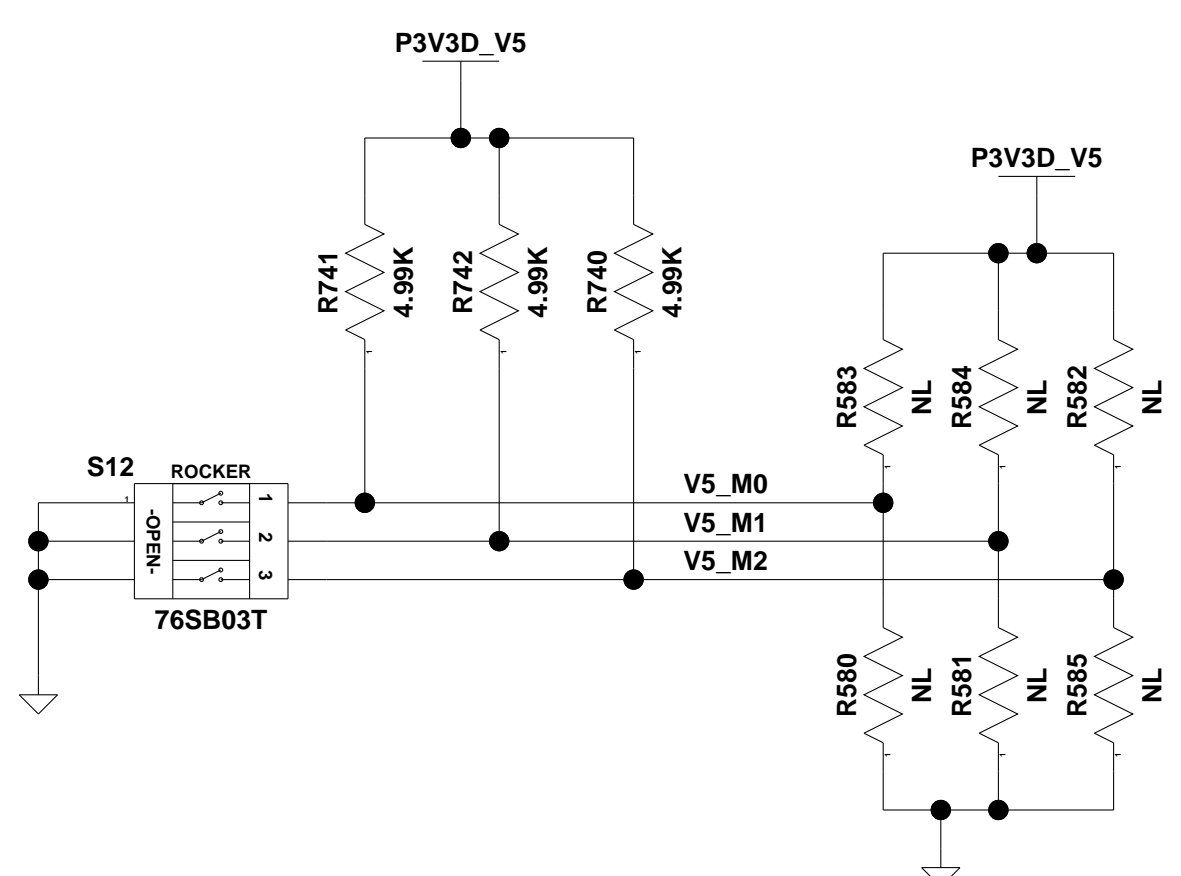


See pages 46-49 of Xilinx UG192 for PC Design Guidelines

D Virtex-5 SX50T FPGA Configuration Mode

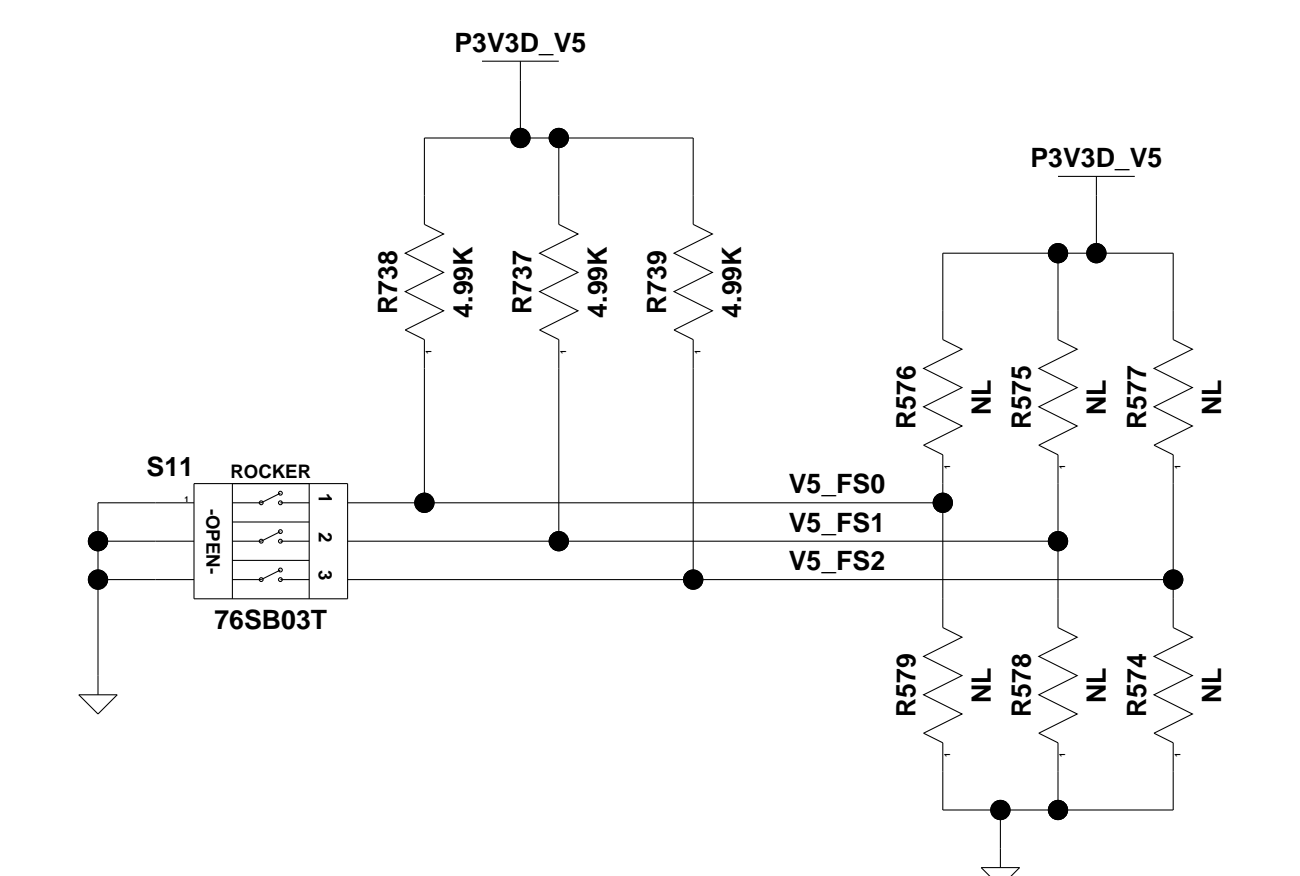
CONFIG MODE	M2	M1	M0	DATA WIDTH	CCLK Direction
Master Serial	0	0	0	1 bit	Output
Master SPI	0	0	1	1 bit	Output
Master BPI-Up	0	1	0	8, 16 bits	Output
Master BPI-Down	0	1	1	8, 16 bits	Output
"Master SelectMAP"	1	0	0	8, 16 bits	Output
JTAG/Bdry Scan	1	0	1	1 bit	Input (TCK)
Slave SelectMAP	1	1	0	8, 16, 32 bits	Input
Slave Serial	1	1	1	1 bit	Input

For more information see Xilinx Virtex 5 Configuration Guide (UG191)



E Virtex-5 SX50T FPGA SPI Mode

FS2	FS1	FS0	HEX CMD CODE
0	0	0	0xFF
0	0	1	RCMD[7:0]
0	1	0	0x52
0	1	1	RESERVED
1	0	0	0x55
1	0	1	0x03
1	1	0	0xE8
1	1	1	0x0B



Xilinx Virtex-5 SX50T I/O

** INPUTS **

SRAM Read Data

23-D4,23-E1,23-E4,28-B4
28-C4,28-E7,28-E8

SRAM Read Clock

23-D4,23-E1,28-A4,28-E7
28-E8

AsAP 1 Data Output

23-D3,23-E1,36-D4,36-E5
23-D3,23-E1,36-D4,36-E5
23-D3,23-E1,36-C4,36-E5

AsAP 1 Data Input

23-D3,23-E1,36-C3,36-E5

** OUTPUTS **

SDRAM Signals

FPGA_DDR2_SDRAM_DQ[63:0] → 23-B1,23-B4,23-C1,23-C4
23-D3,23-E3,28-B2,28-E1
27-C2,27-C3,27-C4,27-D1
27-D2,27-D3,27-D4,27-E1
27-E4

FPGA_DDR2_SDRAM_A[15:0] → 23-B1,23-B4,23-D3,23-E5
27-A3,27-C2,27-D3,27-E1
27-E4

FPGA_DDR2_SDRAM_BA2 → 23-D3,23-E5,27-B4,27-C2
27-E1

FPGA_DDR2_SDRAM_BA1 → 23-B1,23-B4,23-C1,23-D3
23-E3,23-E5,27-C1,27-C3
27-E1

FPGA_DDR2_SDRAM_DQS[0:7] → 23-B1,23-B4,23-C1,23-D3
23-E3,23-E5,27-C1,27-C3
27-E1

FPGA_DDR2_SDRAM_DQSN_NC[7:0] → 23-B1,23-B4,23-C1,23-D3
23-E3,23-E5,27-C1,27-C3
27-E1

FPGA_DDR2_SDRAM_CK_P[1:0] → 23-B1,23-B4,23-E5,27-C1
27-D4,27-E1

FPGA_DDR2_SDRAM_CK_N[1:0] → 23-B1,23-B4,23-E5,27-C1
27-D4,27-E1

FPGA_DDR2_SDRAM_DM[7:0] → 23-D3,23-E3,23-E5,27-C1
23-D3,23-E3,27-D1,27-D2
27-D4,27-E1,27-E2

SRAM Control

FPGA_SRAM_BWN2 → 23-B3,23-E5,28-B2,28-E1
28-E2,28-C4,28-E1

FPGA_SRAM_BWN1 → 28-E2,28-C4,28-E1

FPGA_SRAM_BWN0 → 28-E2,28-C4,28-E1

SRAM Write Data

FPGA_SRAM_WDATA0 → 23-C3,23-D5,28-C2,28-E1
28-E2,28-C4,28-E1

FPGA_SRAM_WDATA1 → 28-E2,28-C4,28-E1

FPGA_SRAM_WDATA2 → 23-C3,23-D5,28-C2,28-E1
28-E2,28-C4,28-E1

FPGA_SRAM_WDATA3 → 23-C3,23-D5,28-C2,28-E1
28-E2,28-C4,28-E1

FPGA_SRAM_WDATA4 → 23-C3,23-D5,28-C2,28-E1
28-E2,28-C4,28-E1

FPGA_SRAM_WDATA5 → 23-C3,23-D5,28-C2,28-E1
28-E2,28-C4,28-E1

FPGA_SRAM_WDATA6 → 23-C3,23-D5,28-C2,28-E1
28-E2,28-C4,28-E1

FPGA_SRAM_WDATA7 → 23-C3,23-D5,28-C2,28-E1
28-E2,28-C4,28-E1

FPGA_SRAM_WDATA8 → 23-B3,23-E5,28-B2,28-E1
28-E2,28-C4,28-E1

FPGA_SRAM_WDATA9 → 23-C3,23-D5,28-C2,28-E1
28-E2,28-C4,28-E1

FPGA_SRAM_WDATA10 → 28-E2,28-C4,28-E1

FPGA_SRAM_WDATA11 → 23-B3,23-E5,28-B2,28-E1
28-E2,28-C4,28-E1

FPGA_SRAM_WDATA12 → 28-E2,28-C4,28-E1

FPGA_SRAM_WDATA13 → 23-C3,23-D5,28-C2,28-E1
28-E2,28-C4,28-E1

FPGA_SRAM_WDATA14 → 23-C3,23-D5,28-C2,28-E1
28-E2,28-C4,28-E1

FPGA_SRAM_WDATA15 → 28-E2,28-C4,28-E1

FPGA_SRAM_WDATA16 → 28-E2,28-C4,28-E1

FPGA_SRAM_WDATA17 → 28-E2,28-C4,28-E1

FPGA_SRAM_WDATA18 → 23-B3,23-E5,28-B2,28-E1
28-E2,28-C4,28-E1

FPGA_SRAM_WDATA19 → 23-B3,23-E5,28-B2,28-E1
28-E2,28-C4,28-E1

FPGA_SRAM_WDATA20 → 28-E2,28-C4,28-E1

FPGA_SRAM_WDATA21 → 23-B3,23-E5,28-B2,28-E1
28-E2,28-C4,28-E1

FPGA_SRAM_WDATA22 → 23-B3,23-E5,28-B2,28-E1
28-E2,28-C4,28-E1

FPGA_SRAM_WDATA23 → 23-B3,23-E5,28-B2,28-E1
28-E2,28-C4,28-E1

FPGA_SRAM_WDATA24 → 23-B3,23-E5,28-B2,28-E1
28-E2,28-C4,28-E1

FPGA_SRAM_WDATA25 → 28-E2,28-C4,28-E1

FPGA_SRAM_WDATA26 → 23-B3,23-E5,28-B2,28-E1
28-E2,28-C4,28-E1

FPGA_SRAM_WDATA27 → 28-E2,28-C4,28-E1

FPGA_SRAM_WDATA28 → 23-B3,23-E5,28-B2,28-E1
28-E2,28-C4,28-E1

FPGA_SRAM_WDATA29 → 23-B3,23-E5,28-B2,28-E1
28-E2,28-C4,28-E1

FPGA_SRAM_WDATA30 → 28-E2,28-C4,28-E1

FPGA_SRAM_WDATA31 → 23-B3,23-E5,28-B2,28-E1
28-E2,28-C4,28-E1

FPGA_SRAM_WDATA32 → 28-E2,28-C4,28-E1

FPGA_SRAM_WDATA33 → 23-B3,23-E5,28-B2,28-E1
28-E2,28-C4,28-E1

FPGA_SRAM_WDATA34 → 23-B3,23-E5,28-B2,28-E1
28-E2,28-C4,28-E1

AsAP 1 Data Output

FPGA_ASAP1_REQ_OUT → 23-C5,23-D3,36-C4,36-E1

AsAP 1 Data Input

FPGA_ASAP1_DATA_IN[15:0] → 23-C5,23-D3,36-E3,36-D3
36-E1,37-C2,37-C4,37-D1
23-D8,23-D3,36-D3,36-E1
23-D4,23-B1,36-D3,36-E1
27-D2,27-D1,27-D2,27-D4

FPGA_ASAP1_CLK_IN → 23-C5,23-D3,36-E3,36-D3
36-E1,37-C2,37-C4,37-D1
23-D8,23-D3,36-D3,36-E1
23-D4,23-B1,36-D3,36-E1
27-D2,27-D1,27-D2,27-D4

FPGA_ASAP1_VLD_IN → 23-C5,23-D3,36-E3,36-D3
36-E1,37-C2,37-C4,37-D1
23-D8,23-D3,36-D3,36-E1
23-D4,23-B1,36-D3,36-E1
27-D2,27-D1,27-D2,27-D4

FPGA_DAC_SYNC_N → 23-B3,23-E5,34-D1

DAC5682 Data/Clock

FPGA_DAC_DATA_P[15:0] → 23-B3,23-E5,23-C3,34-D1
34-E1

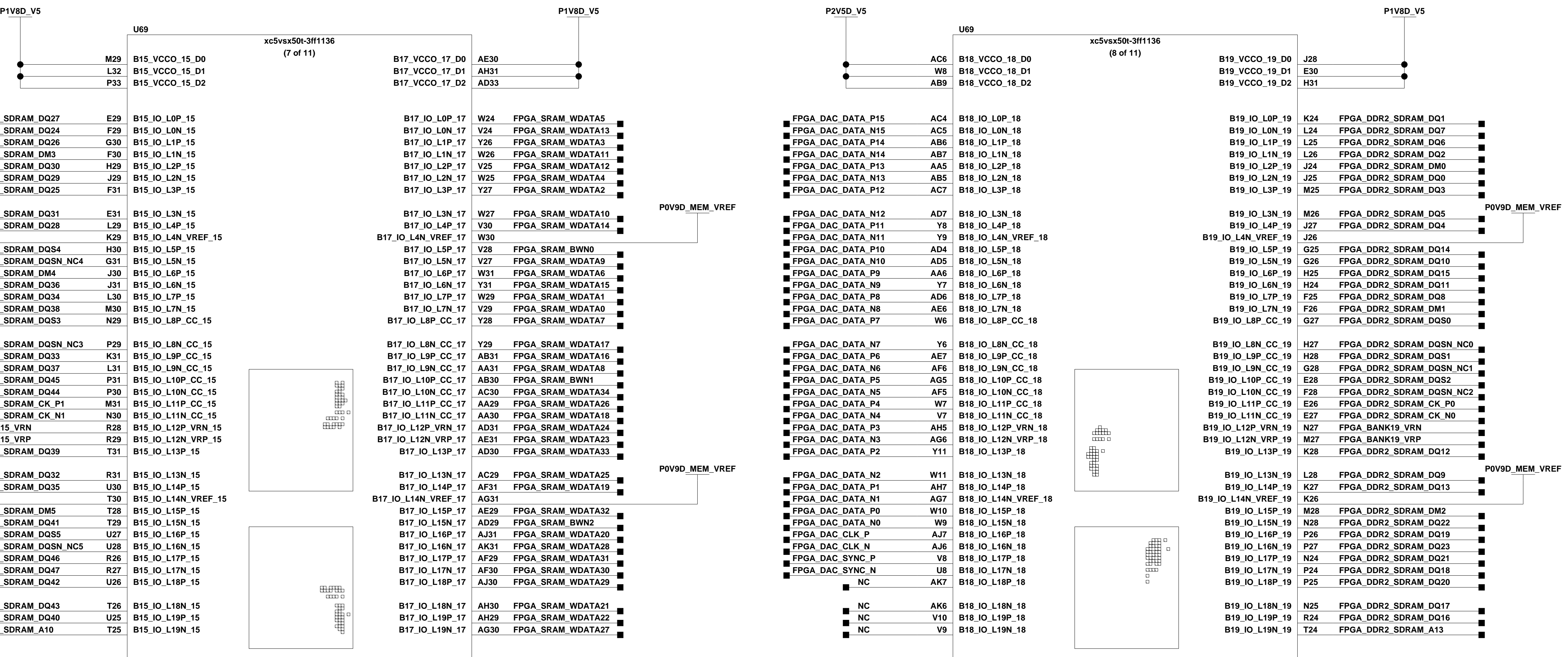
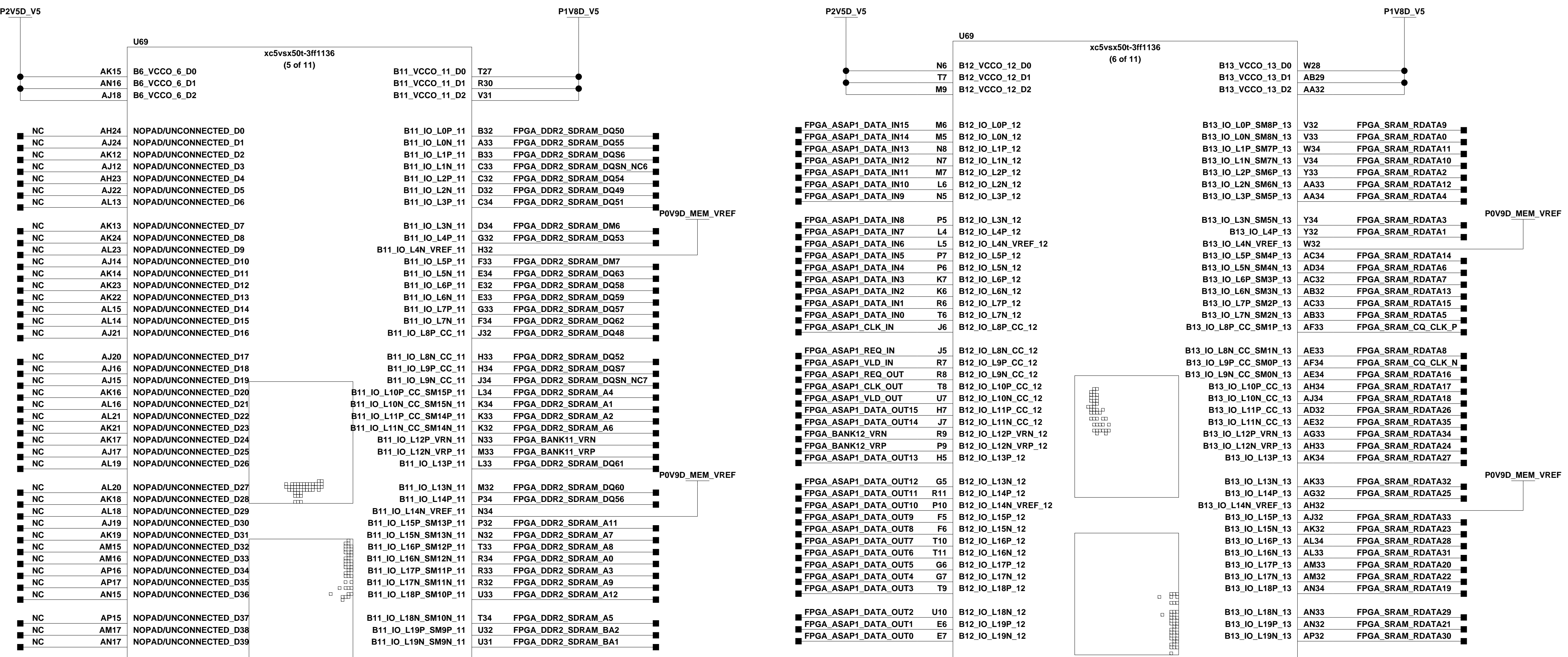
FPGA_DAC_DATA_N[15:0] → 23-B3,23-E5,23-C3,34-D1
34-E1

FPGA_DAC_CLK_P → 23-B3,23-E5,34-E1

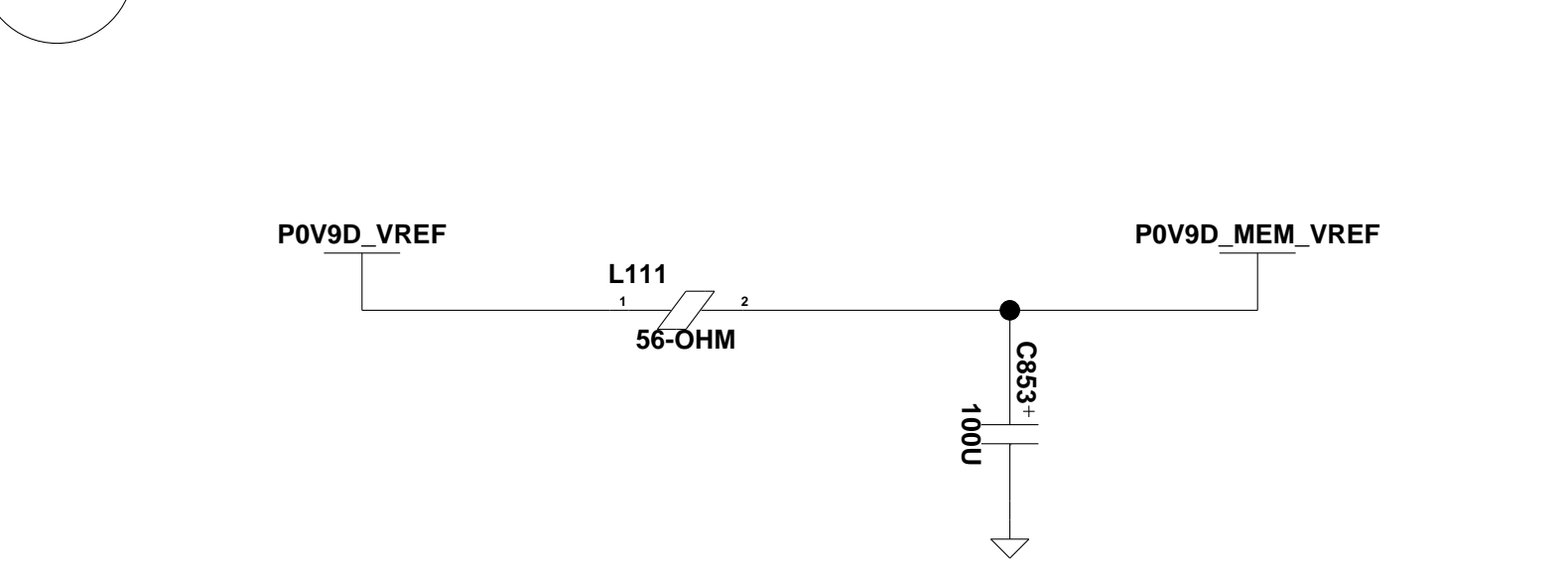
FPGA_DAC_CLK_N → 23-B3,23-E5,34-E1

FPGA_DAC_SYNC_P → 23-B3,23-E5,34-D1

FPGA_DAC_SYNC_N → 23-B3,23-E5,34-D1



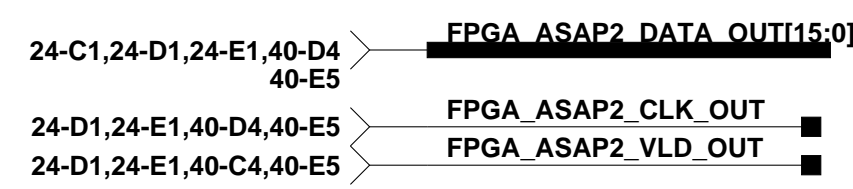
B) DDR2/QDR-II Reference



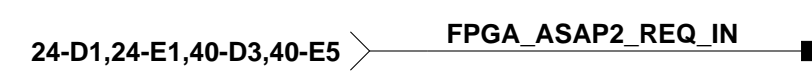
Xilinx Virtex-5 SX50T I/O

**** INPUTS ****

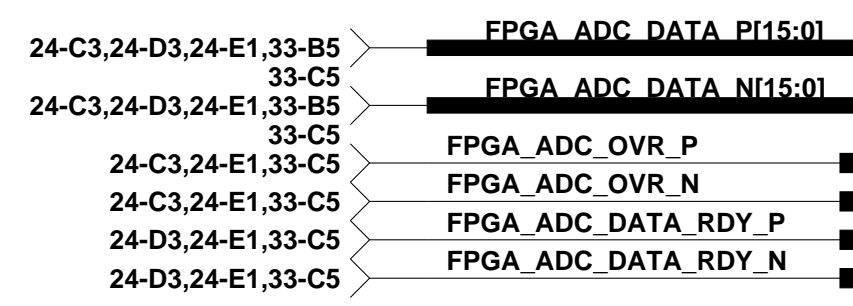
AsAP 2 Data Output



AsAP 2 Data Input

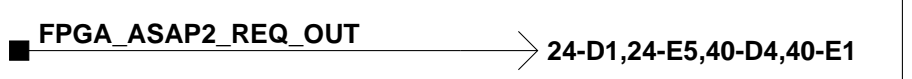


ADS5463 Data/Clock

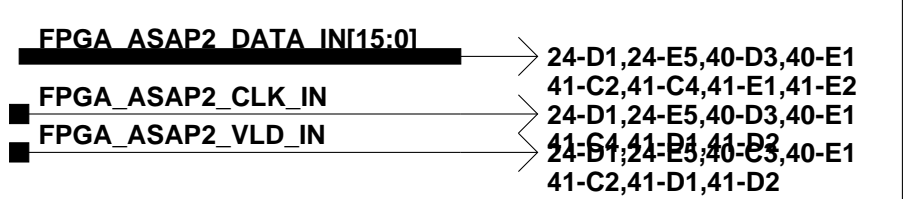


**** OUTPUTS ****

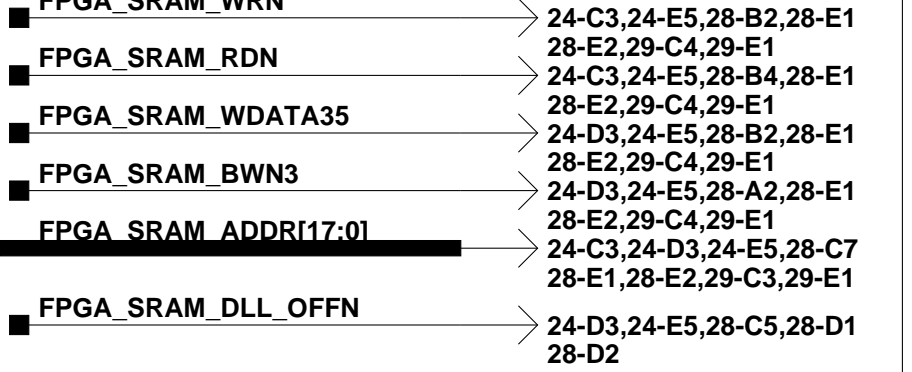
AsAP 2 Data Output



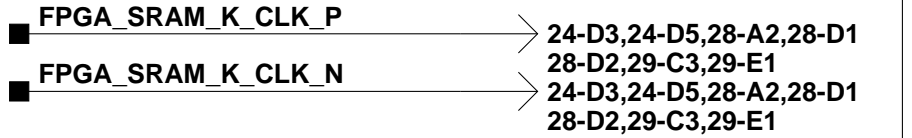
AsAP 2 Data Input



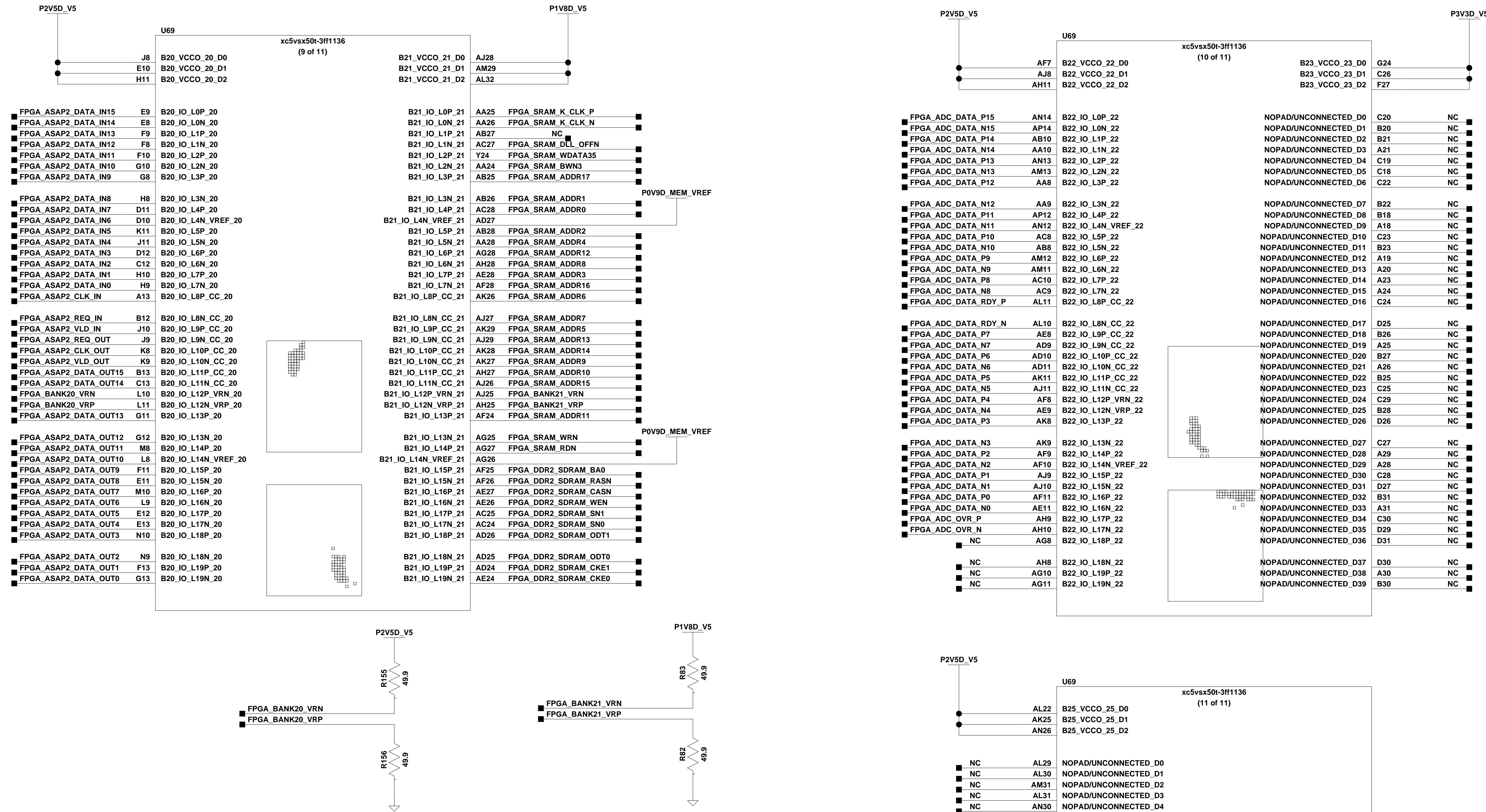
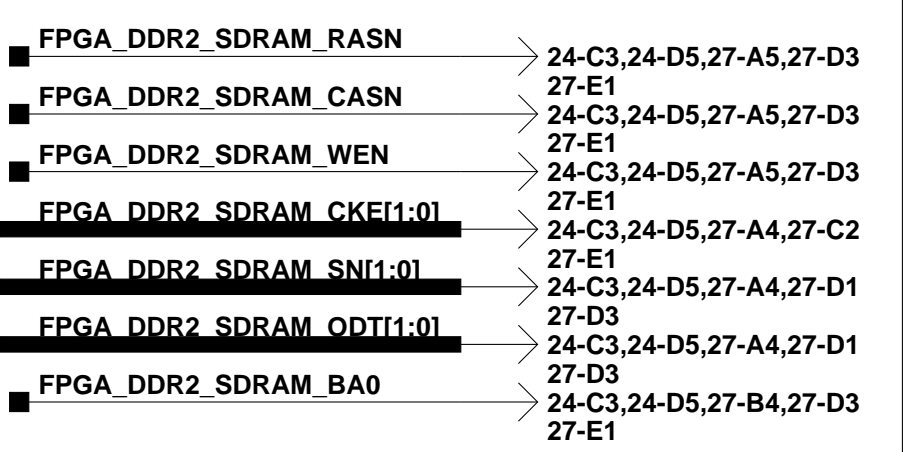
SRAM Control



SRAM Clocks



SDRAM Signals



QDR-II SRAM DCI Constraint: DCI_CASCADE = "21 13 17";
Master Bank: 21
Slave Bank(s): 13, 17
(requires Master Bank to contain at least one I/O standard that uses VRN/VRP)
Pin AB27 will be used as dummy Input and fed to a register.
Banks 13, 17, and 21 are in the same column in order.

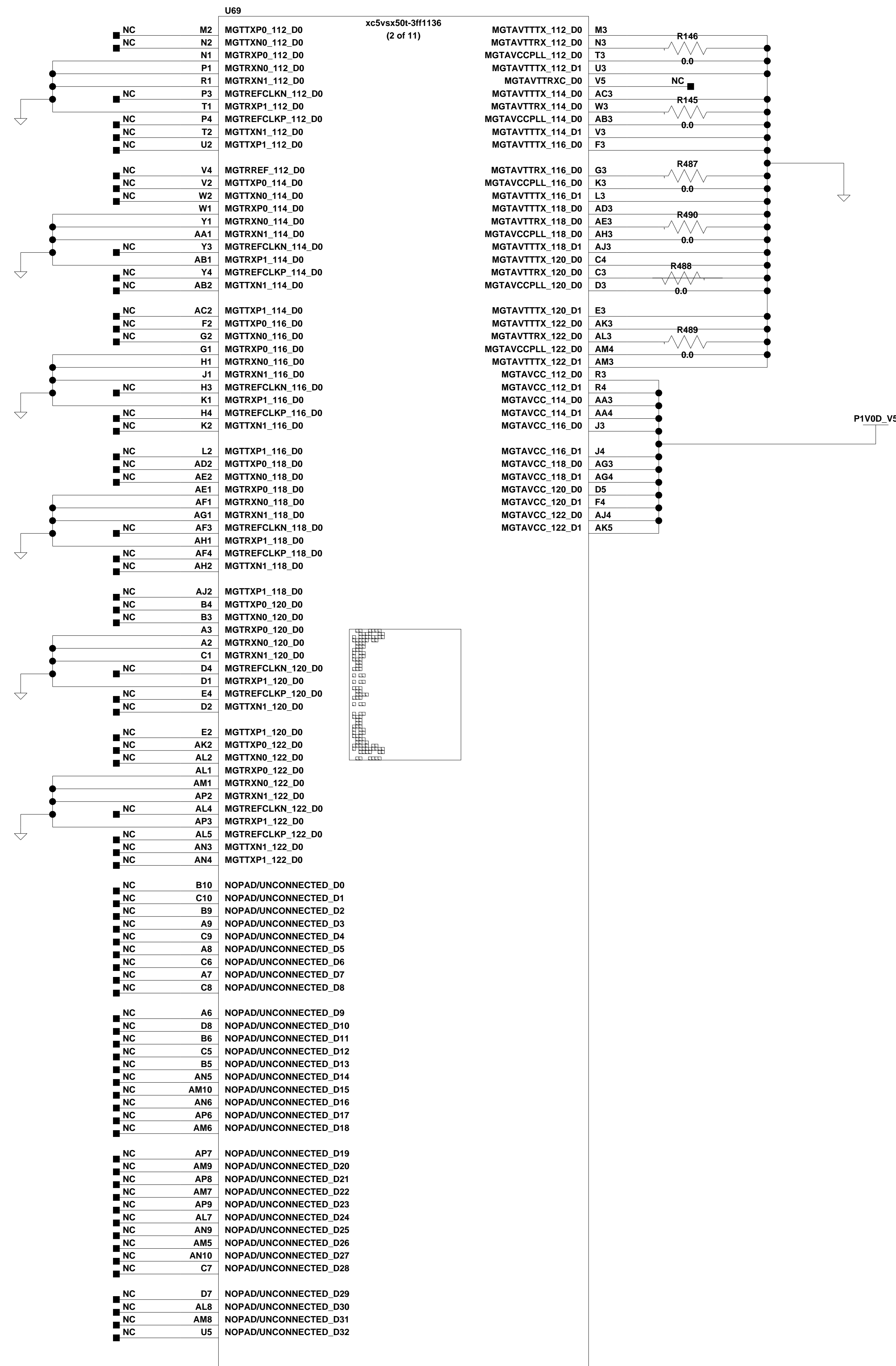
Xilinx Virtex-5 SX50T MGT I/O and Power Inputs

Table 10-5: GTP_DUAL Power Supply Connections for a Completely Unused GTP_DUAL Column

Pin or Pin Pair	Connect To
MGTRXP/MGTRXN	GND
MGTTXP/MGTTXN	Floating, No connection
MGTREFCLKP/MGTREFCLKN	Floating, No connection
MGTITX	GND
MGTTRX	GND
MGTAVTRXC	Floating, No connection
MGTAVCCPLL	GND
MGTAVCC ⁽¹⁾	V _{CCINT} or GND

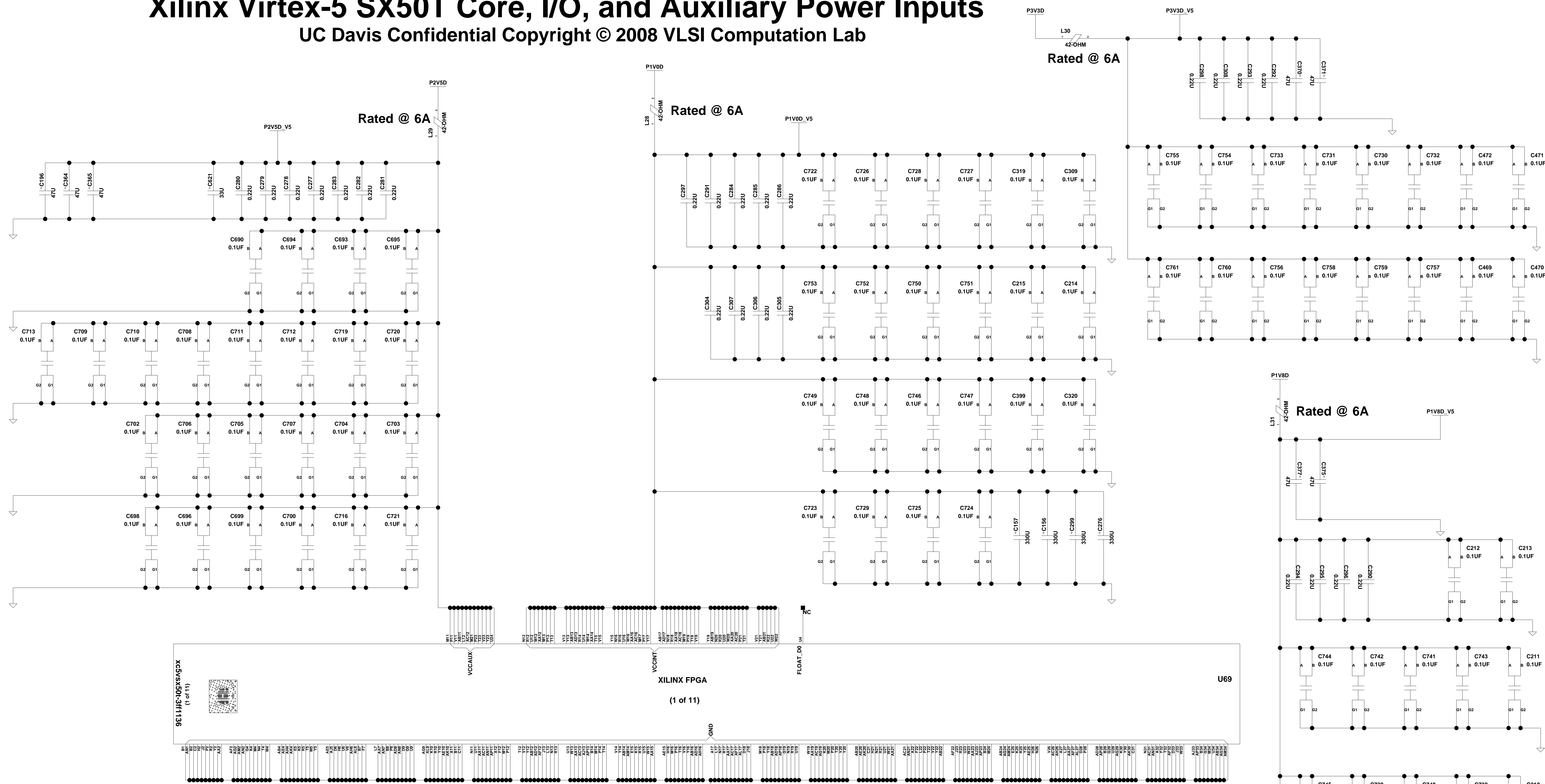
Notes:

1. If Boundary-Scan is part of the product verification, connect the analog supply voltage pin MGTAVCC of all GTP_DUAL tiles directly without filtering to the V_{CCINT} pins of the device. If Boundary-Scan is *not* part of the product verification, connect MGTAVCC to GND.

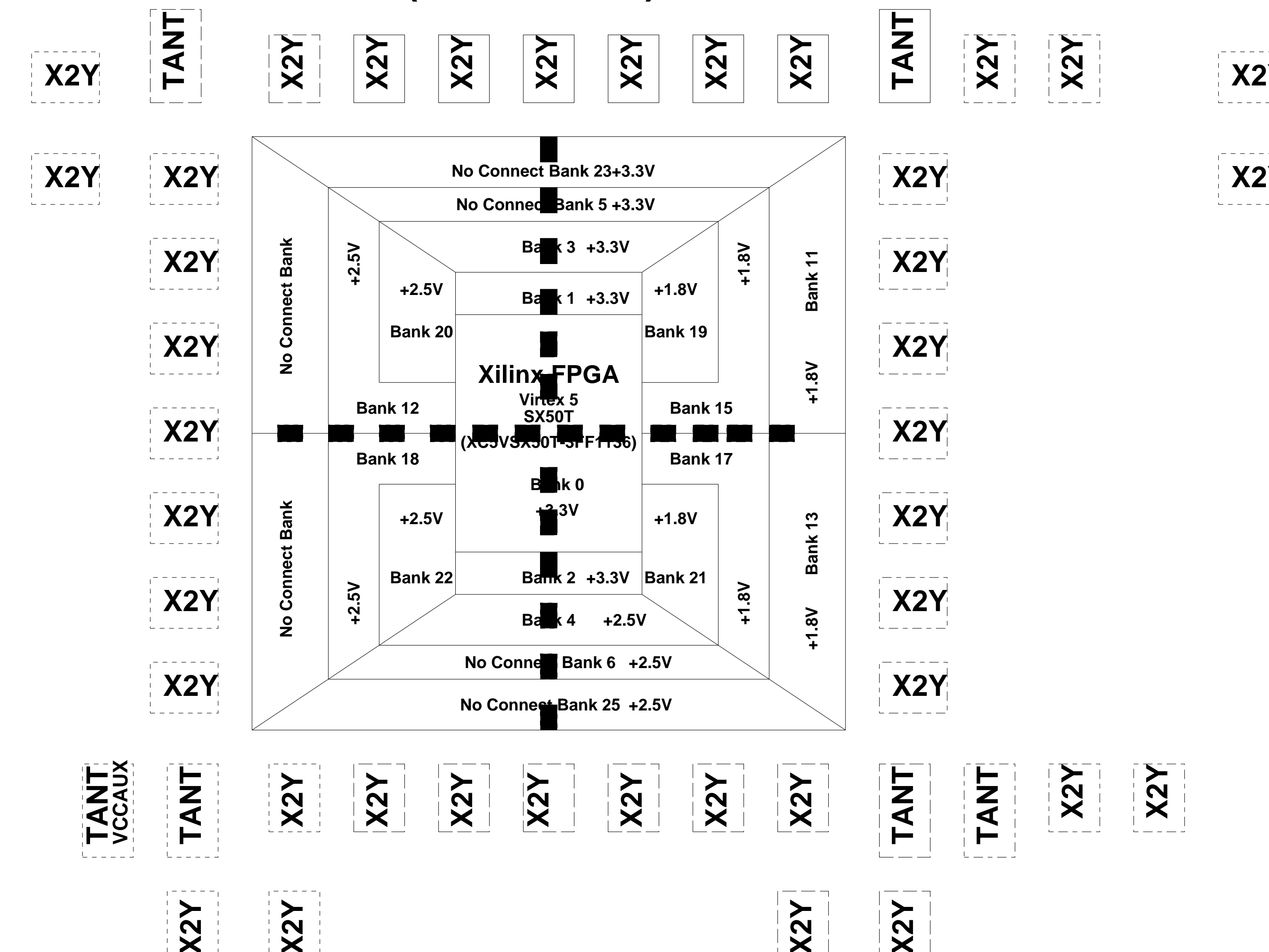


Xilinx Virtex-5 SX50T Core, I/O, and Auxiliary Power Inputs

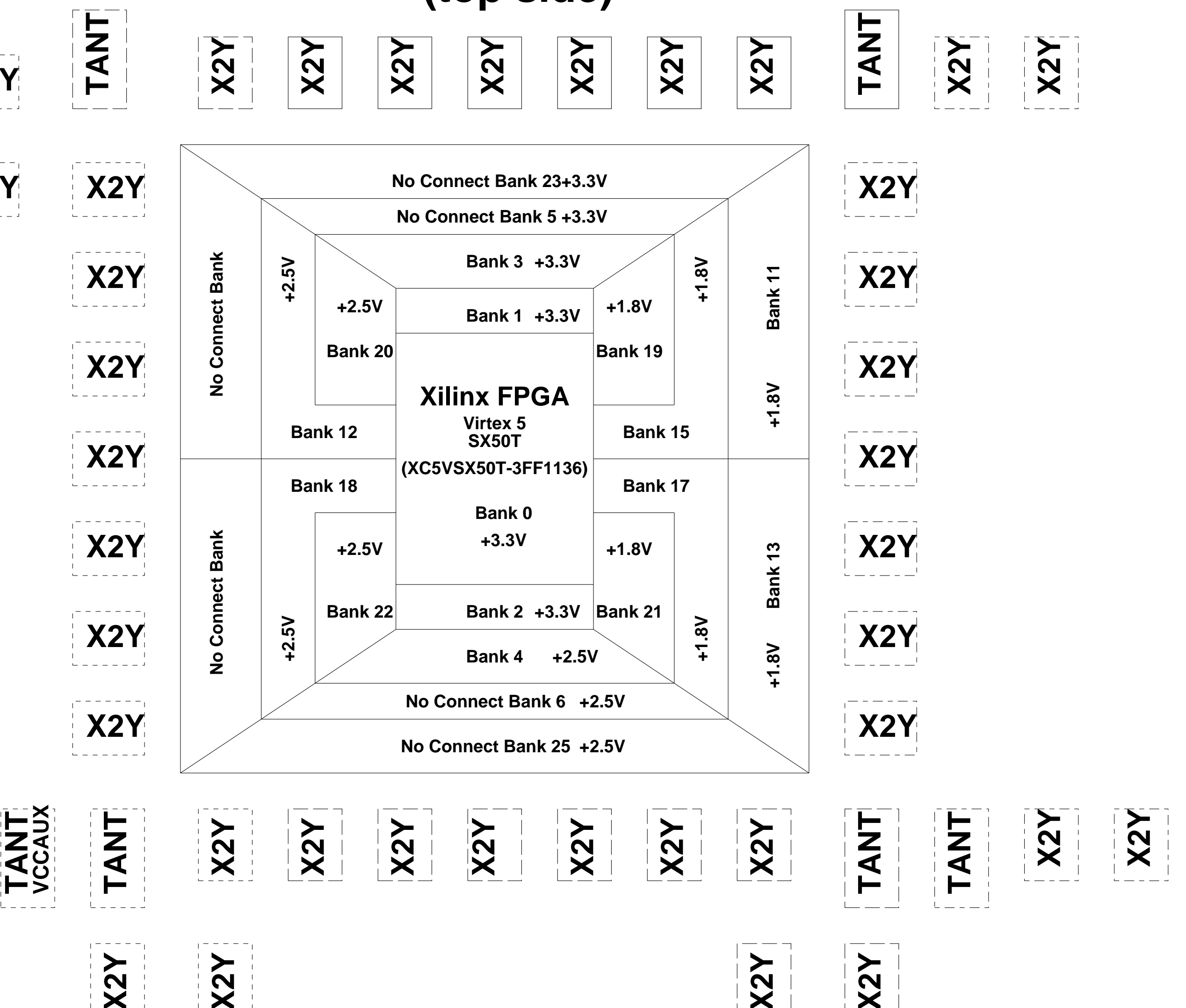
UC Davis Confidential Copyright © 2008 VLSI Computation Lab



Capacitor Placement (bottom side)



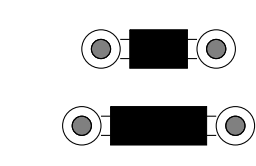
Capacitor Placement (top side)



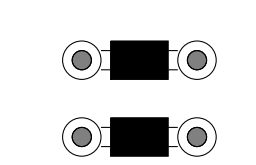
Capacitor Legend:

PWR	0402	X2Y / TANT
+1V	■	□
+1.8V	■	□
+2.5V	■	□
+3.3V	■	□

X2Y Capacitor Via Placement



Tantalum/O402 Via Placement

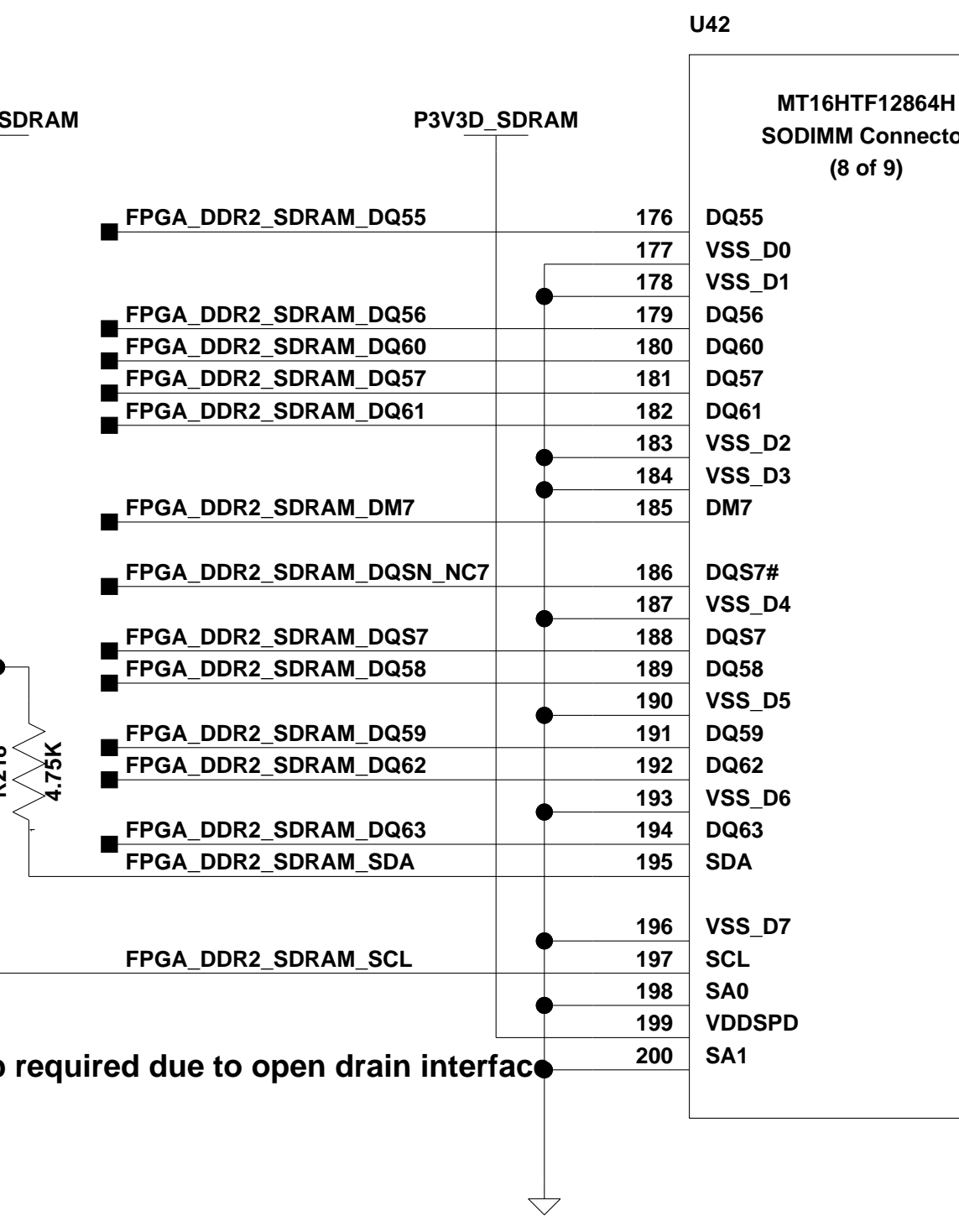
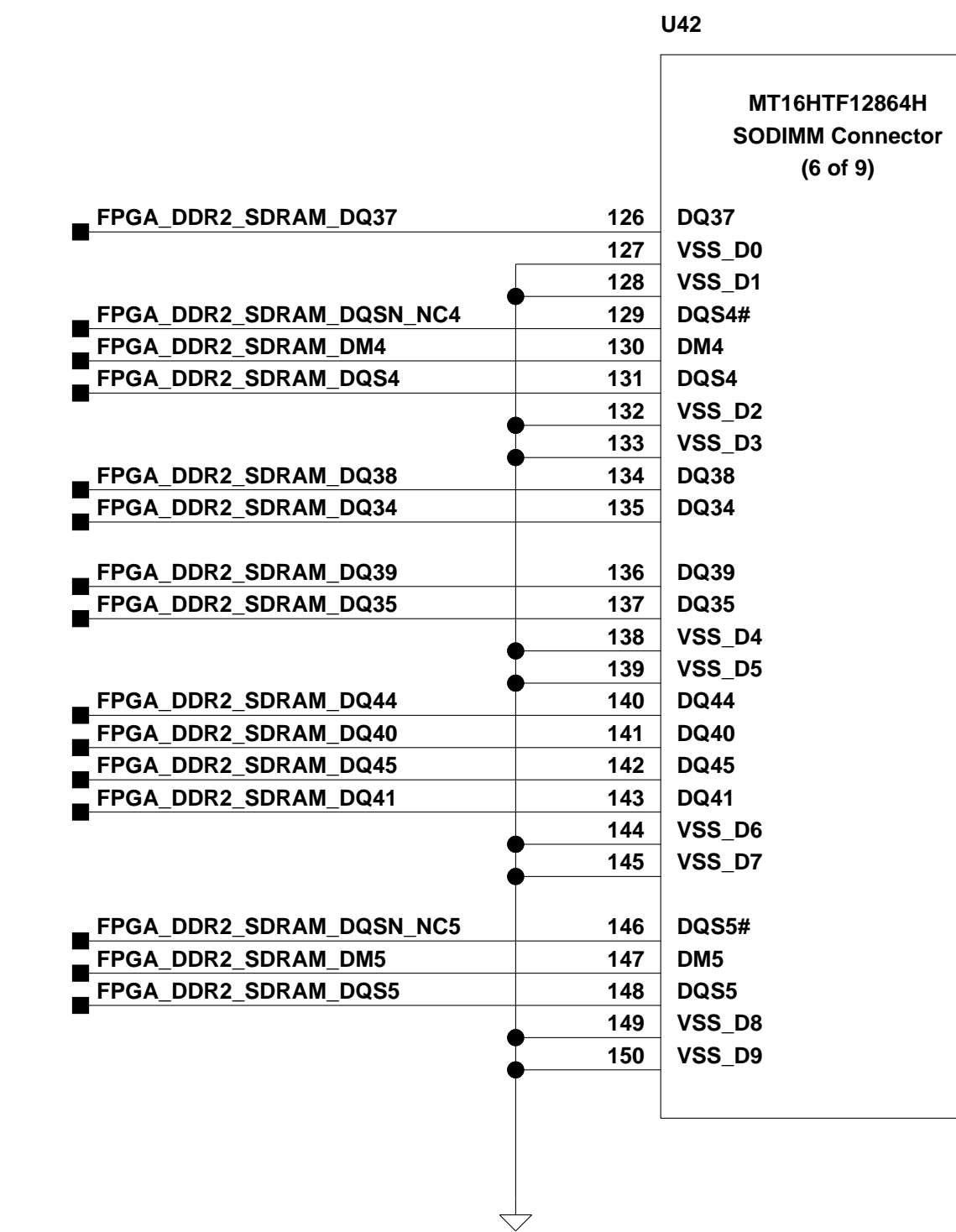
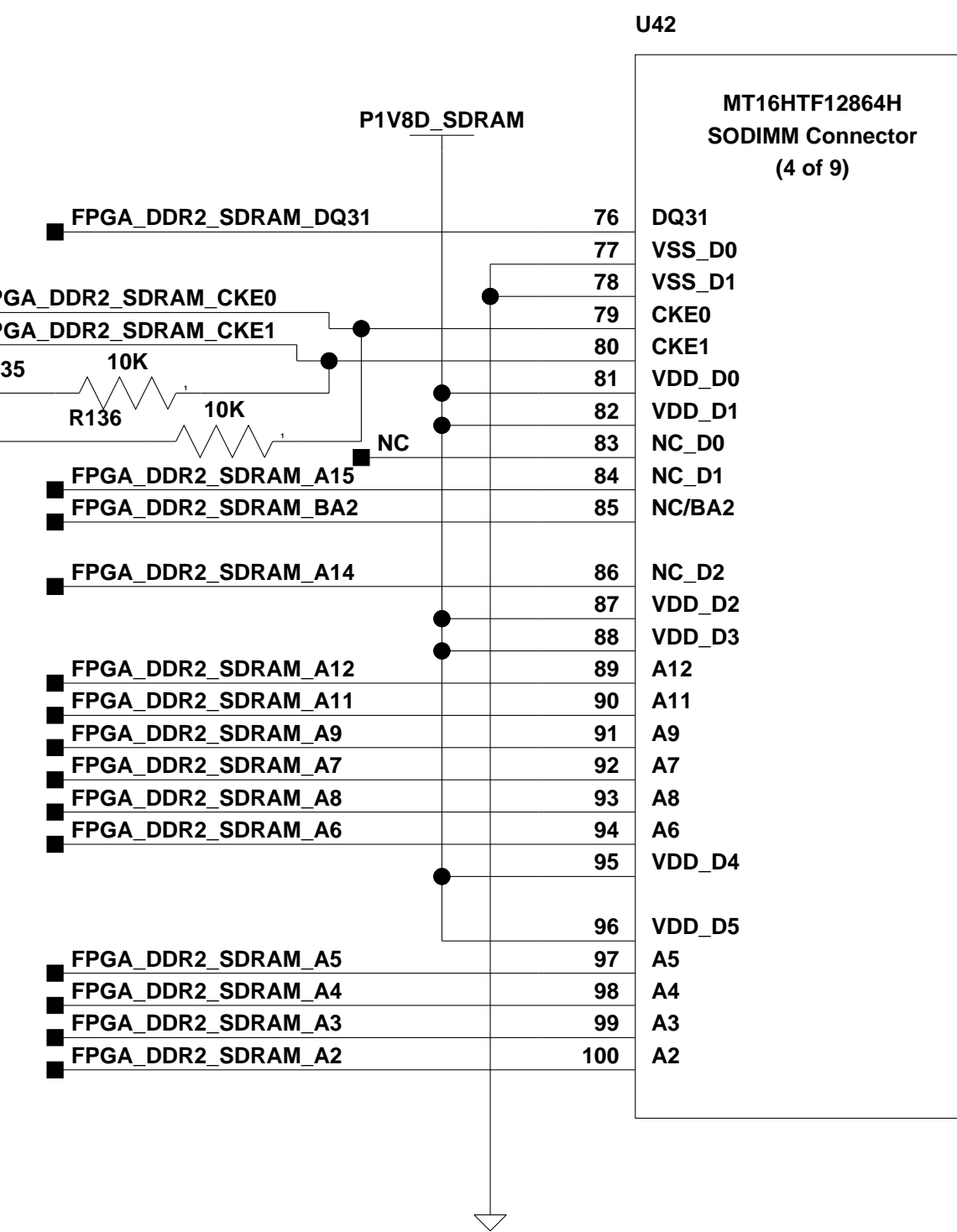
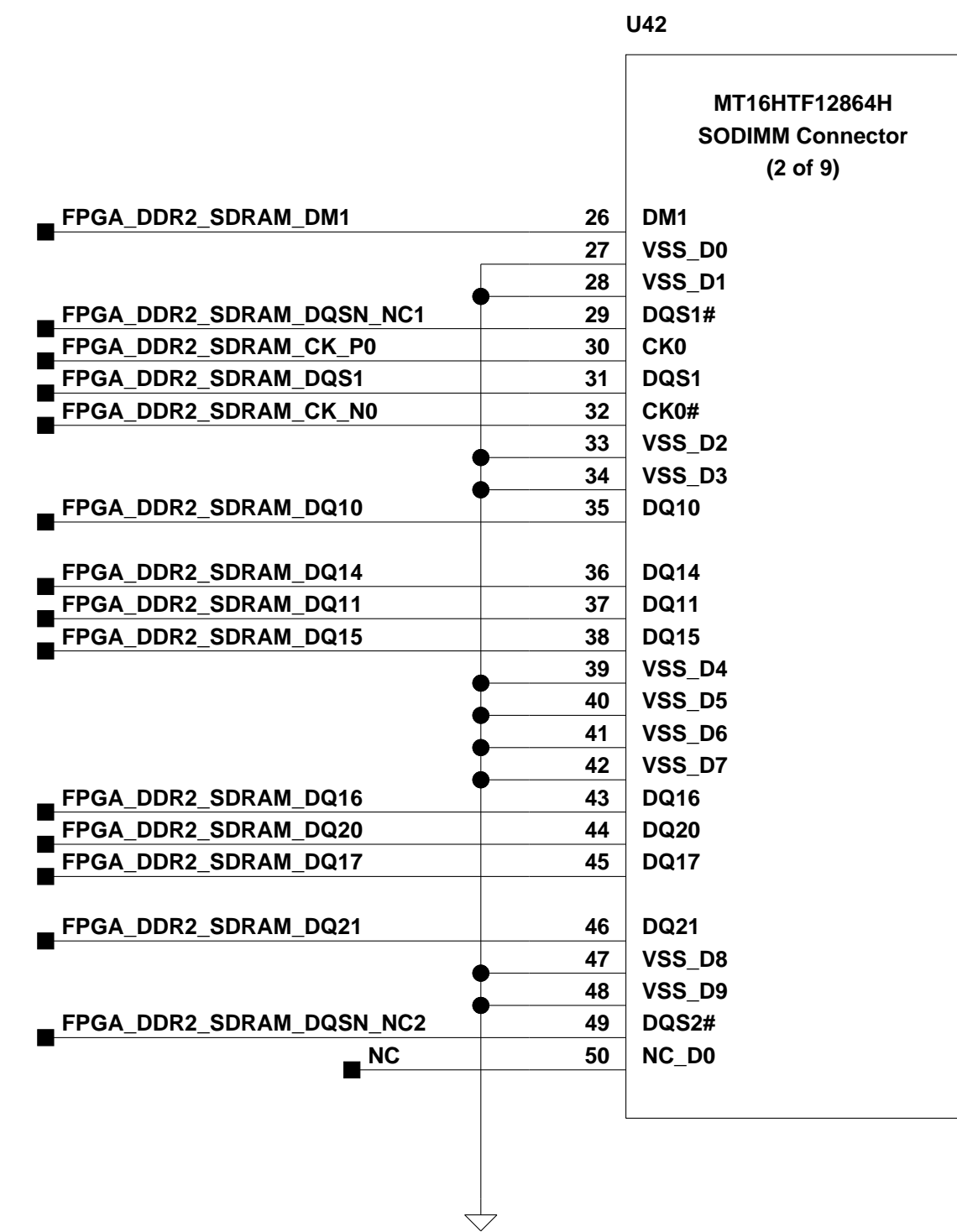
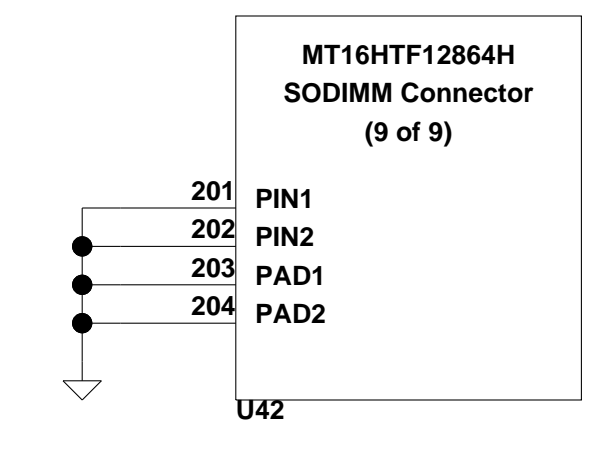
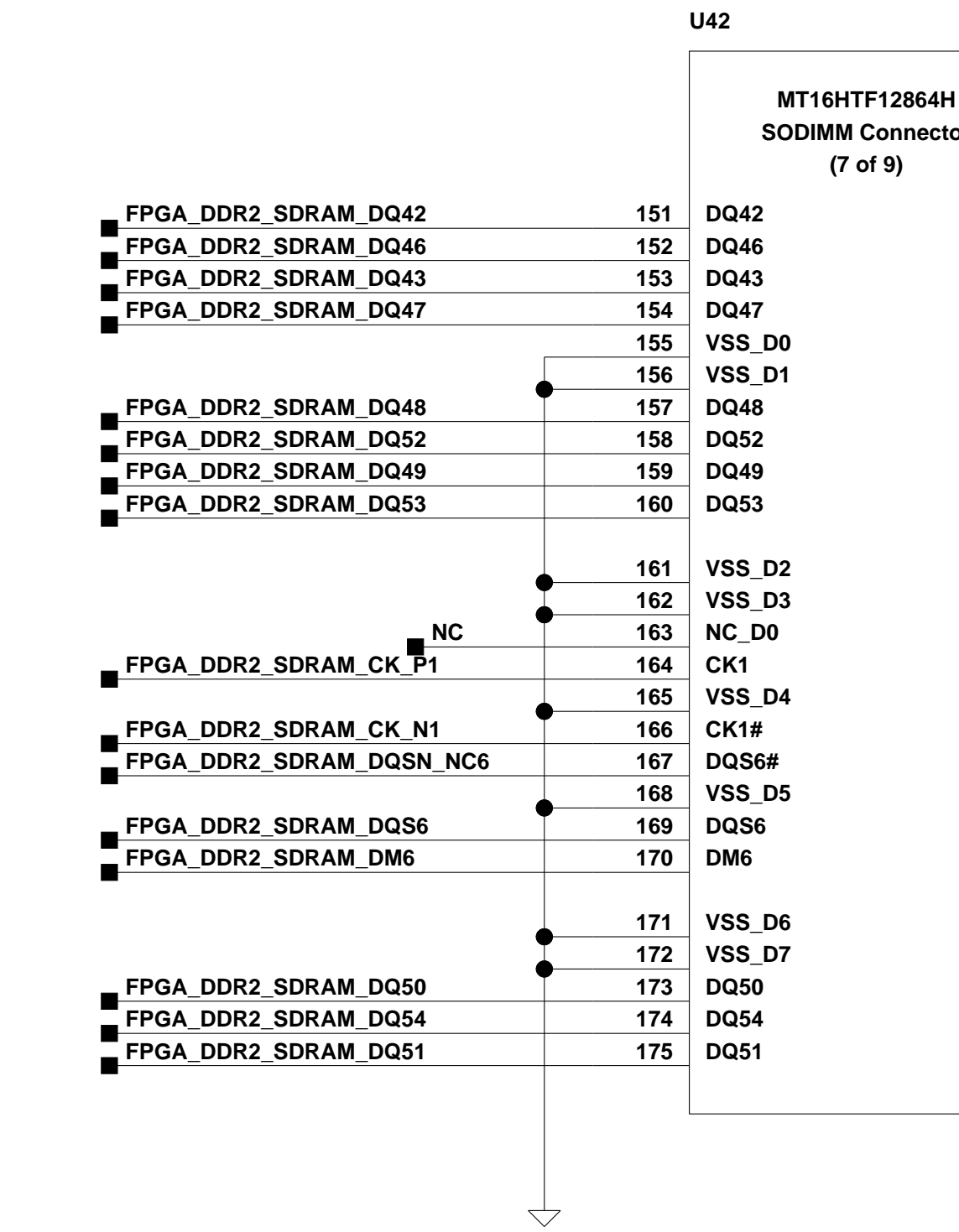
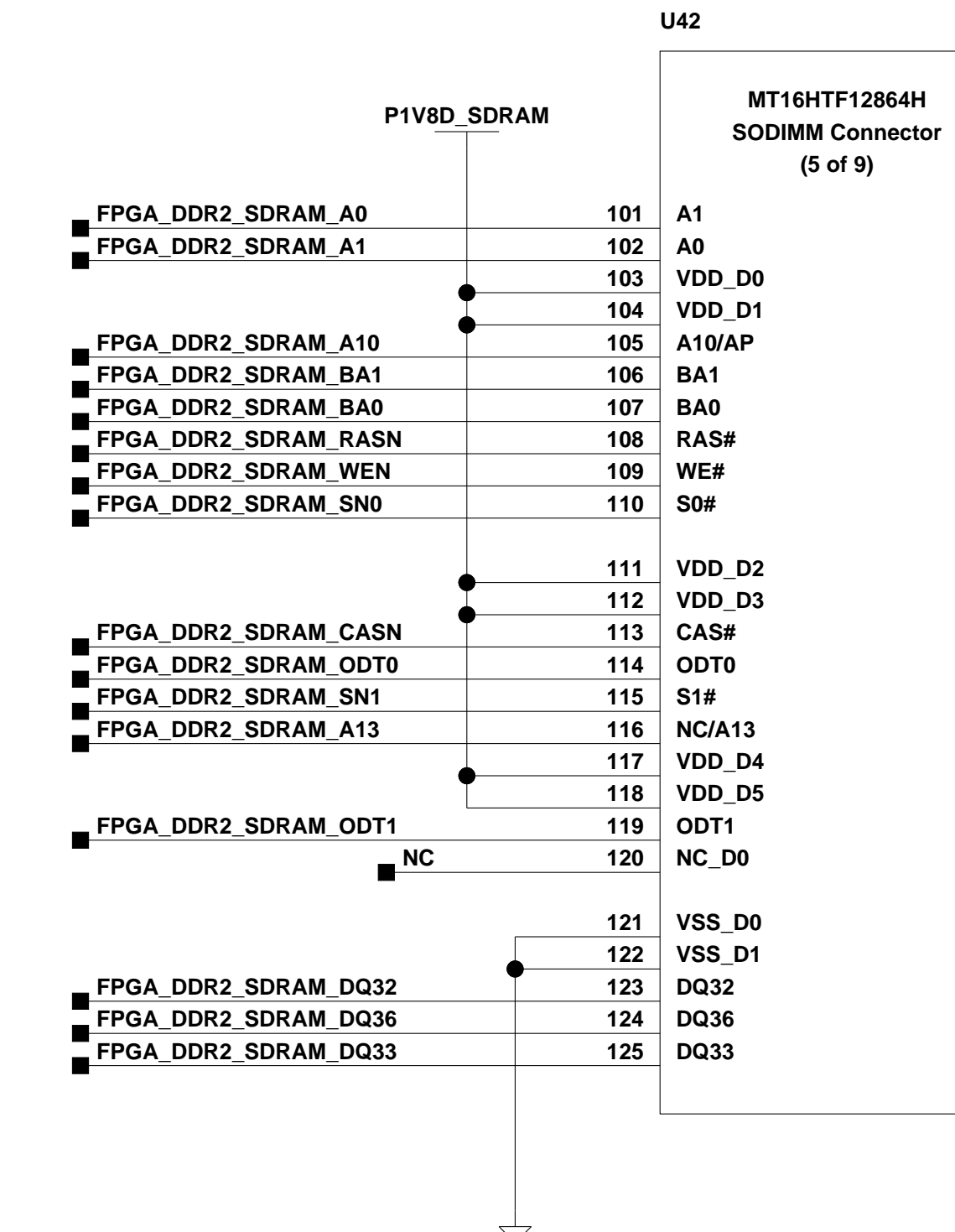
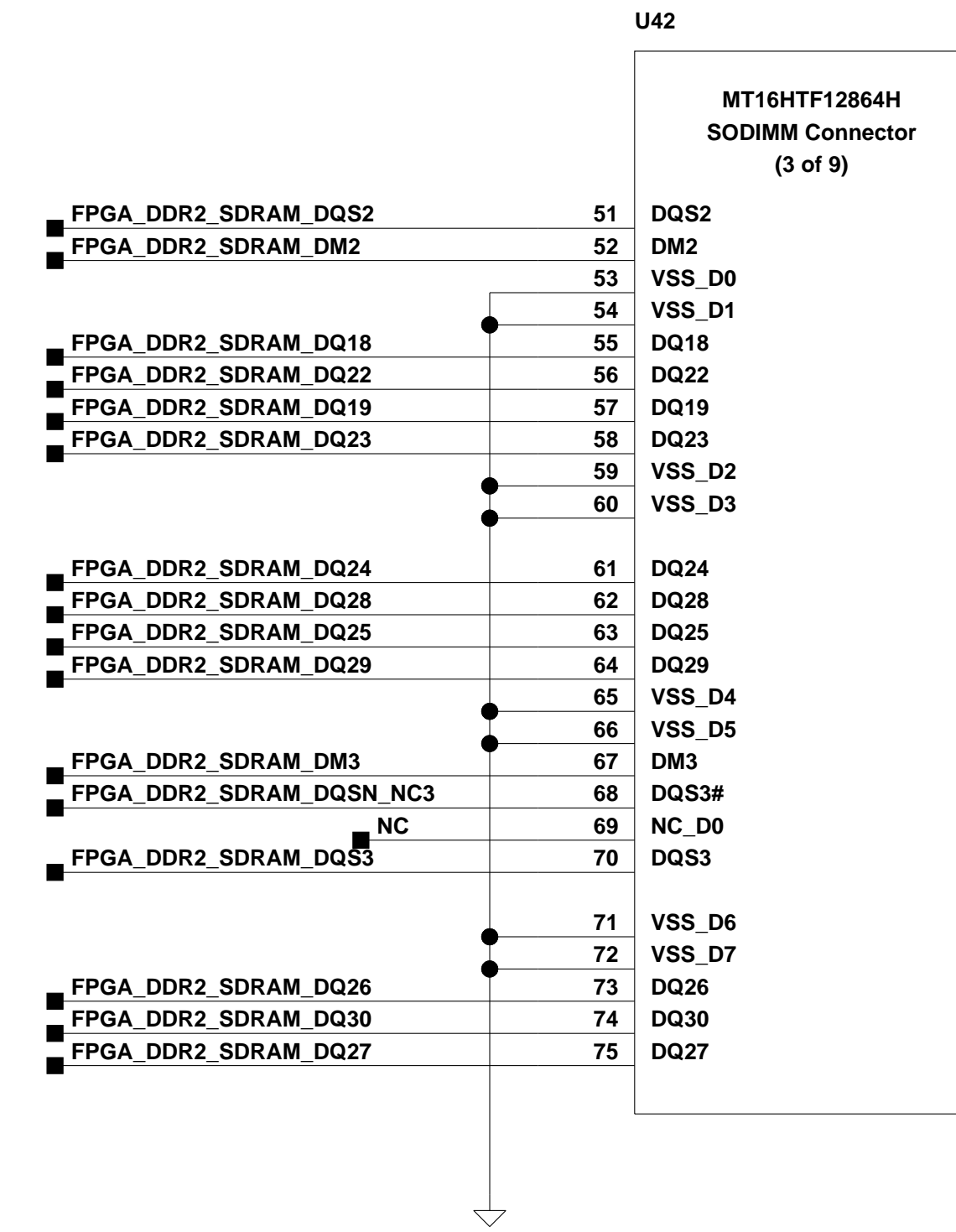
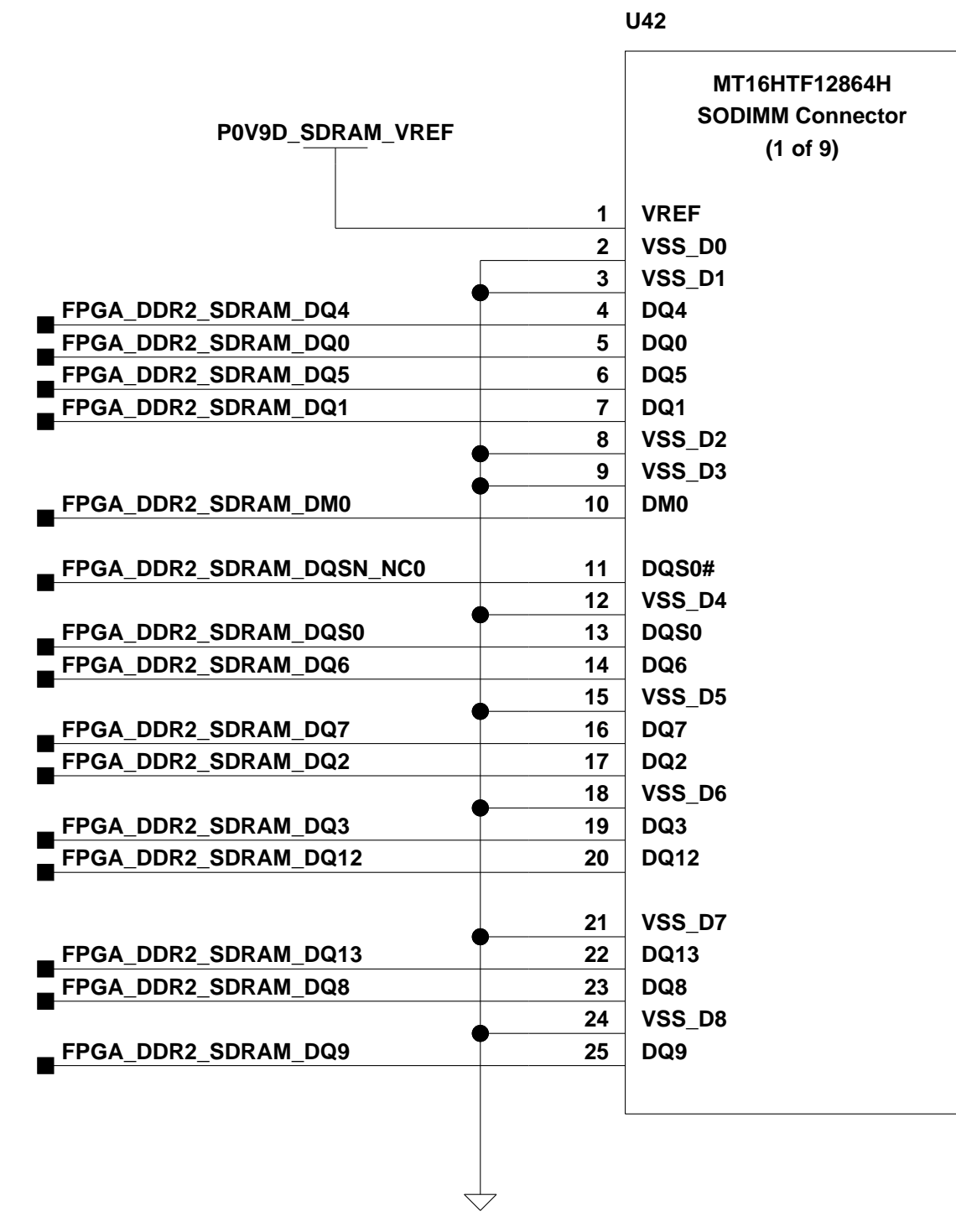
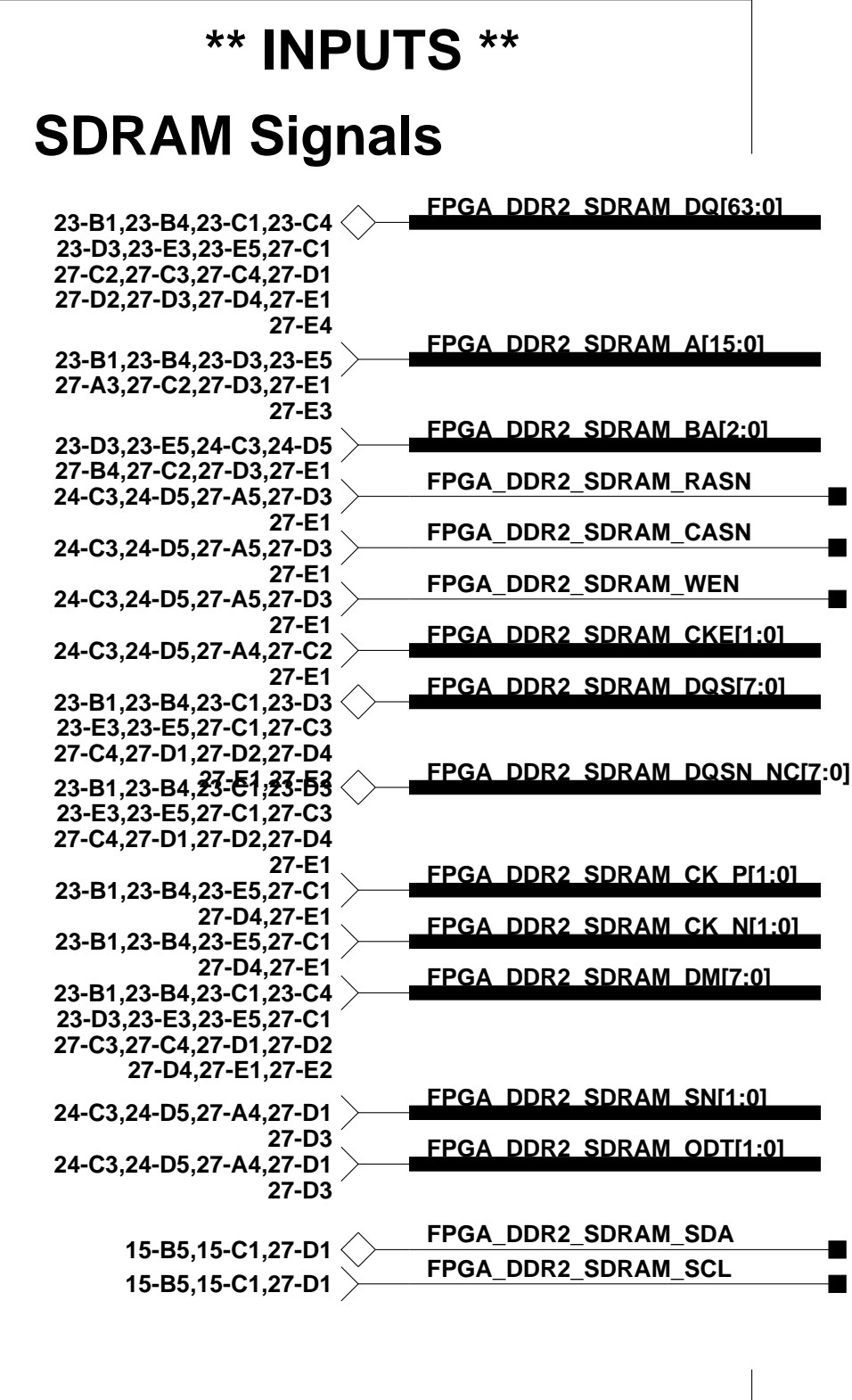


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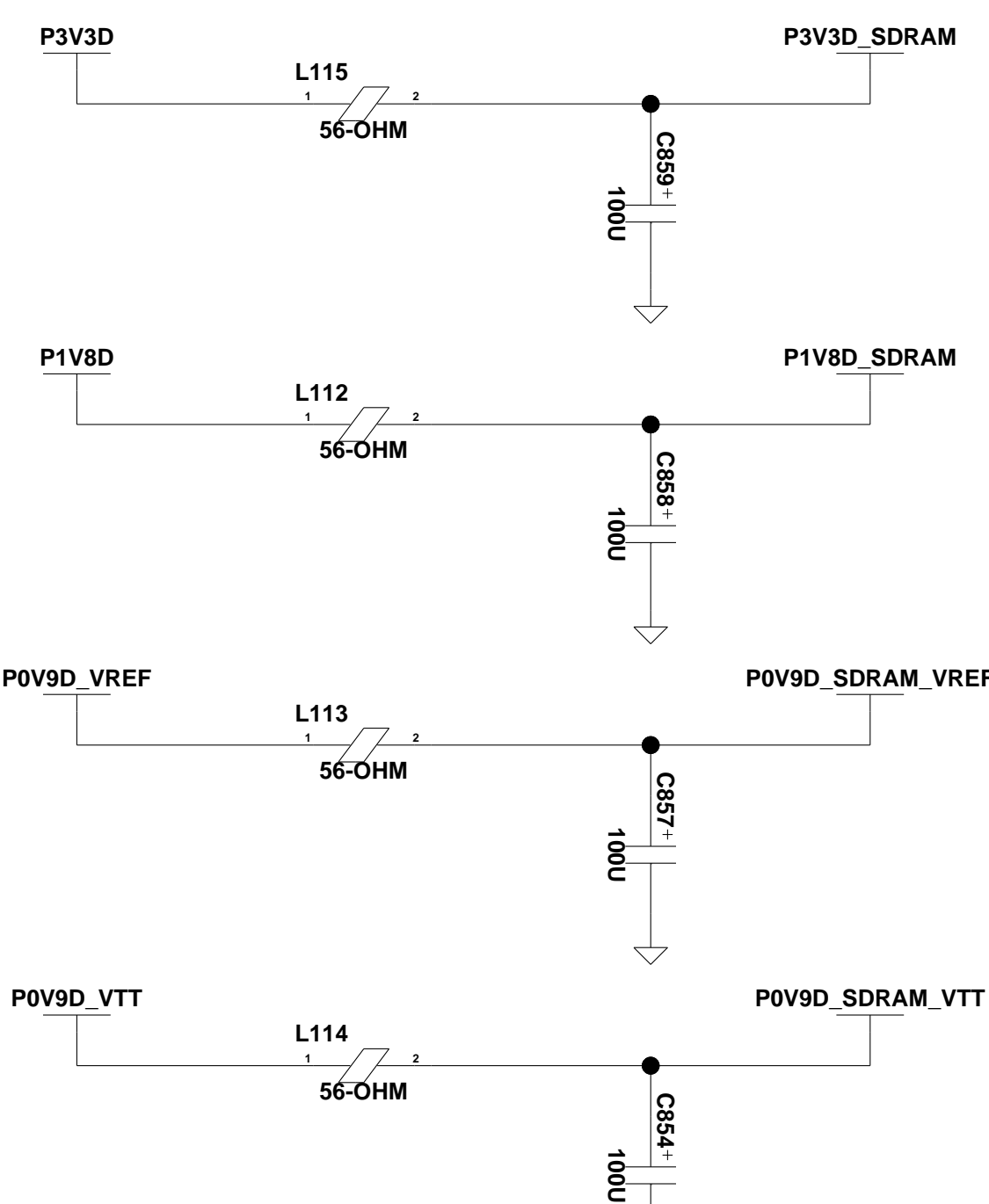
DDR2 SDRAM SODIMM - MT16HTF25664H – 2GB

256 Meg x 64-bits

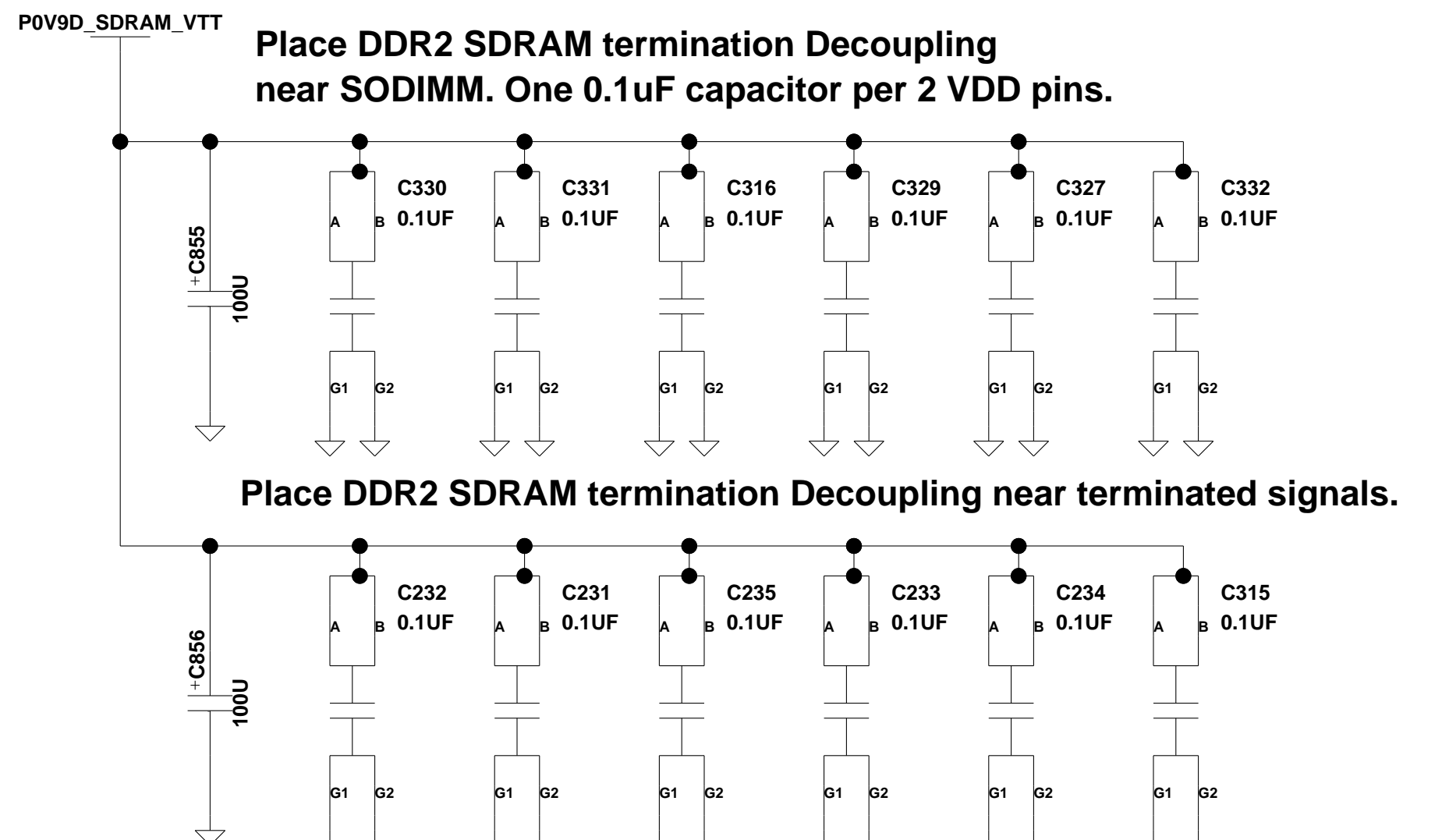
Provides between 1.024 GS and 1.280 GS storage of sampled data.



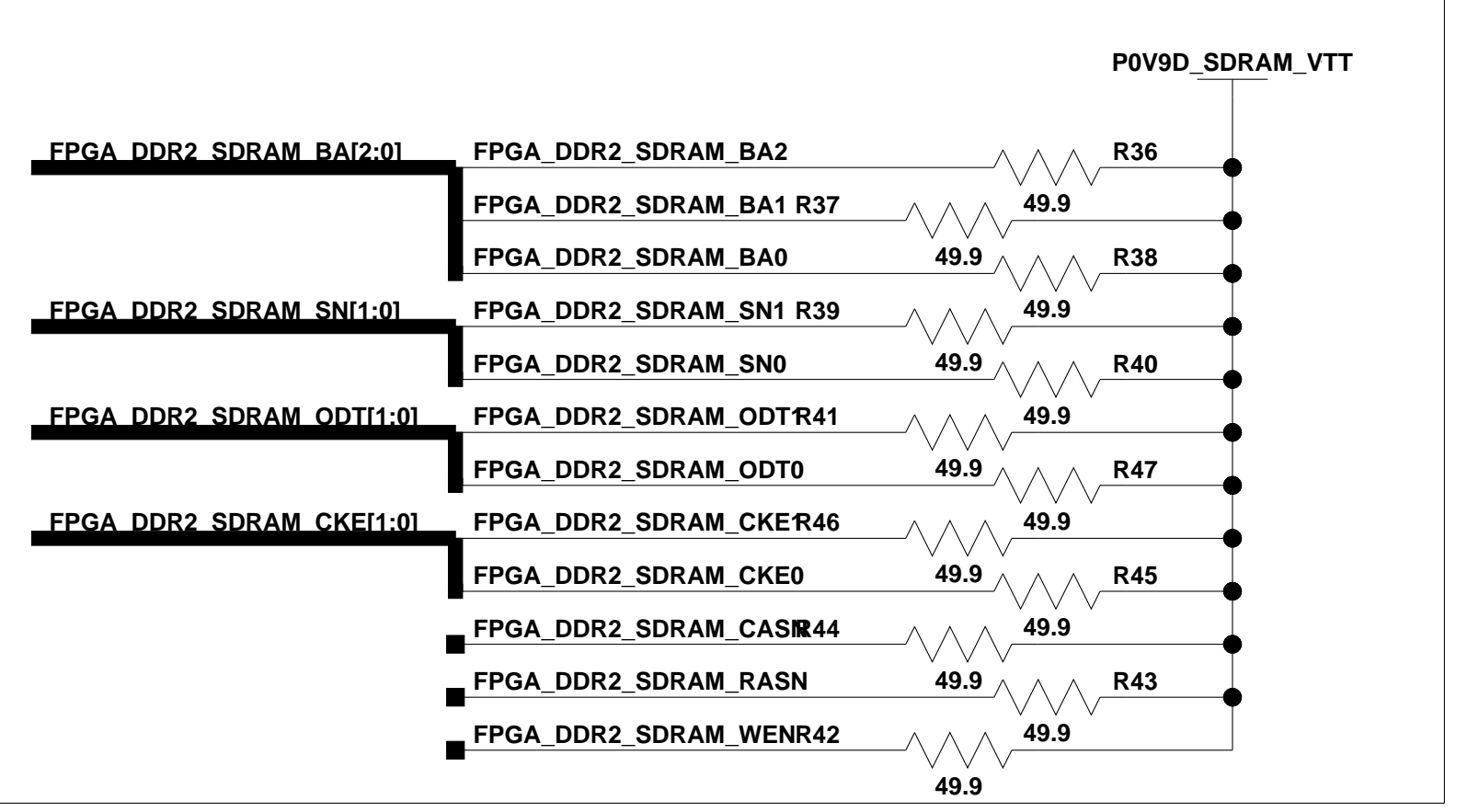
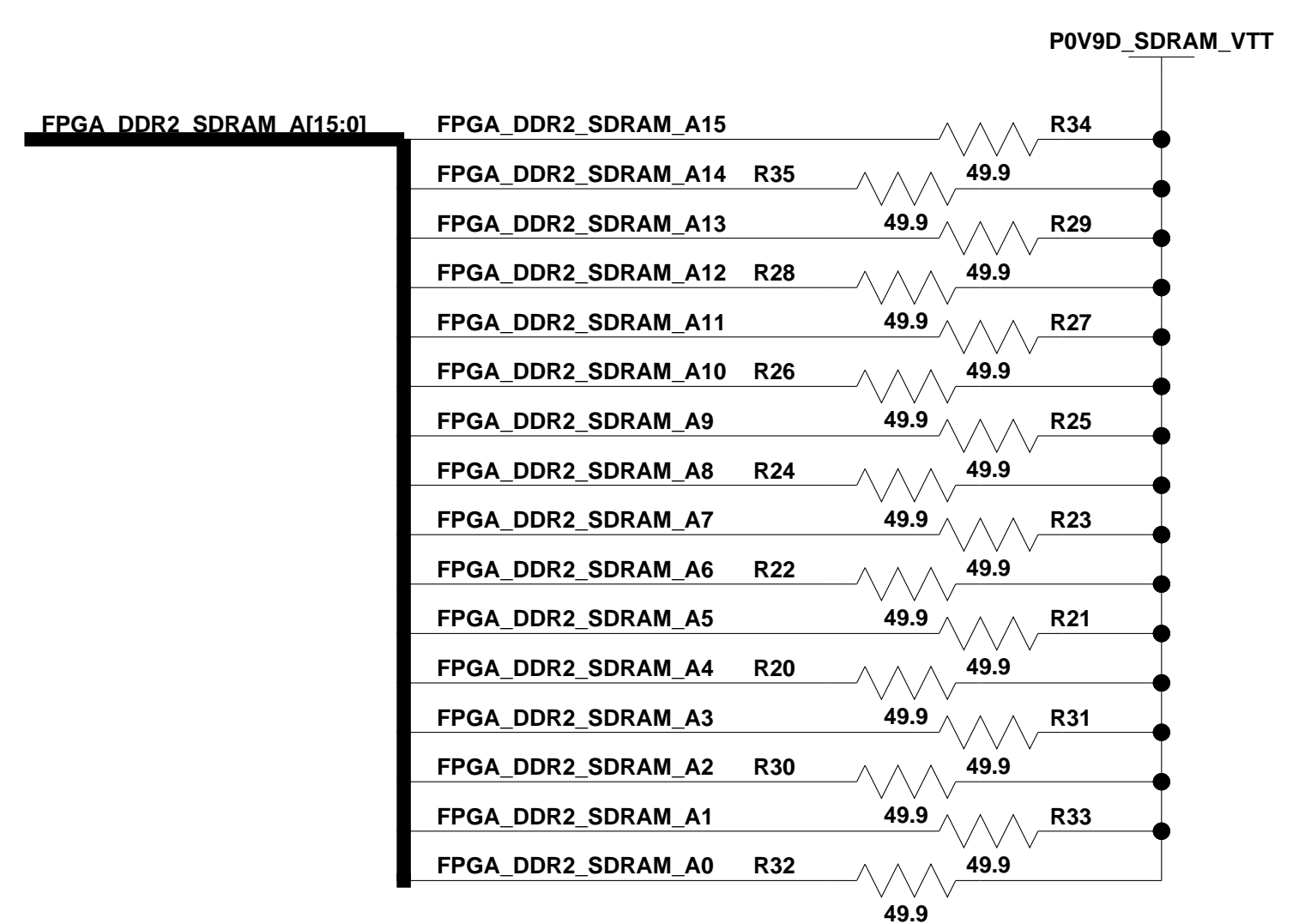
B DDR2 Termination/Power Inputs



C DDR2 Termination Decoupling



D DDR2 Terminations



VLSI Computation LAB

Title: DDR2 SDRAM SODIMM - MT16HTF25664H - 2GB
 File: MEAS_MAIN_BOARD
 Created by: JEREMY W. WEBB
 Modified by: JEREMY W. WEBB
 Date: 4-20-2009 13:35
 Date:
 PCB NO: 342
 Size: E
 Sheet 27 of 43
 REV: 001

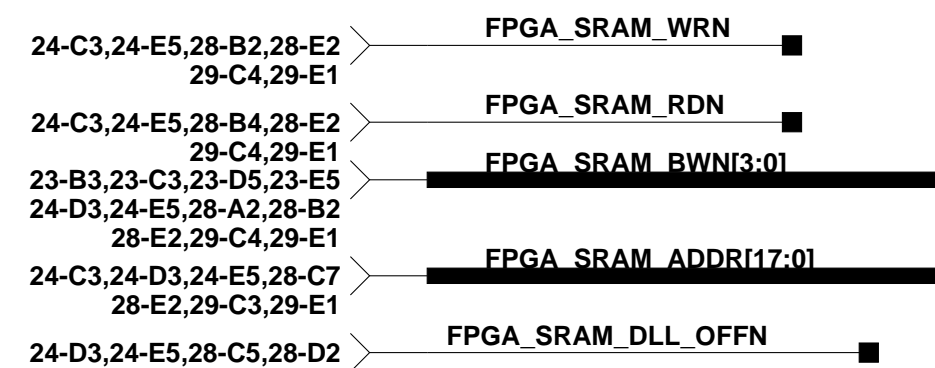
QDR-II SRAM - Address, Data, Control Samsung K7R323684C-EC250

**** INPUTS ****

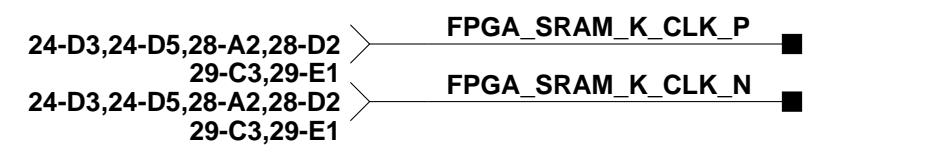
SRAM Write Data



SRAM Control

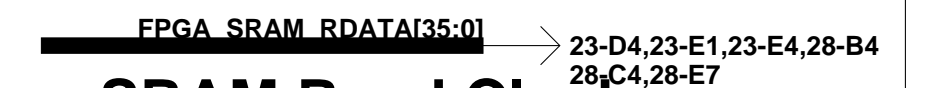


SRAM Clocks

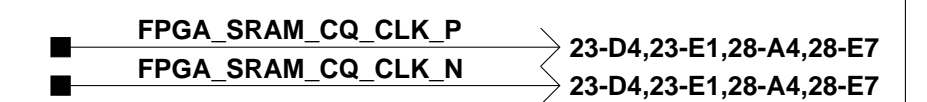


**** OUTPUTS ****

SRAM Read Data

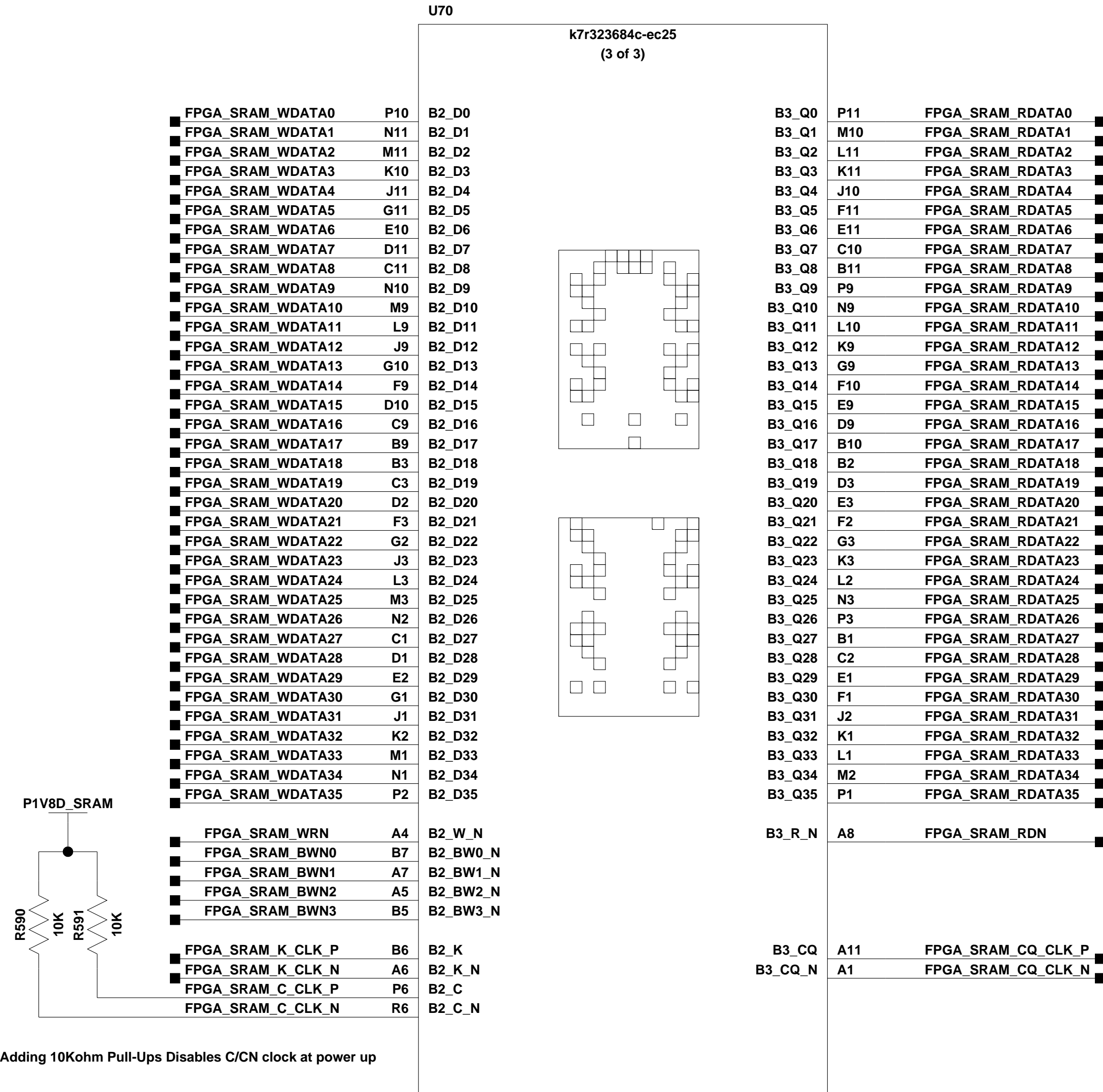


SRAM Read Clock



A QDR-II SRAM Read/Write Data

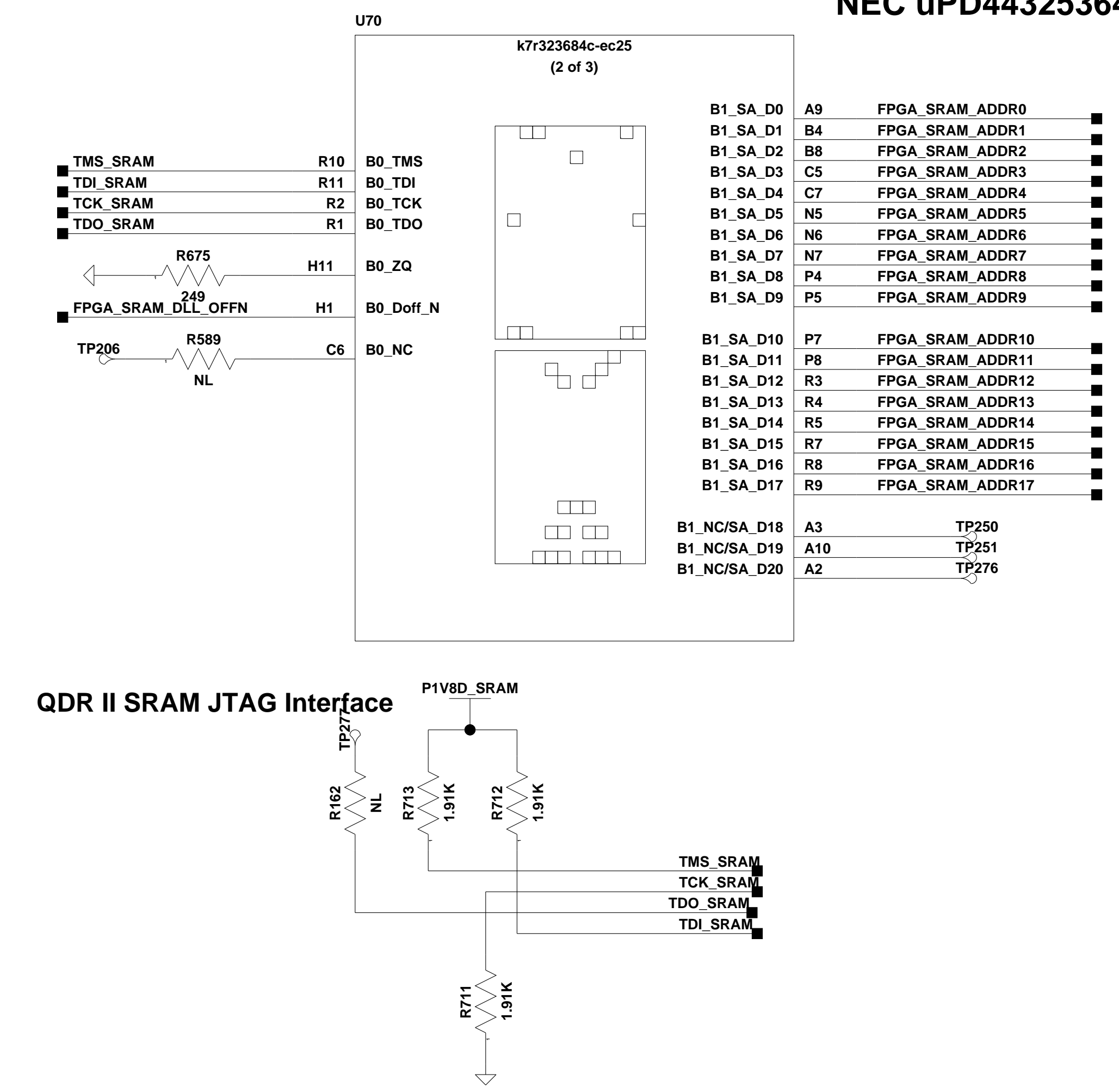
All data, address, clocks must have equal length lines



B QDR-II SRAM Address

Use 0 Ohm Resistors in case we use Cypress CY7C1415AV18, Renesas R1Q3A3636ABG, or NEC uPD44325364F5-E40-EQ2-A

All data, address, clocks must have equal length lines



VLSI Computation LAB

Title:	QDR-II SRAM - ADDRESS, DATA, CONTROL		
File:	MEAS_MAIN_BOARD		
Created by:	JEREMY W. WEBB	Date:	4-20-2009_13:35
Modified by:		Date:	
PCB NO:	342	Size:	D
Sheet	28	of	43
REV:	001		

QDR-II SRAM - Power and Terminations

Samsung K7R323684C-EC250

**** INPUTS ****

SRAM Write Data

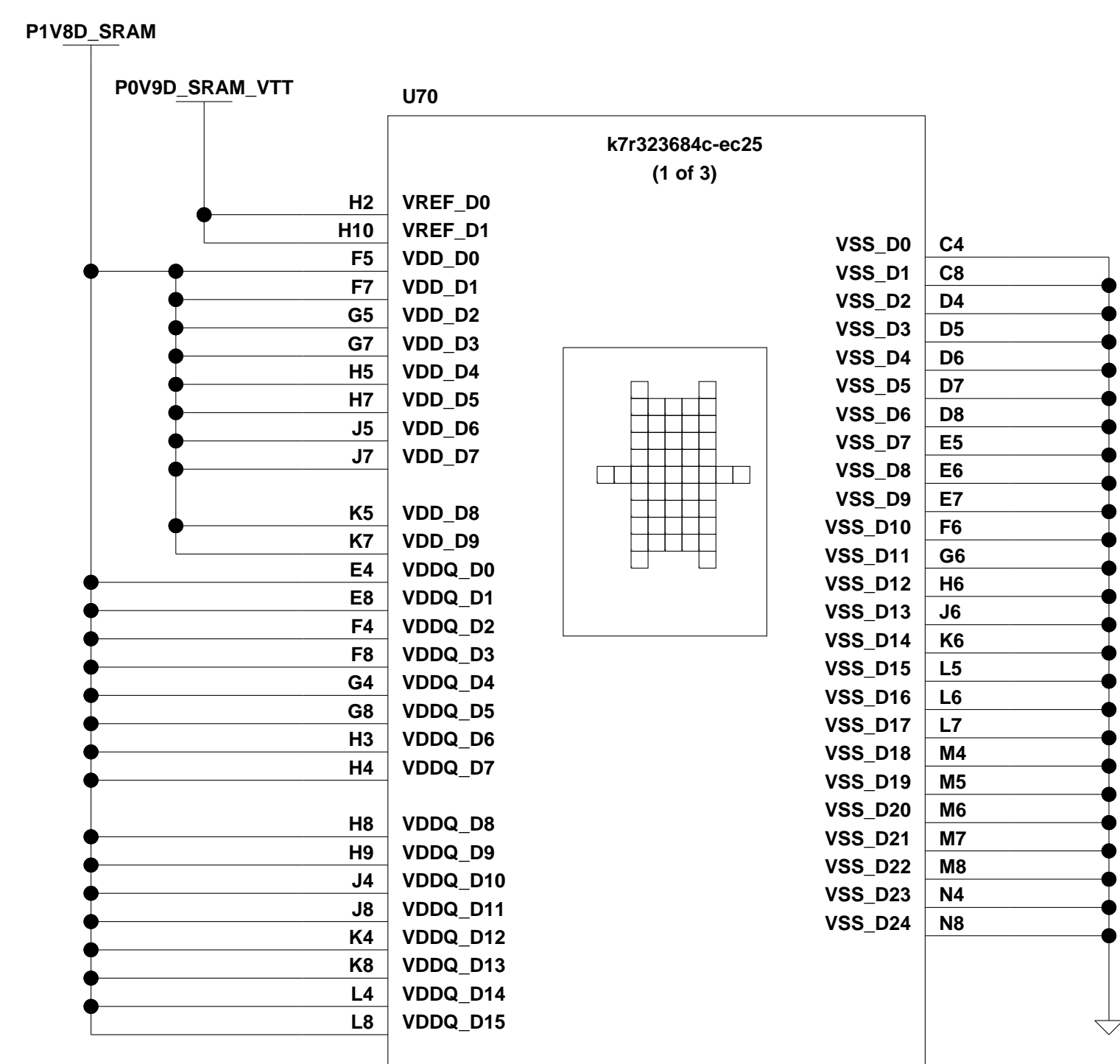
23-B3,23-C3,23-D5,23-E5 → FPGA_SRAM_WDATA[0:255]
 24-D3,24-E5,28-B2,28-C2 → FPGA_SRAM_WDATA[256:511]
 28-E1,28-E2,29-C4,29-E1 → FPGA_SRAM_WDATA[512:767]

SRAM Control

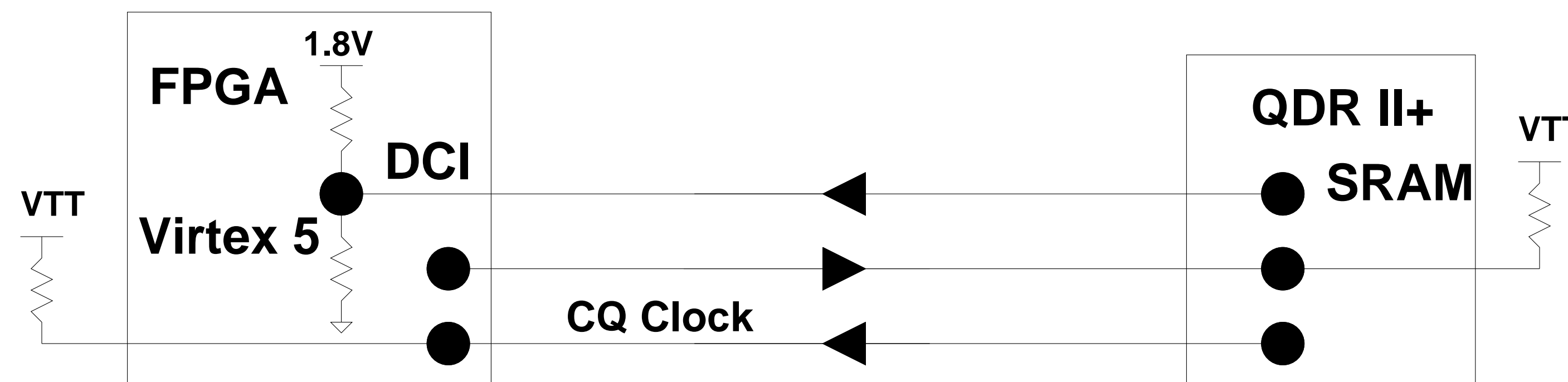
24-C3,24-E5,28-B2,28-E1 → FPGA_SRAM_WRN
 29-E2,29-C4,29-E1 → FPGA_SRAM_RDN
 24-C3,24-E5,28-B4,28-E1 → FPGA_SRAM_BWN[3:0]
 28-E2,29-C4,29-E1 → FPGA_SRAM_ADDR[17:0]

SRAM Clocks

24-D3,24-D5,28-A2,28-D1 → FPGA_SRAM_K_CLK_P
 29-D2,29-C3,29-E1 → FPGA_SRAM_K_CLK_N
 24-D3,24-D5,28-A2,28-D1 → FPGA_SRAM_C_CLK_P
 28-D2,29-C3,29-E1 → FPGA_SRAM_C_CLK_N
 29-C4,29-D1 → FPGA_SRAM_C_CLK_P
 29-B4,29-D1 → FPGA_SRAM_C_CLK_N

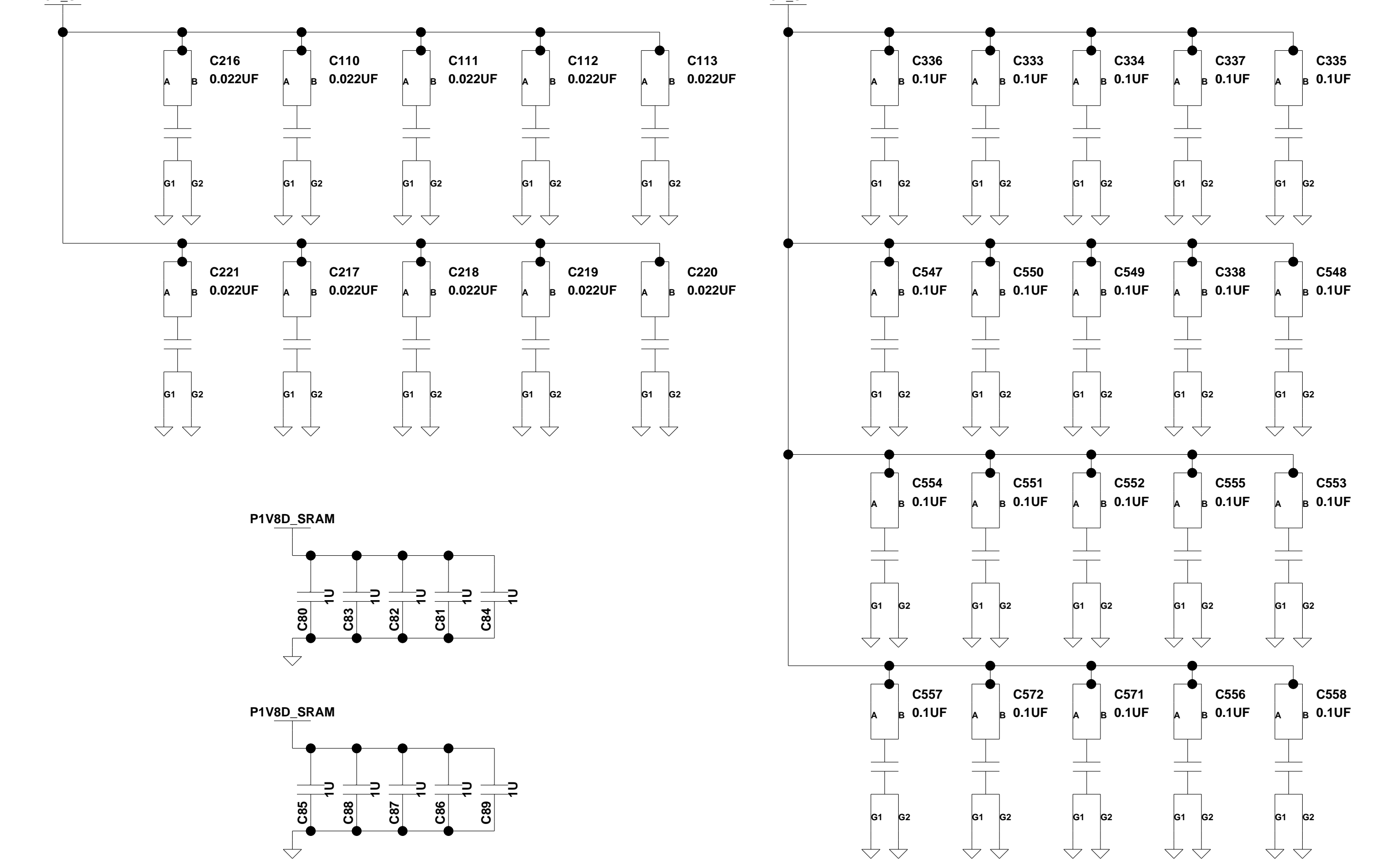


SRAM Termination Placement:
Place parallel terminations just beyond the SRAM and FPGA.

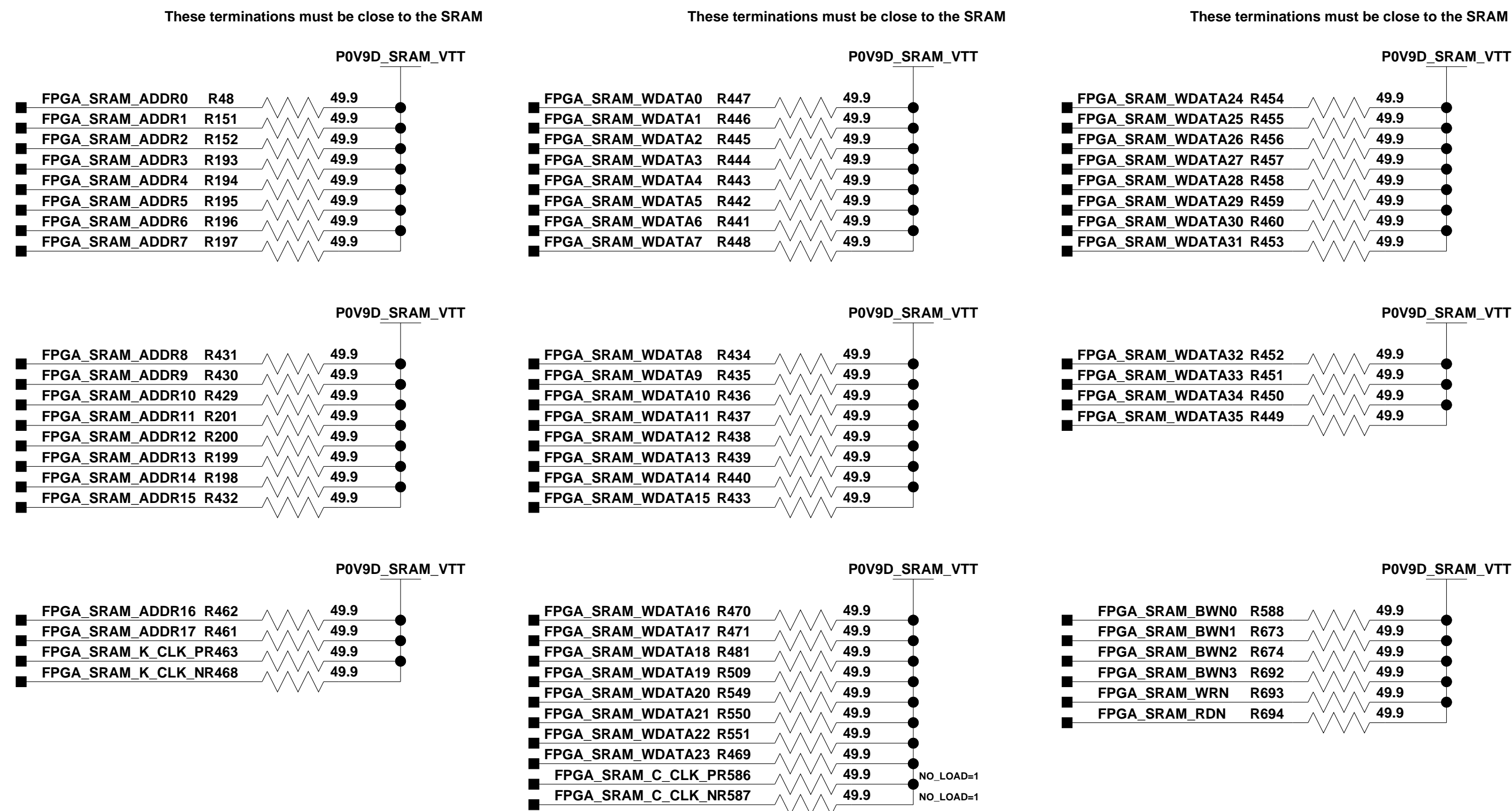


A QDR-II SRAM Decoupling

Place close to QDR II SRAM Power Pins

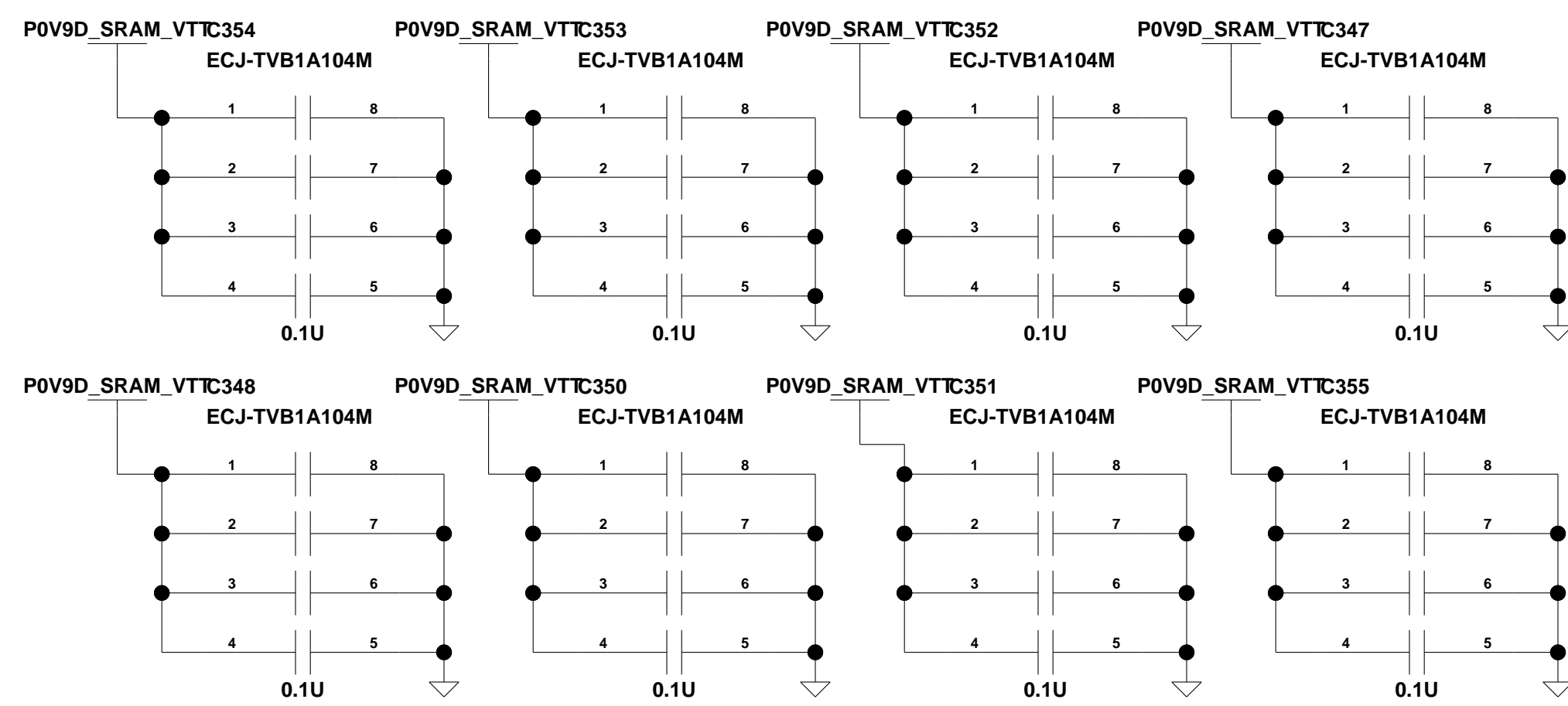


C QDR-II SRAM Write Data, Address Terminations

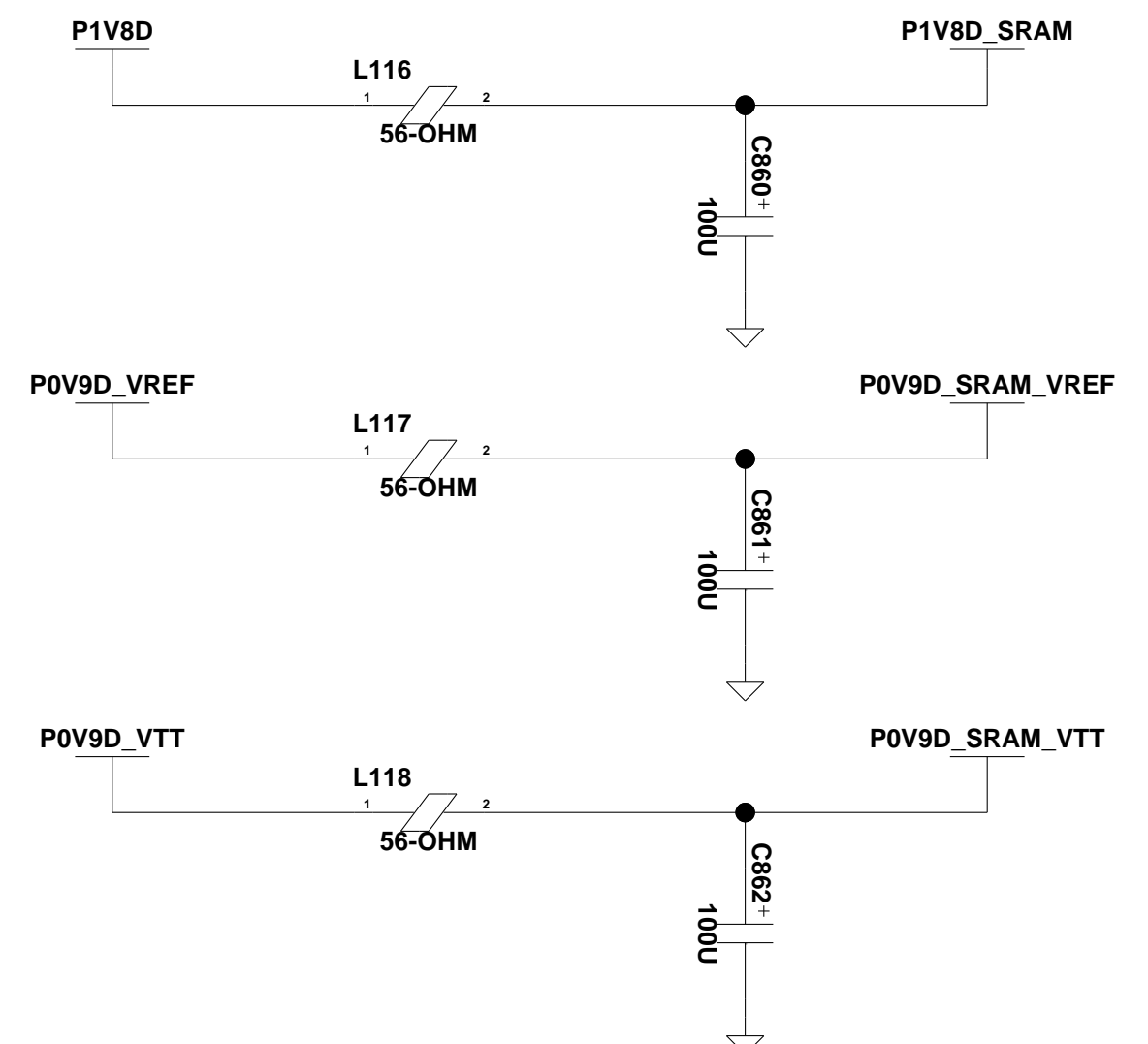


SRAM Read Data and CQ Clock are terminated at Virtex 5 FPGA using DCI HSTL_I_DCI_18.

B QDR-II SRAM Termination Decoupling



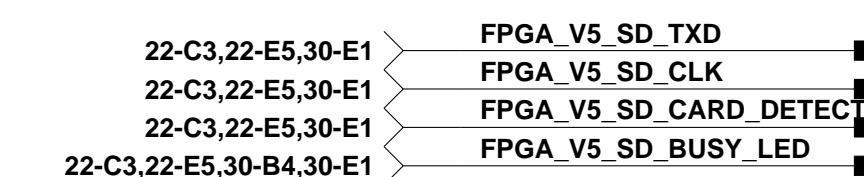
D QDR-II Power Inputs



Xilinx Virtex-5 SX50T FPGA Peripherals

**** INPUTS ****

MicroSD Interface



USB to RS-232



FT245BL USB Interface



Logic Analyzer



**** OUTPUTS ****

USB to RS-232 Interface



Debug LEDs



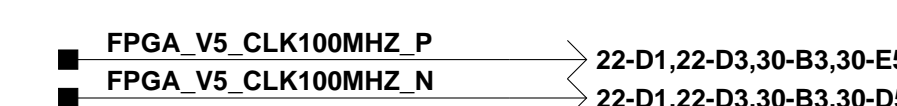
Debug Push Buttons



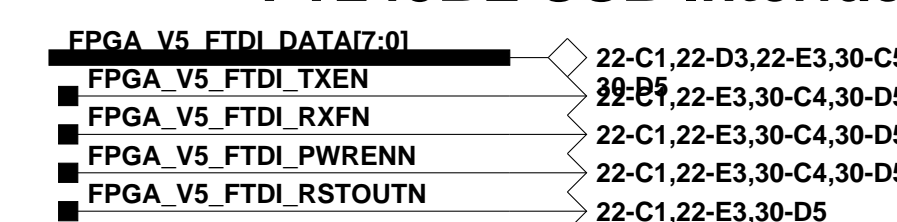
MicroSD Interface



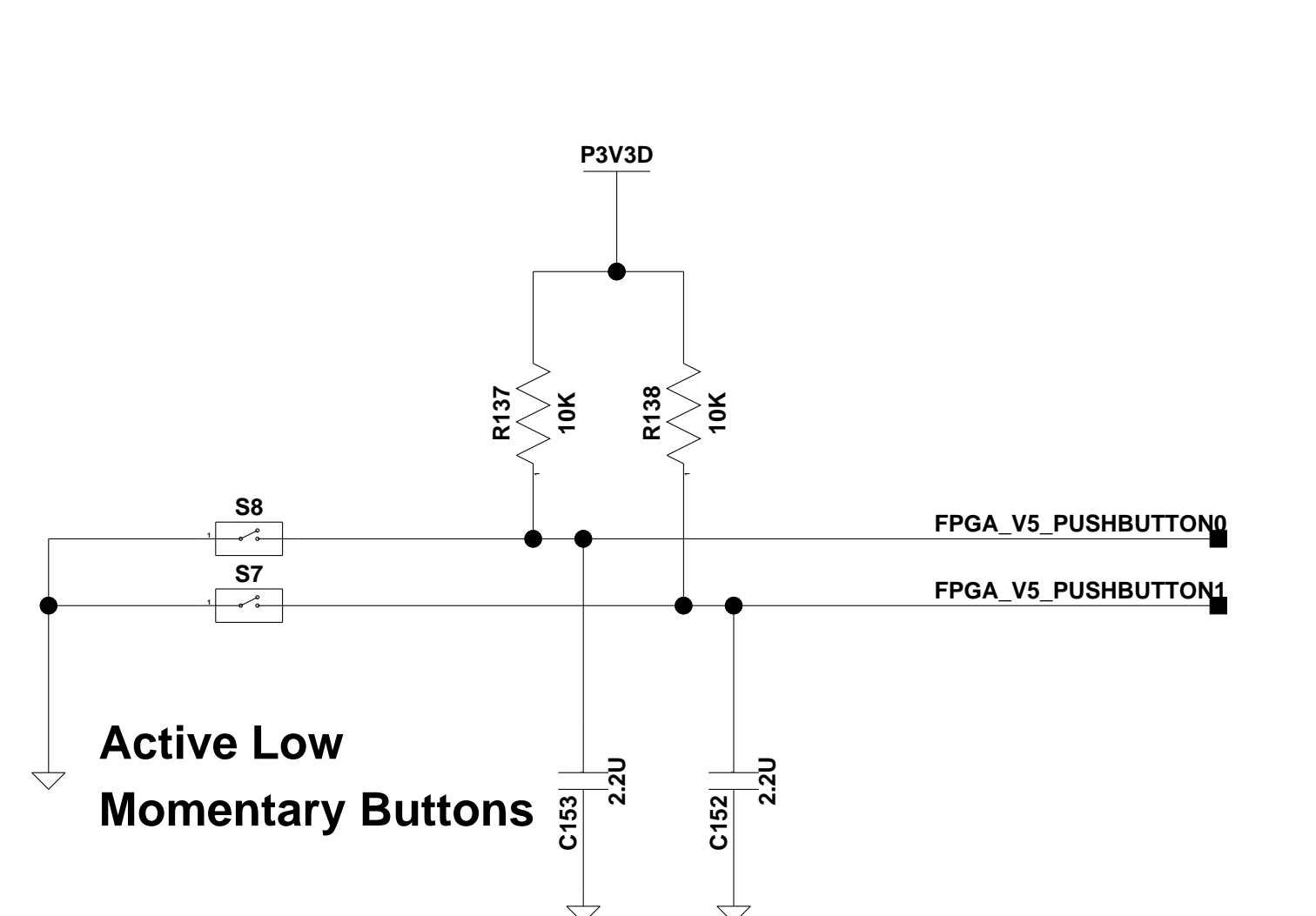
100MHz FPGA Clock



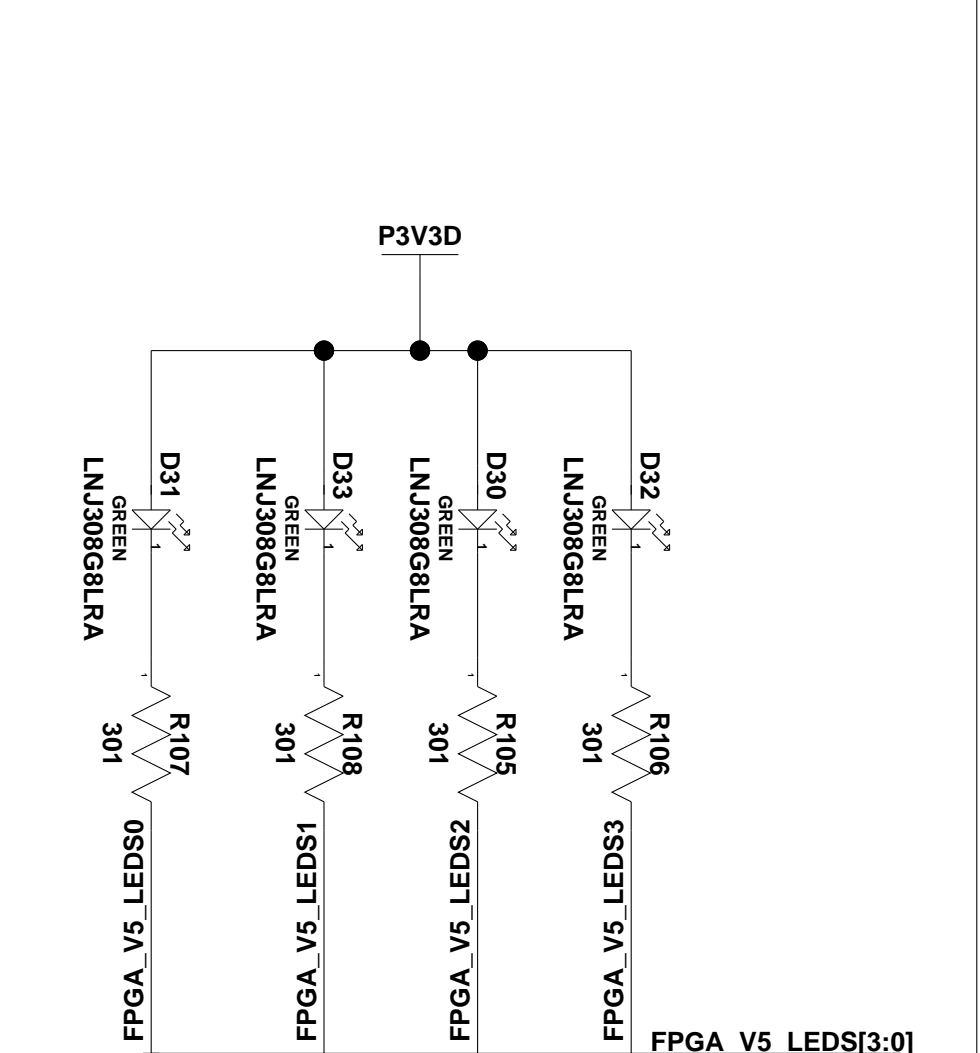
FT245BL USB Interface



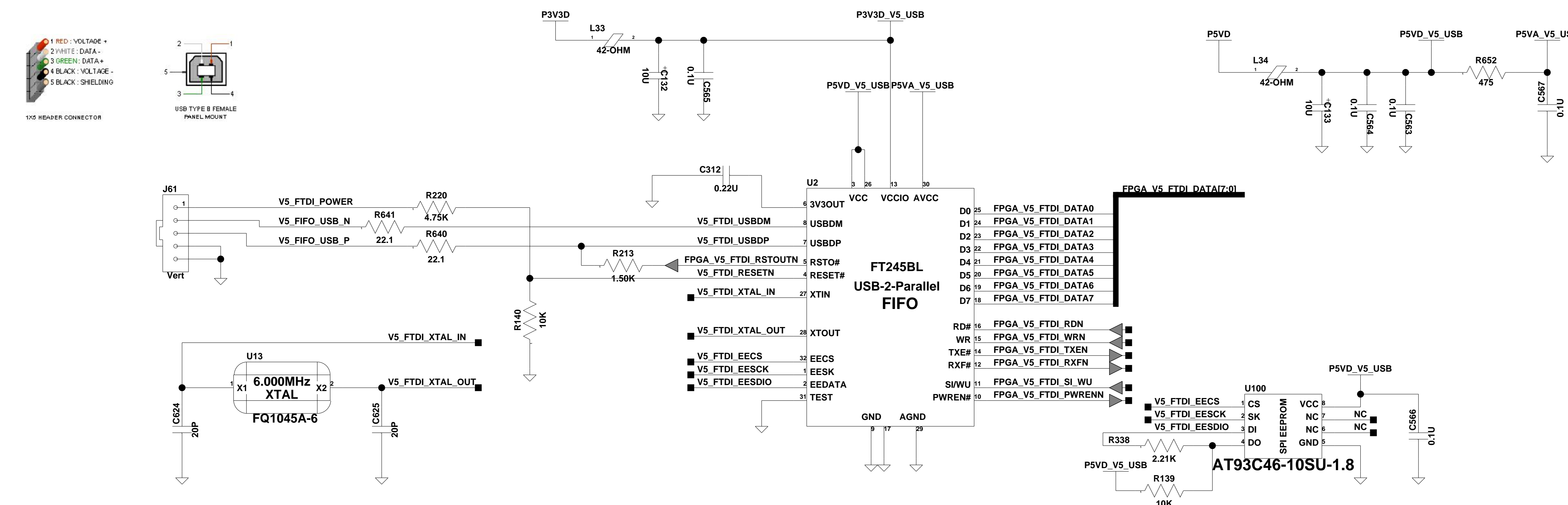
A PUSH-BUTTONS



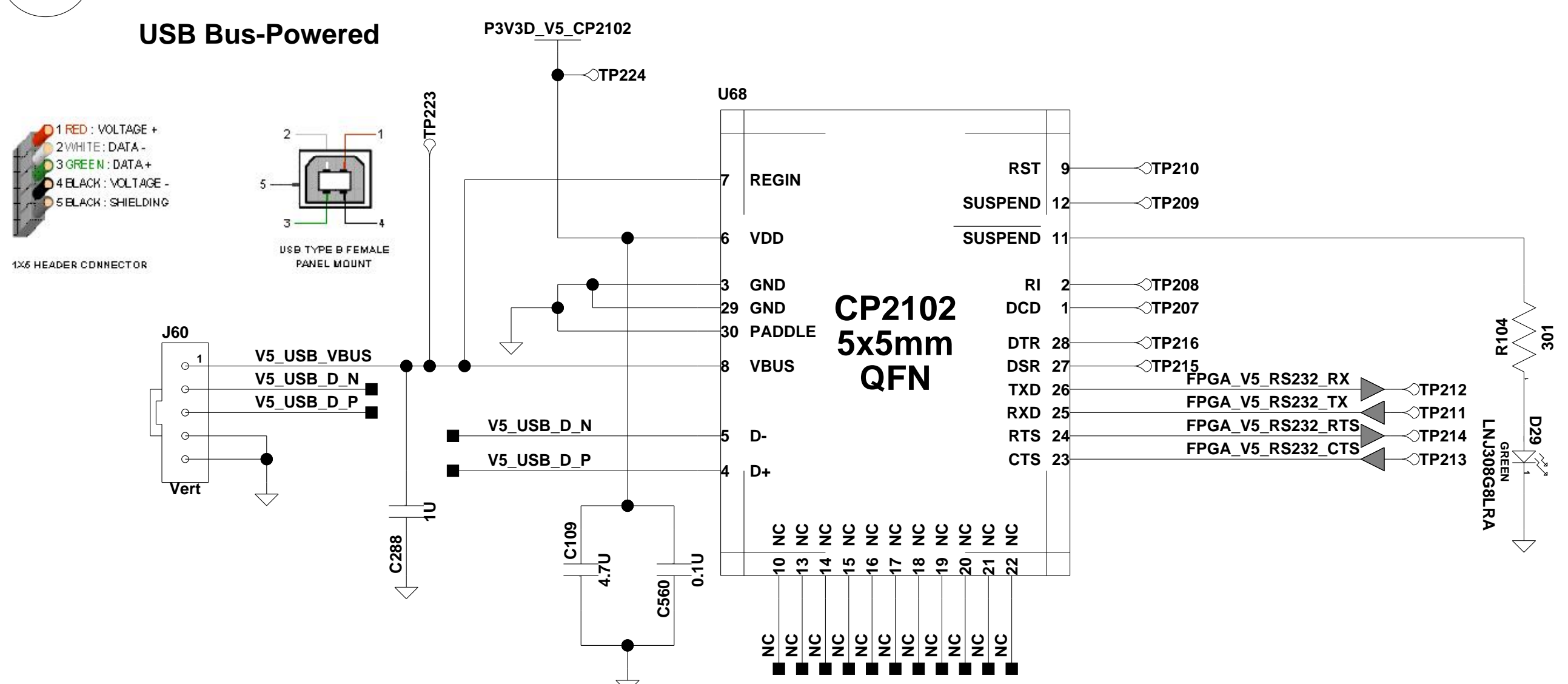
B DEBUG LEDs



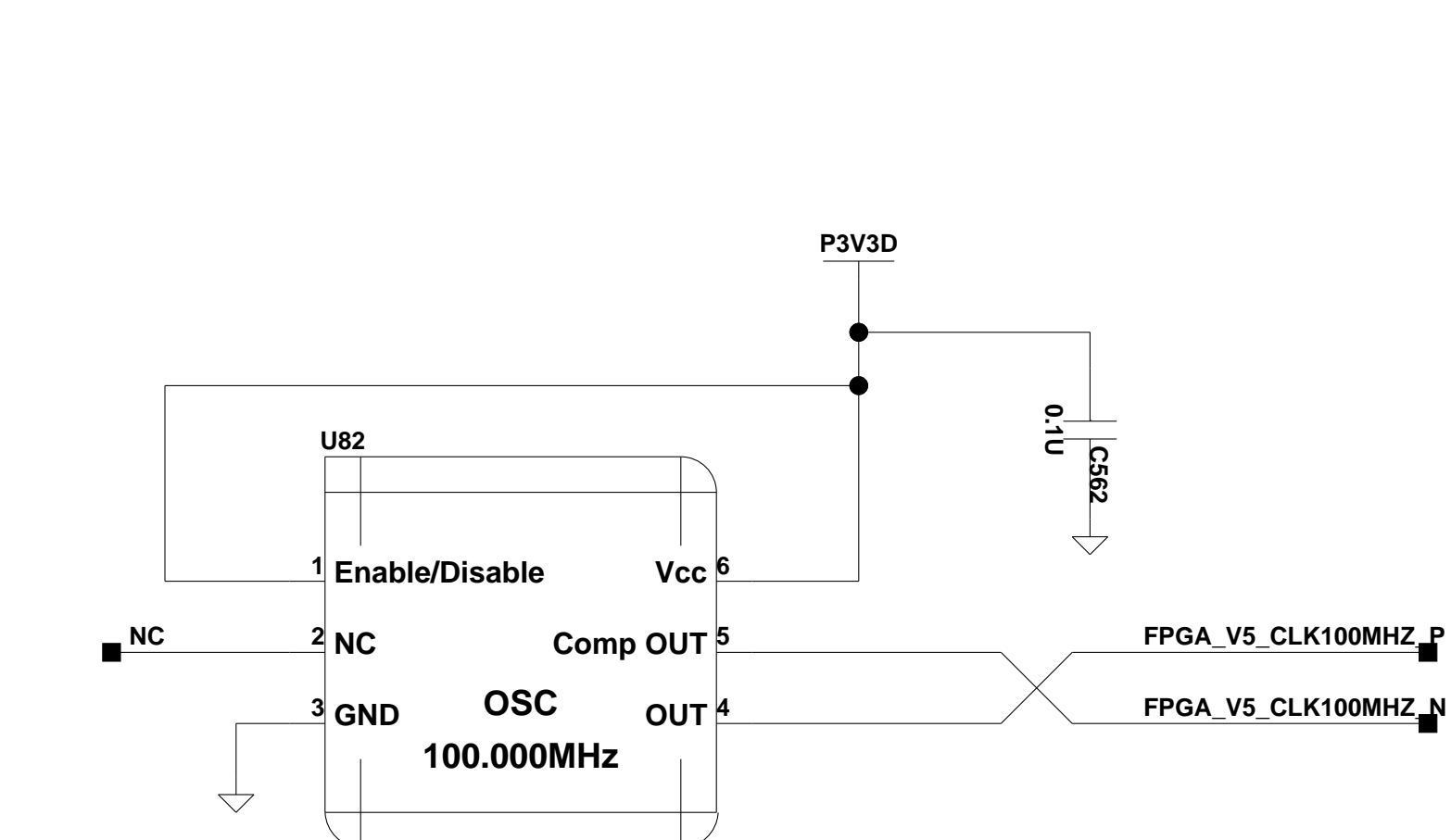
C USB Type-B Peripheral (Back-Up)



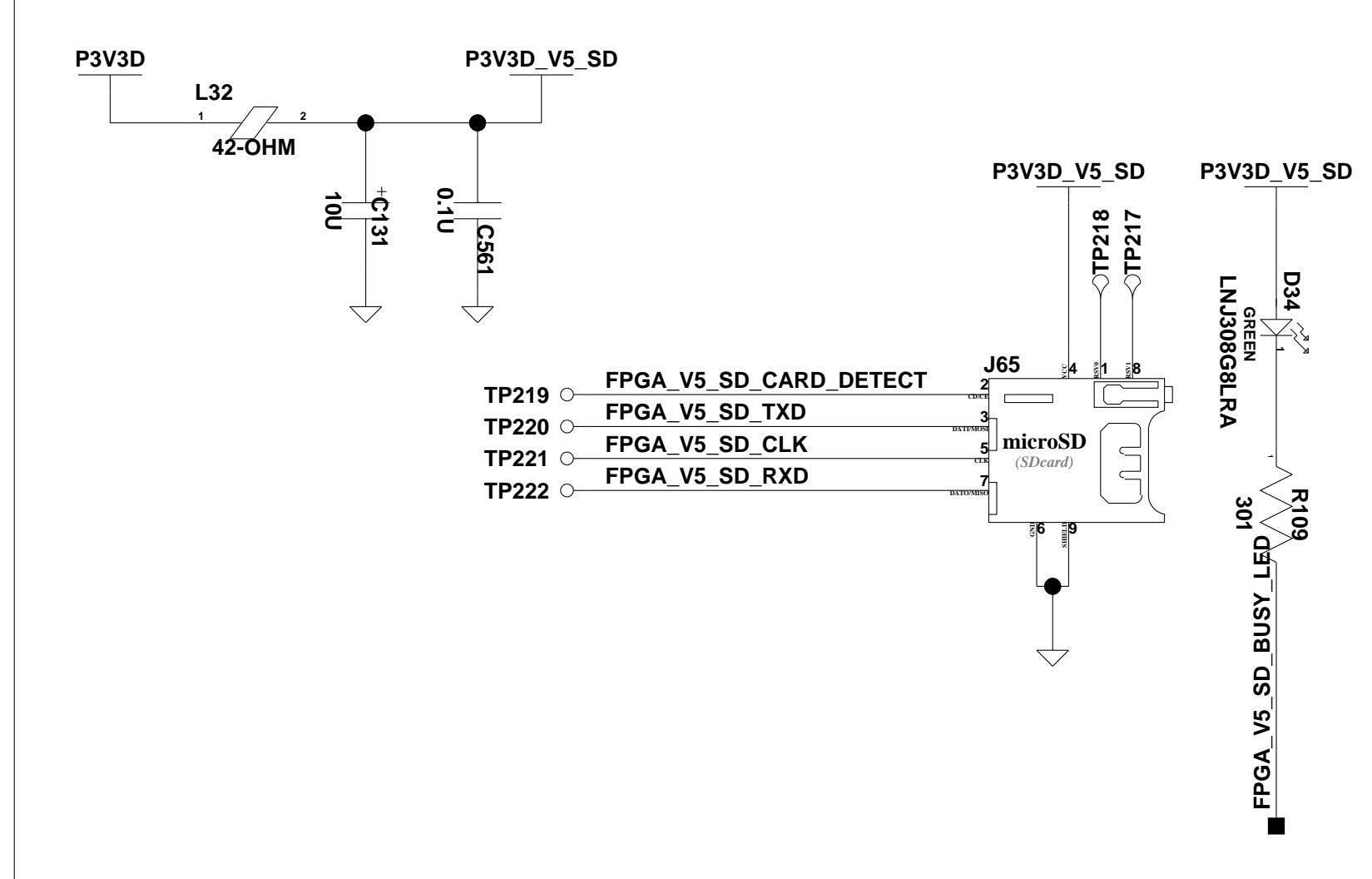
D USB-to-RS-232 Debug Interface



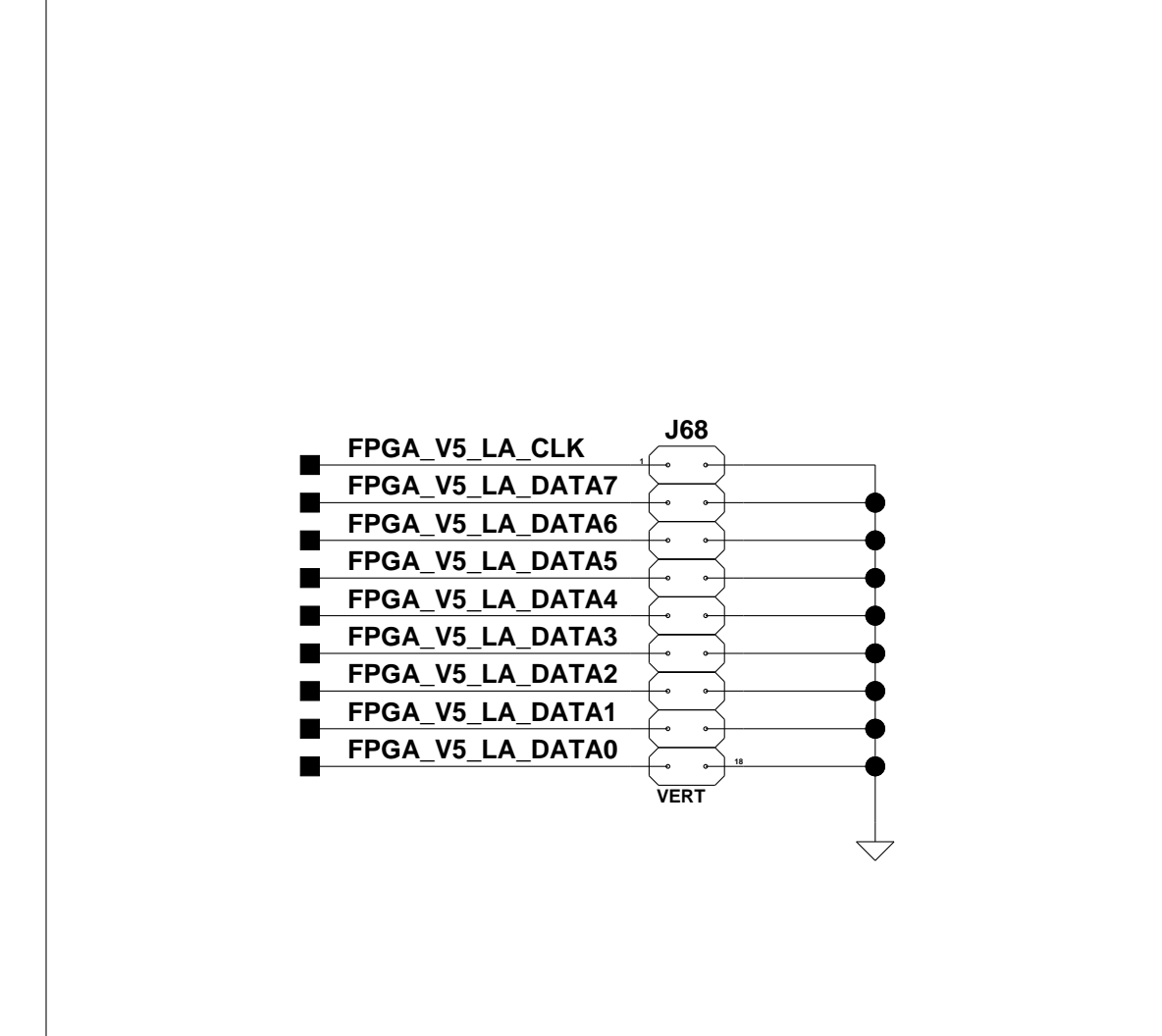
E 100MHz Digital Clock



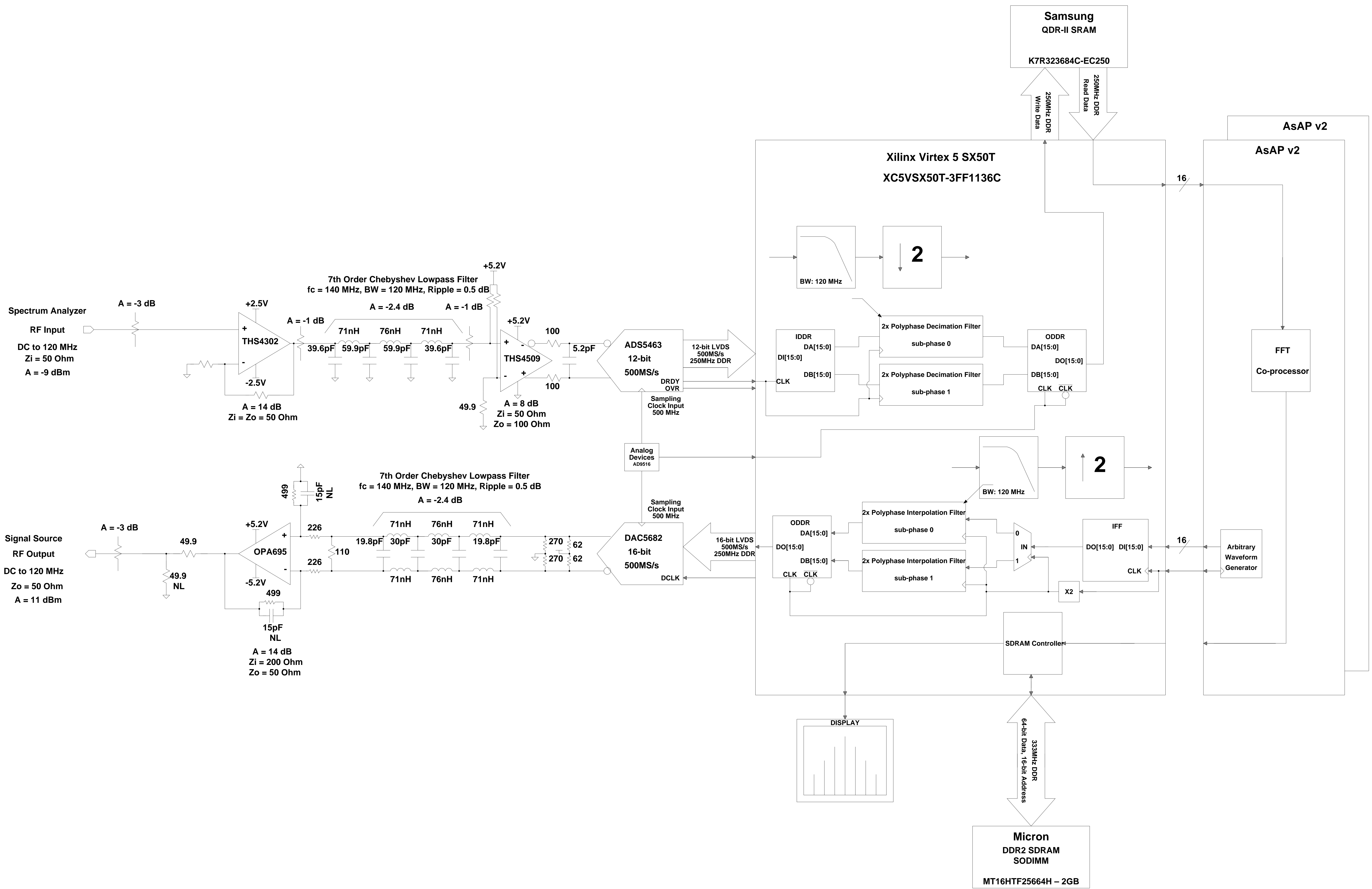
F micro SD Card (2GB)



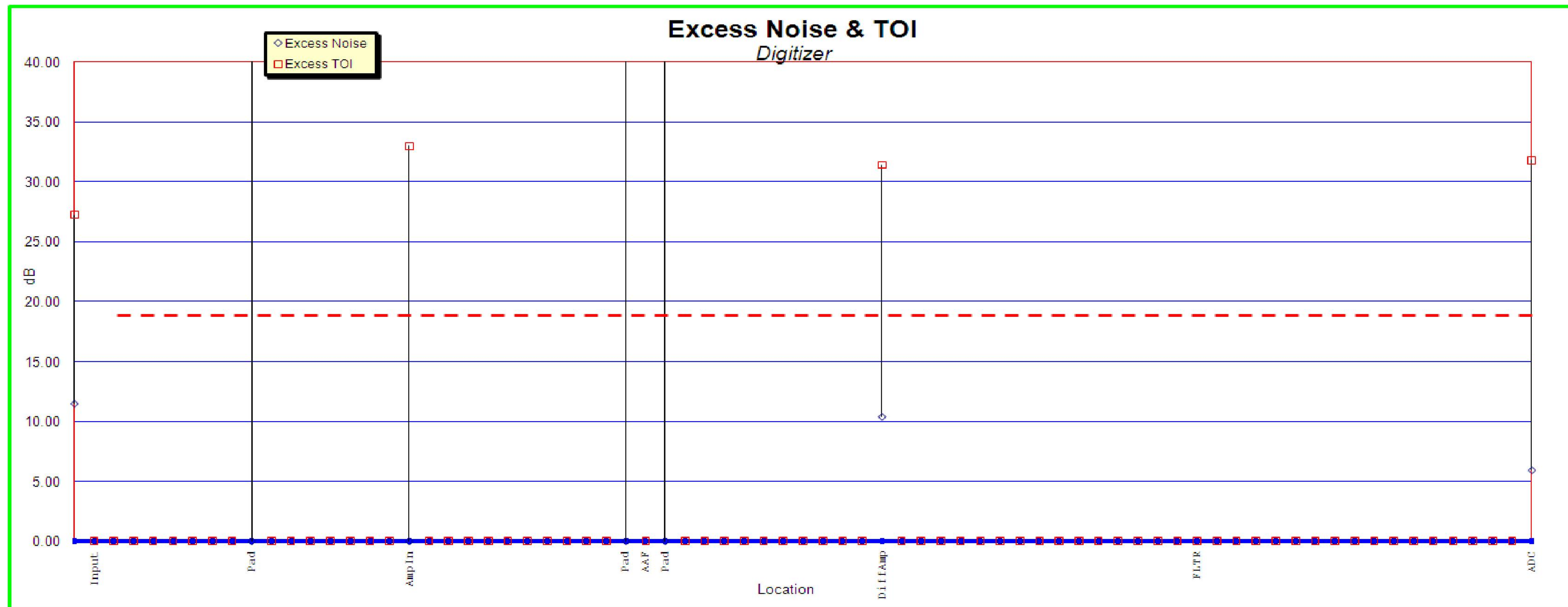
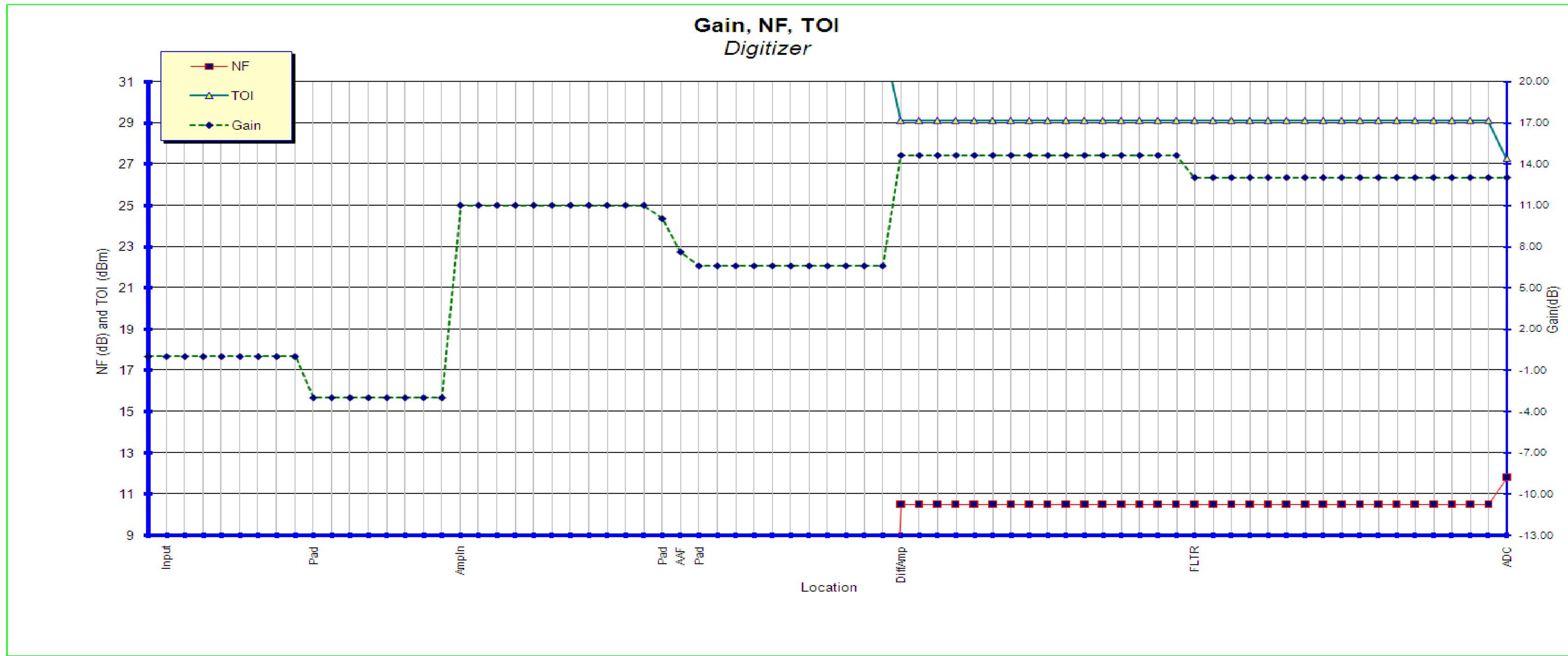
G LA HEADER



Spectrum Analyzer IF and Signal Source Block Diagrams

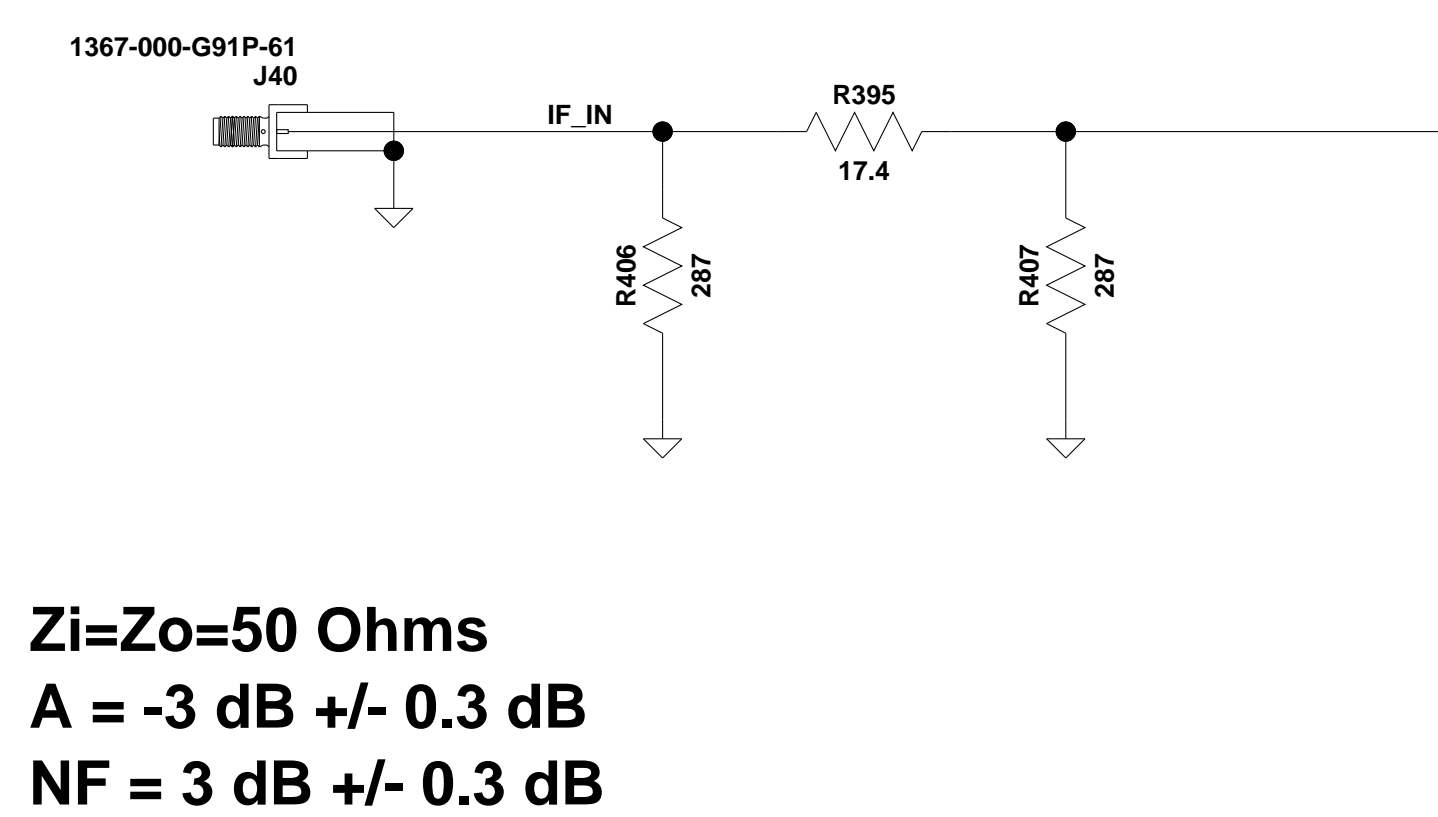


Spectrum Analyzer IF Estimated Performance



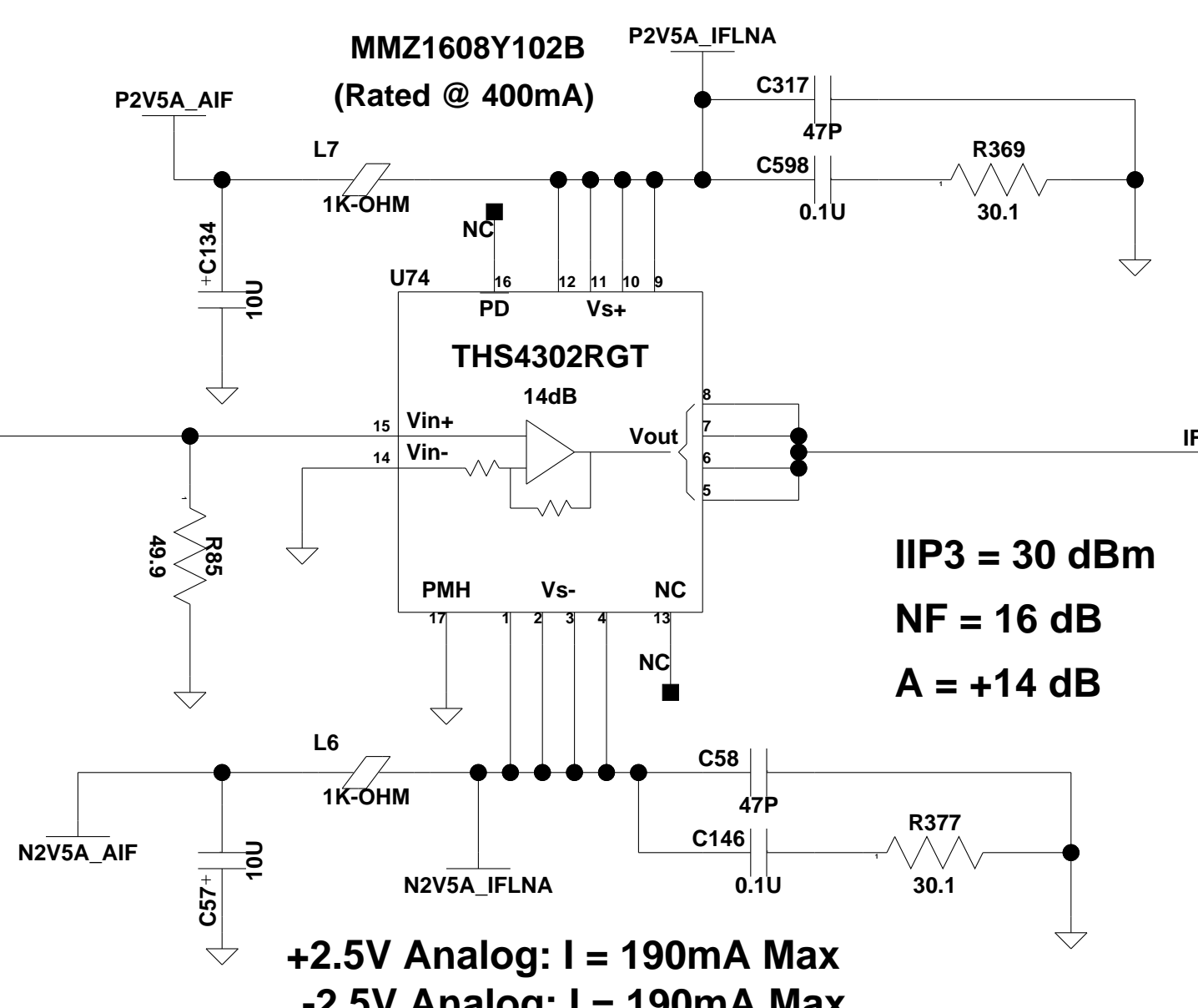
SPECTRUM ANALYZER IF

A 3dB Pad



Zi=Zo=50 Ohms
A = -3 dB +/- 0.3 dB
NF = 3 dB +/- 0.3 dB

B LNA (+14 dBm)

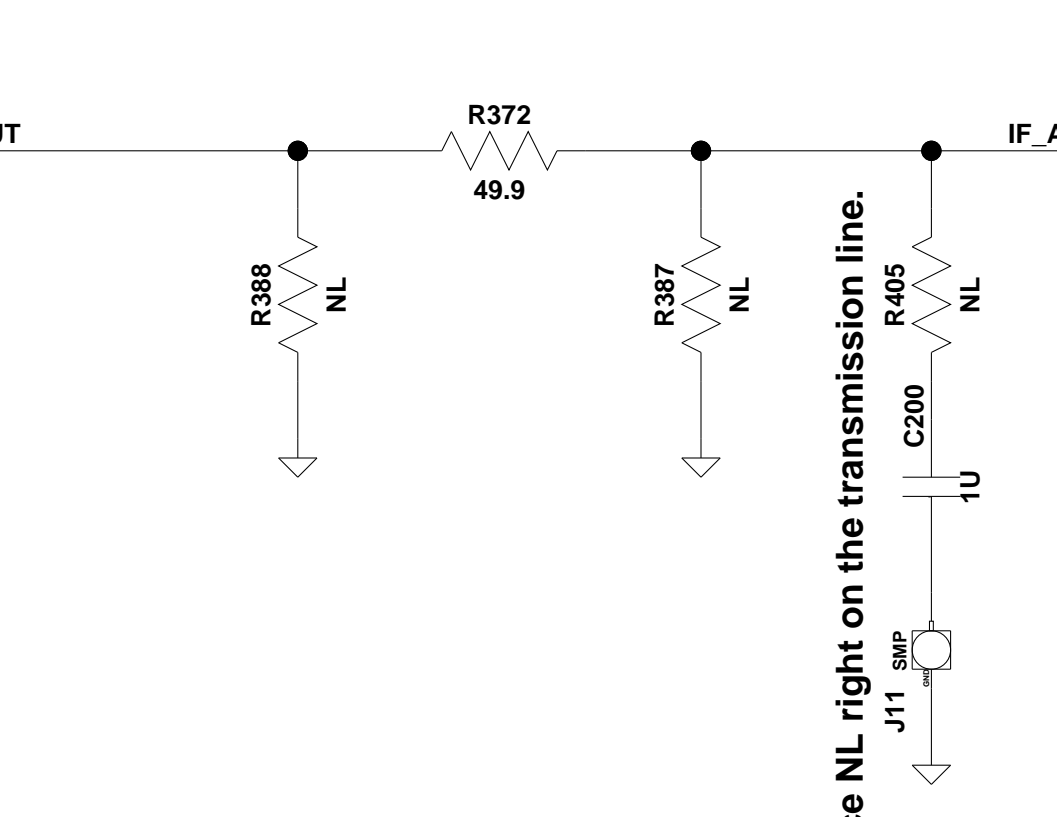


IIP3 = 30 dBm
NF = 16 dB
A = +14 dB

+2.5V Analog: I = 190mA Max
-2.5V Analog: I = 190mA Max

C 1dB PAD

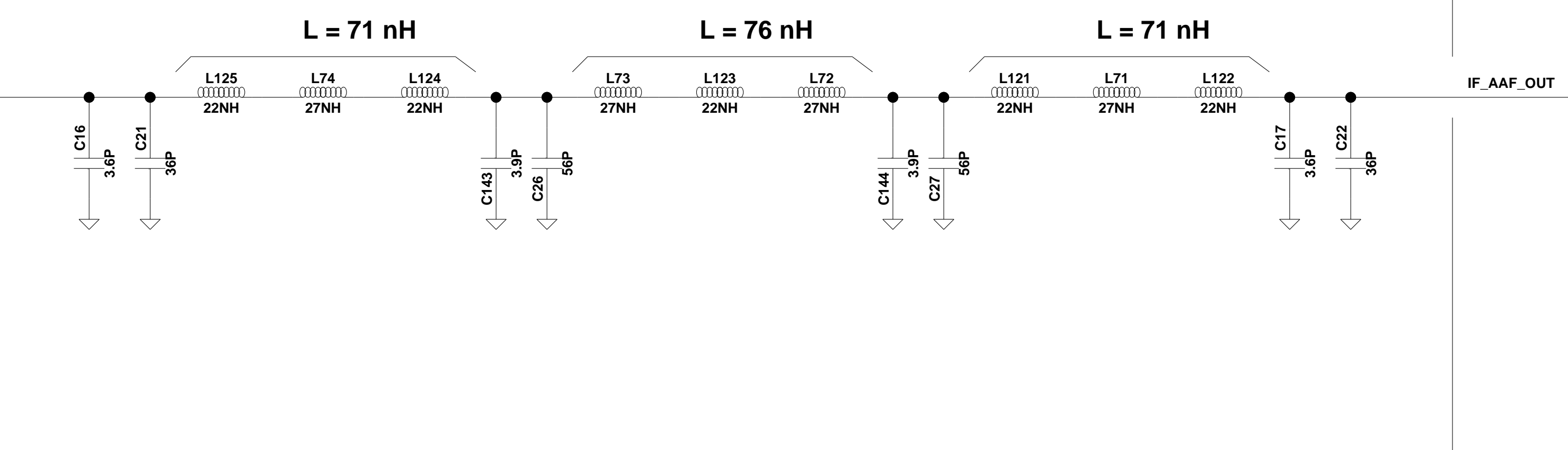
Zi=Zo=50 Ohms
A = -1 dB +/- 0.3 dB
NF = 1 dB +/- 0.3 dB



Place NL right on the transmission line.

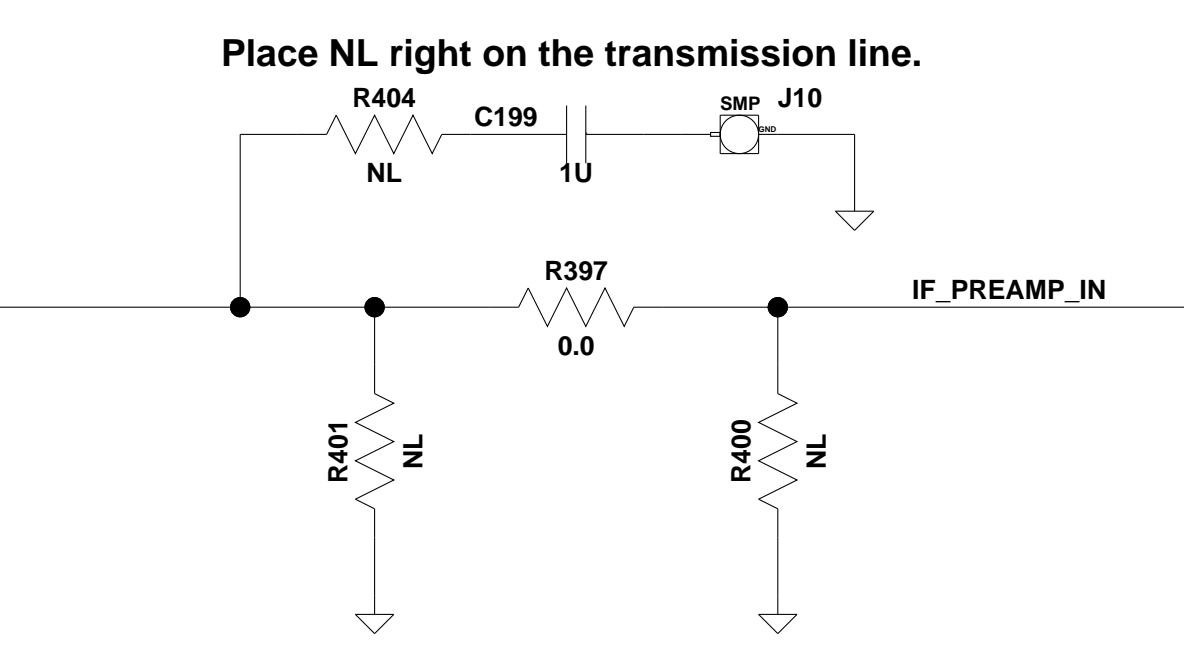
D Anti-Alias Filter

7th order Chebyshev Lowpass Filter
fc = 140 MHz, BW = 120 MHz, and Ripple = 0.5 dB
A = -2.4 dB
NF = 2.4 dB



E 1dB PAD

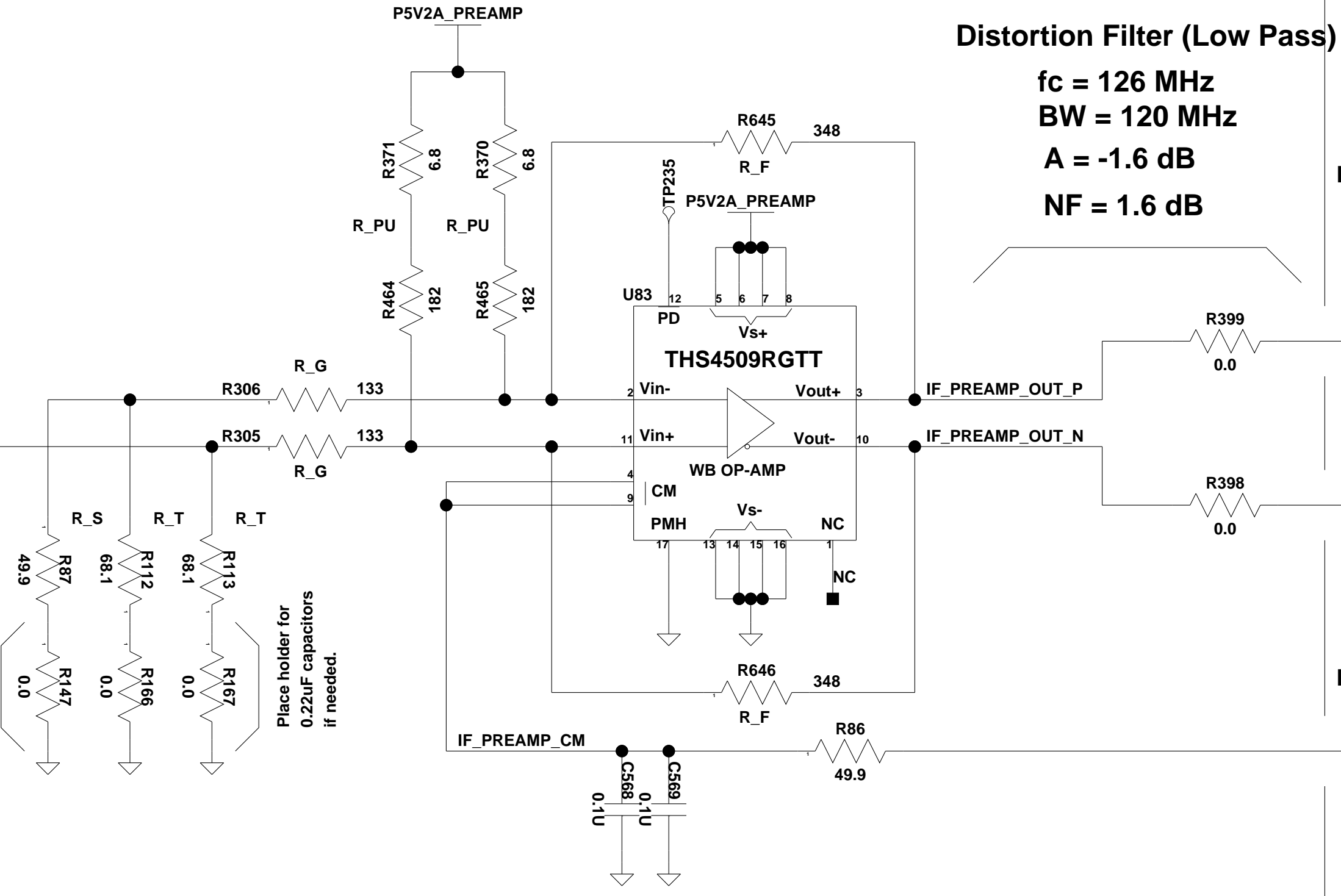
Zi=Zo=50 Ohms
A = -1 dB +/- 0.3 dB
NF = 1 dB +/- 0.3 dB



Place NL right on the transmission line.

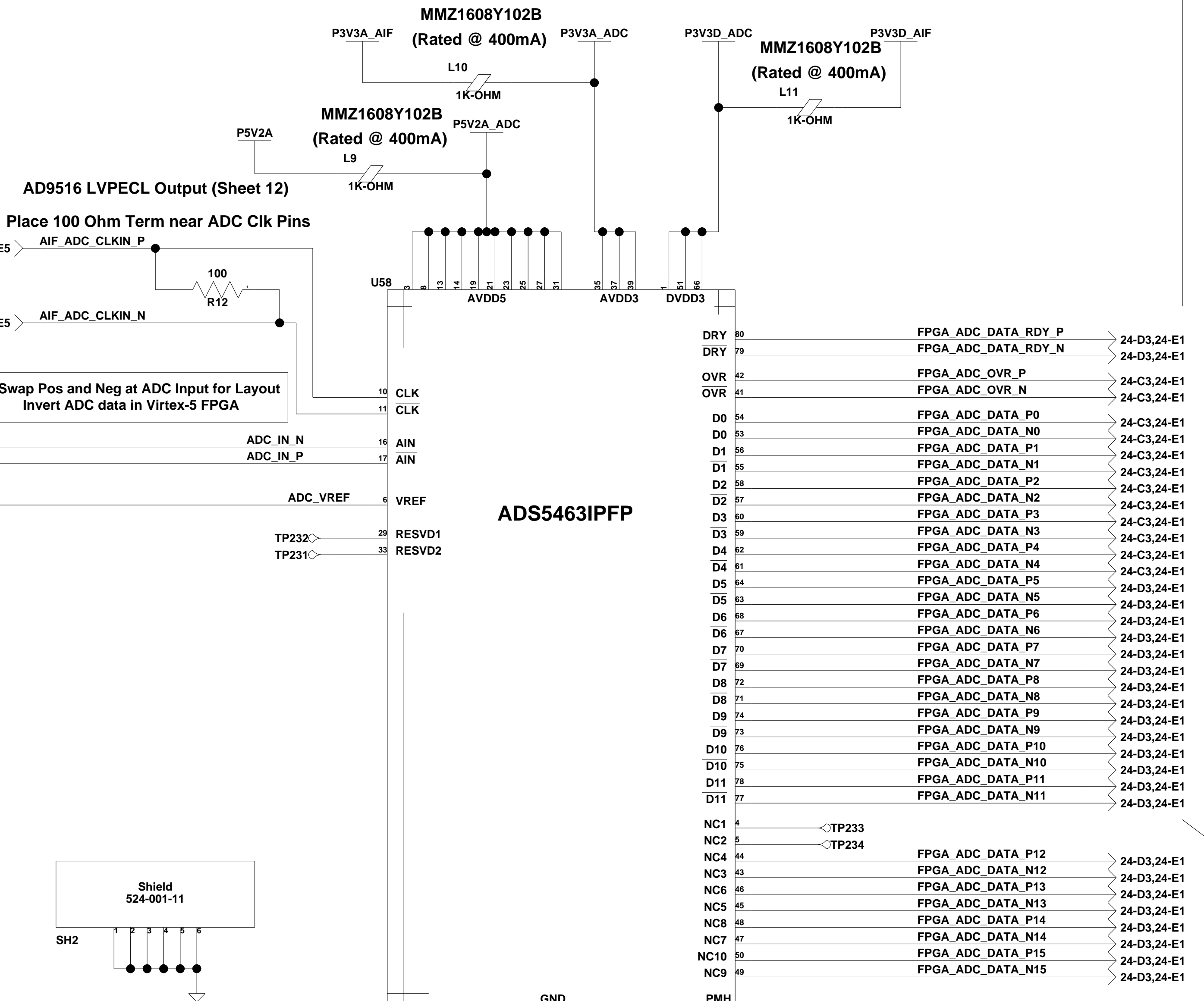
F Pre-Amplifier (+8 dBm)

+5V Analog: I = 50mA Max
IIP3 = 38 dBm
NF = 17.1 dB
A = +8 dB



Distortion Filter (Low Pass)
fc = 126 MHz
BW = 120 MHz
A = -1.6 dB
NF = 1.6 dB

G High-Speed ADC (12-bit, 500MS/s)



AD9516 LVPECL Output (Sheet 12)

Place 100 Ohm Term near ADC Clk Pins

Swap Pos and Neg at ADC Input for Layout
Invert ADC data in Virtex-5 FPGA

Shield 524-001-11

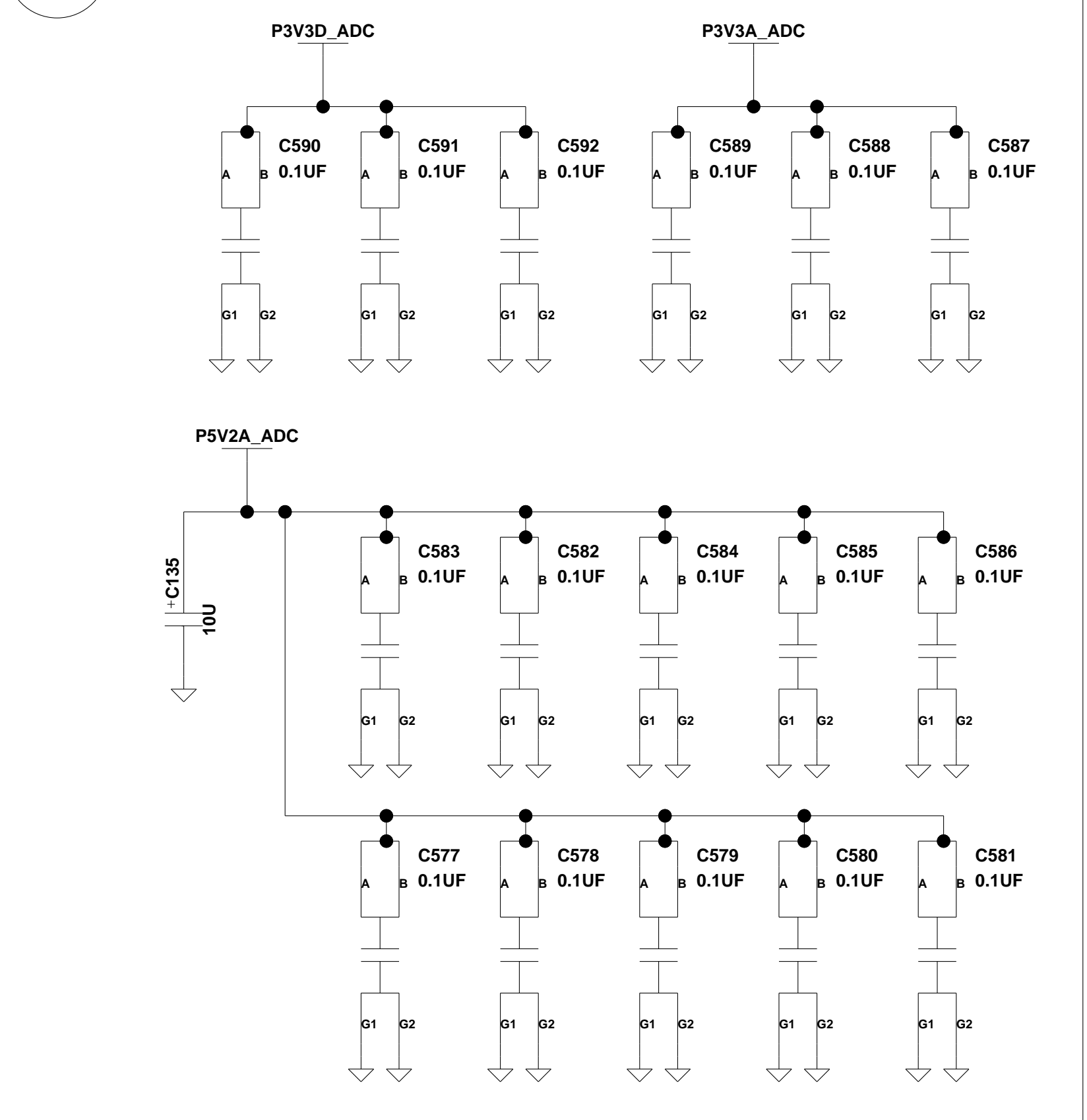
+5V Analog: I = 330mA Max
+3.3V Analog: I = 138mA Max
+3.3V Digital: I = 88mA Max

IIP3 = 44.8 dBm
NF = 18.9898 dB
A = +13.9 dB
Pin = +3.9 dBm
FS = 2Vpp

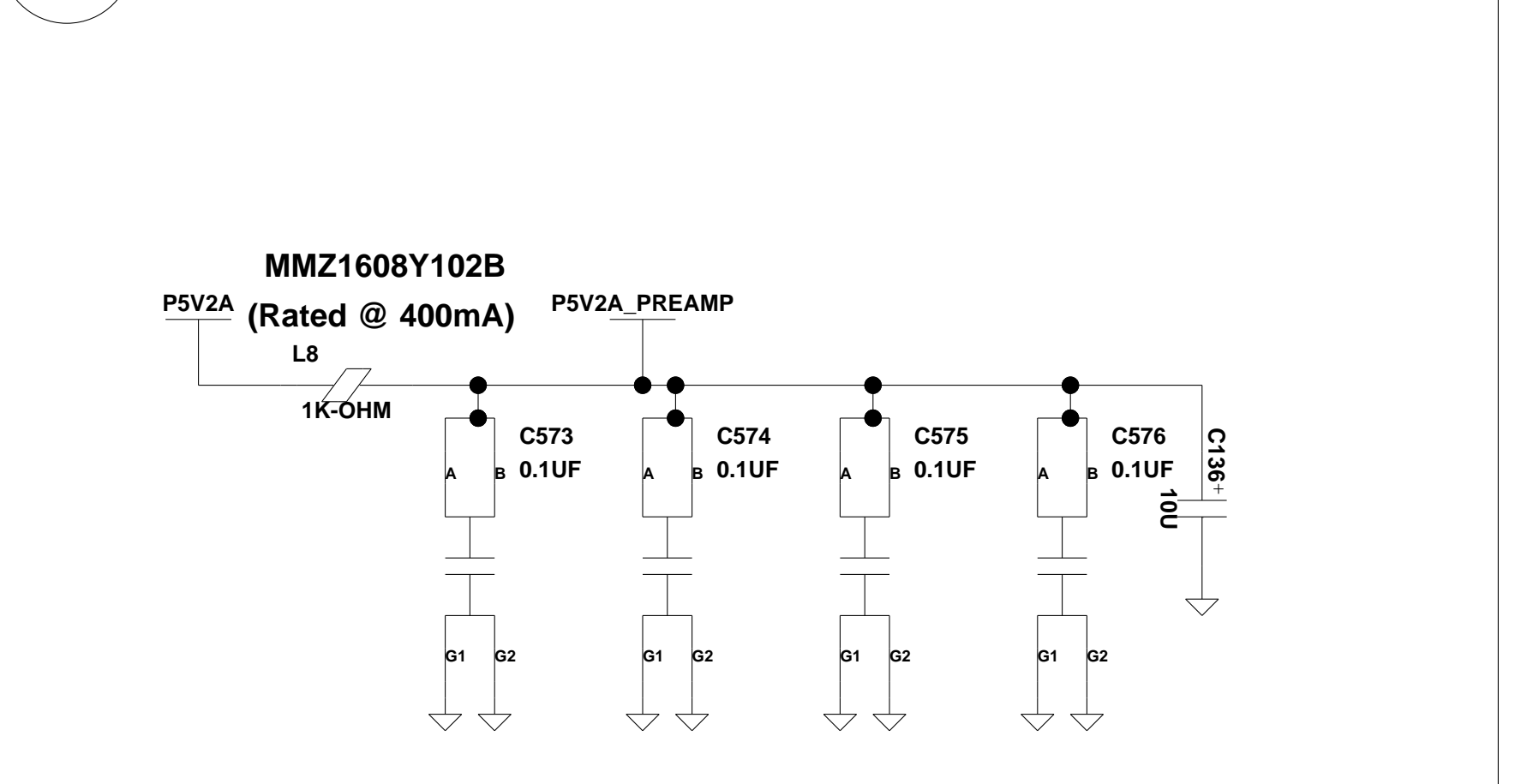
ADC PC Layout Notes:

- Place a 6-by-6 array of thermal vias in the thermal pad area. These holes should be 13 mils in diameter. The small size prevents wicking of the solder through the holes.
- It is recommended to place a small number of 25-mil-diameter holes under the package, but outside the thermal pad area to provide an additional heat path.
- Connect all holes (both those inside and outside the thermal pad area) to an internal copper plane (such as a ground plane).
- Do not use the typical web or spoke via-connection pattern when connecting the thermal vias to the ground plane. Flood the via, rather than using a spoke pattern.

H High-Speed ADC Decoupling



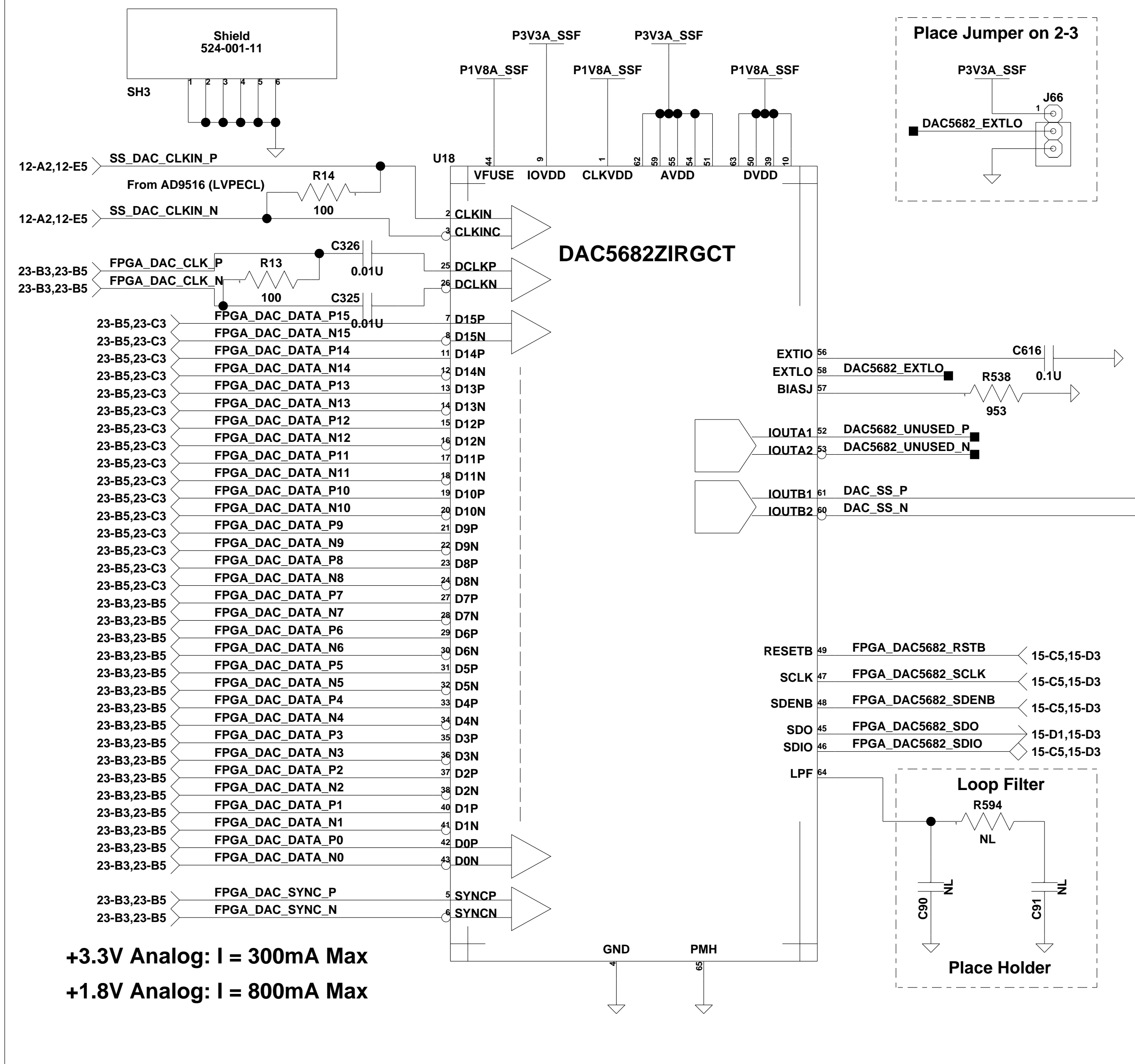
I Pre-Amplifier Decoupling



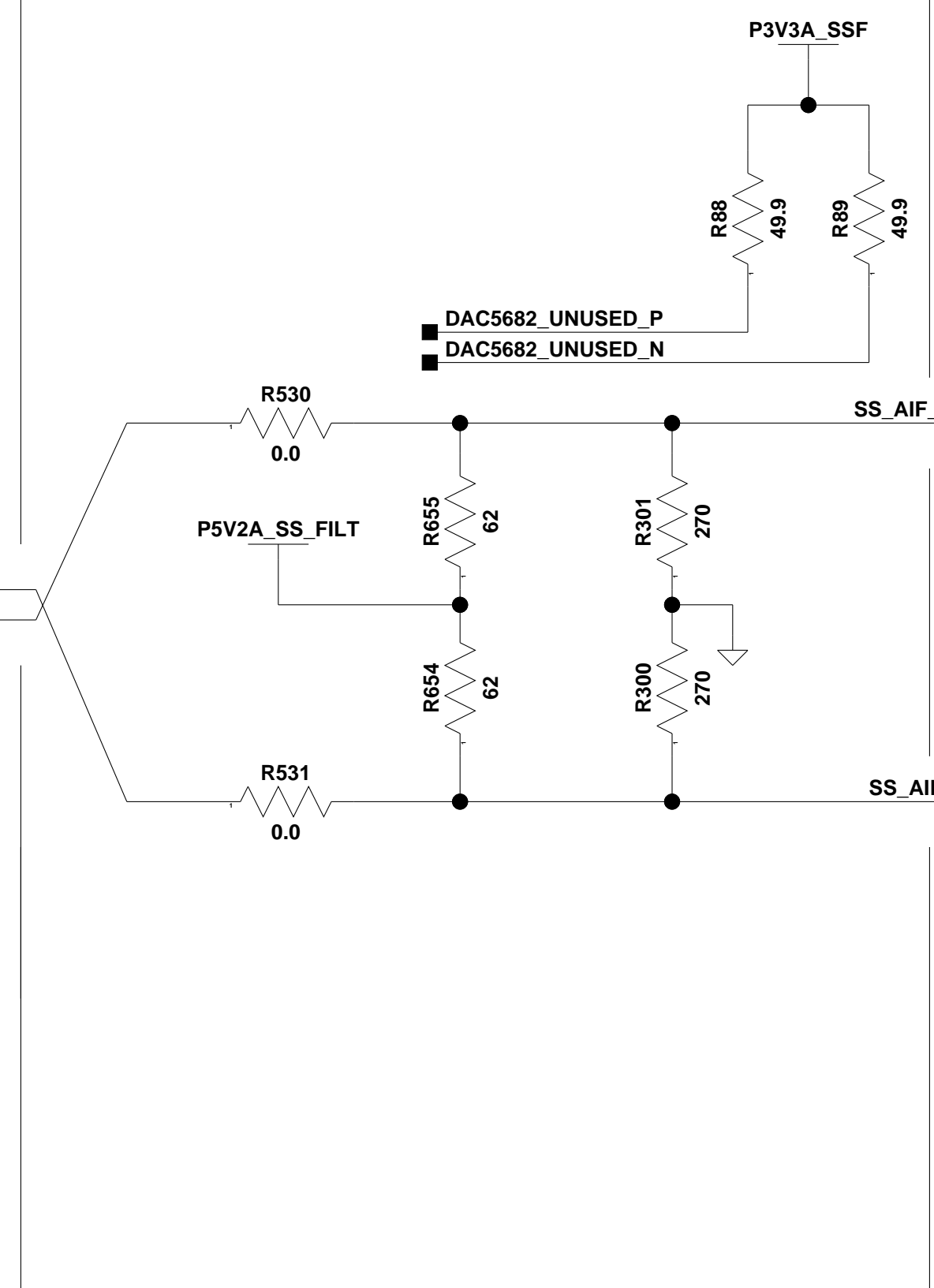
Future Bit Additions

SIGNAL SOURCE

A High-Speed DAC (16-bits, 1GS/s)

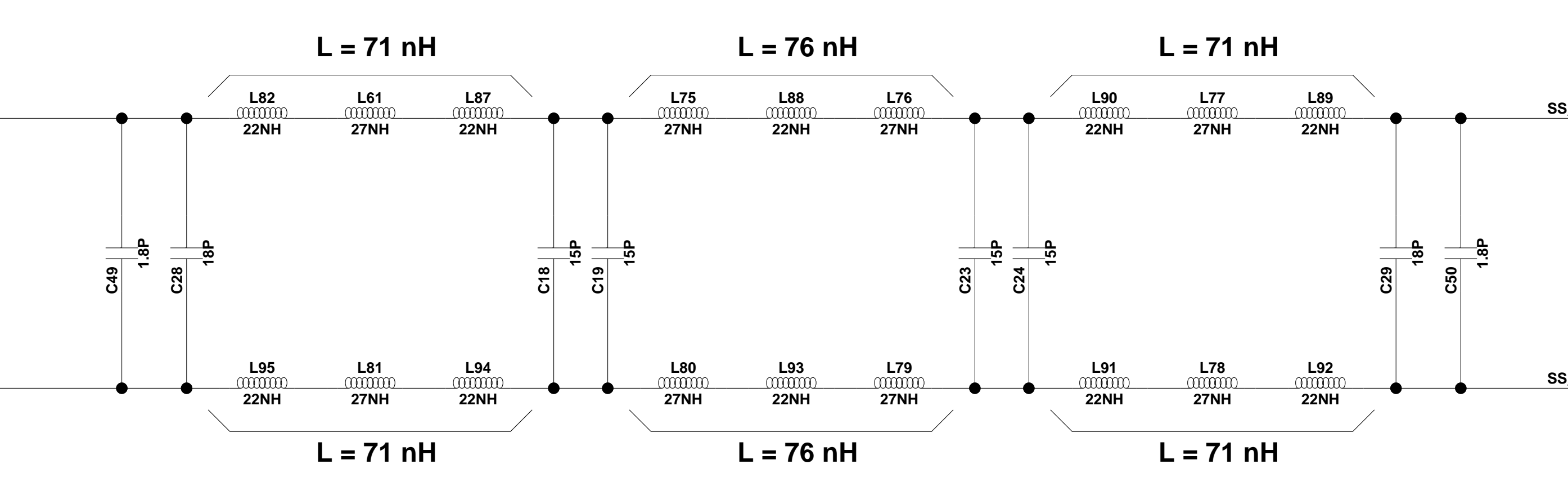


B Output Stage



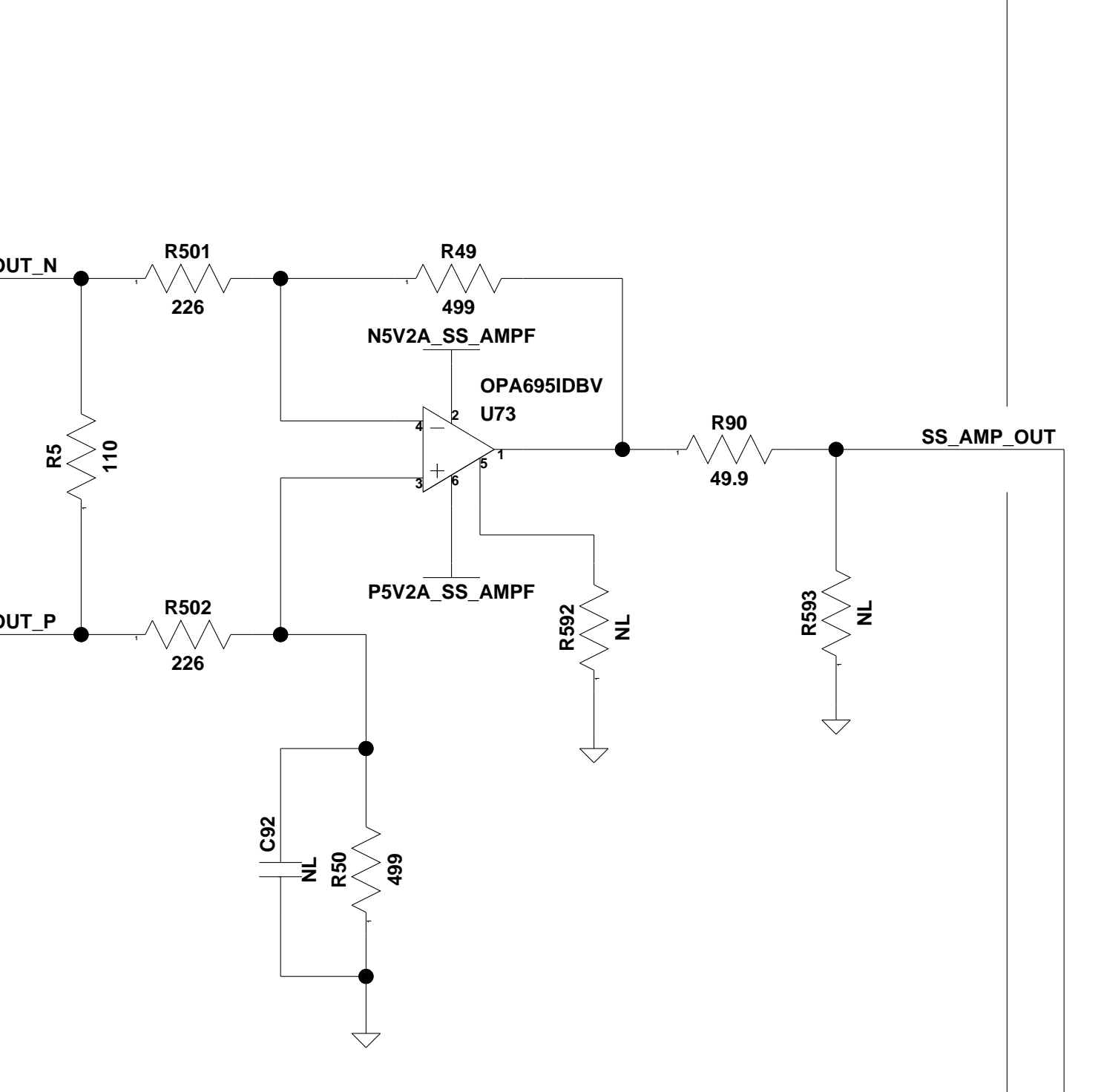
C Anti-Image Filter

7th order Chebyshev Lowpass Filter
 $f_c = 140$ MHz, $BW = 120$ MHz, and $Ripple = 0.5$ dB
 $A = -2.4$ dB
 $NF = 2.4$ dB



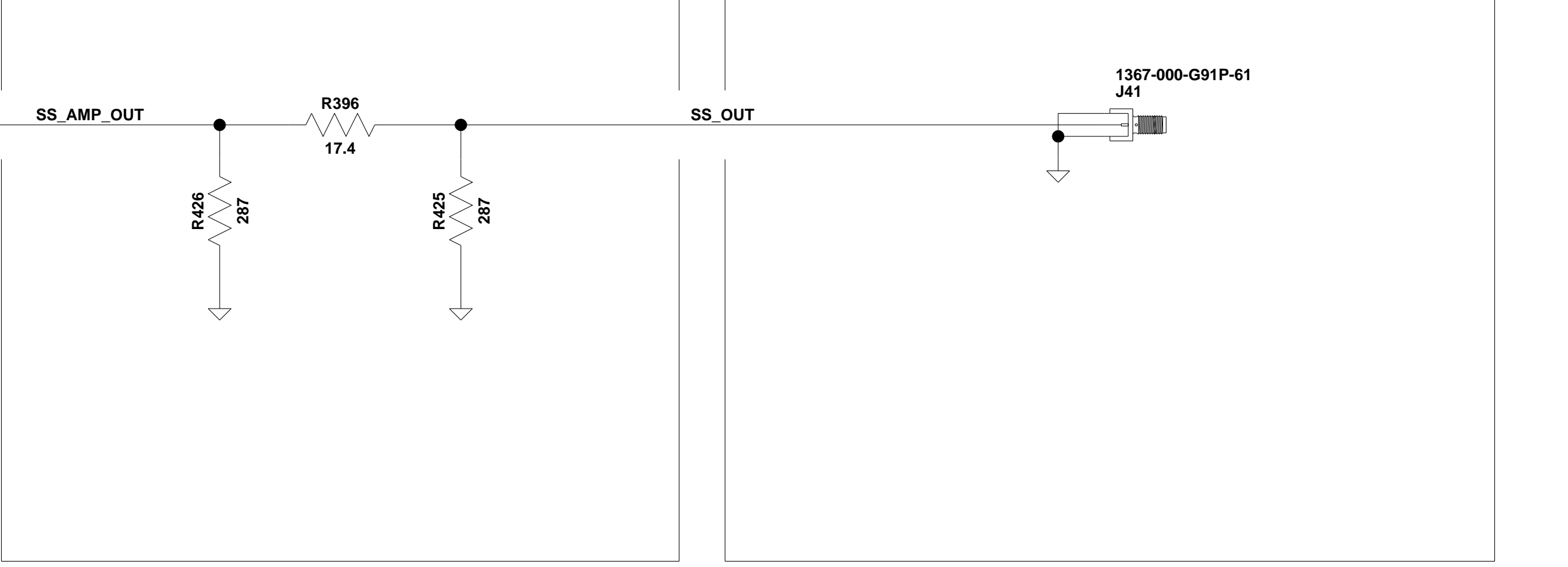
D Amplifier

IIP3 = 20 dBm
 NF = 14 dB
 +5V Analog: I = 100mA Max
 -5V Analog: I = 100mA Max
 A = +14 dB

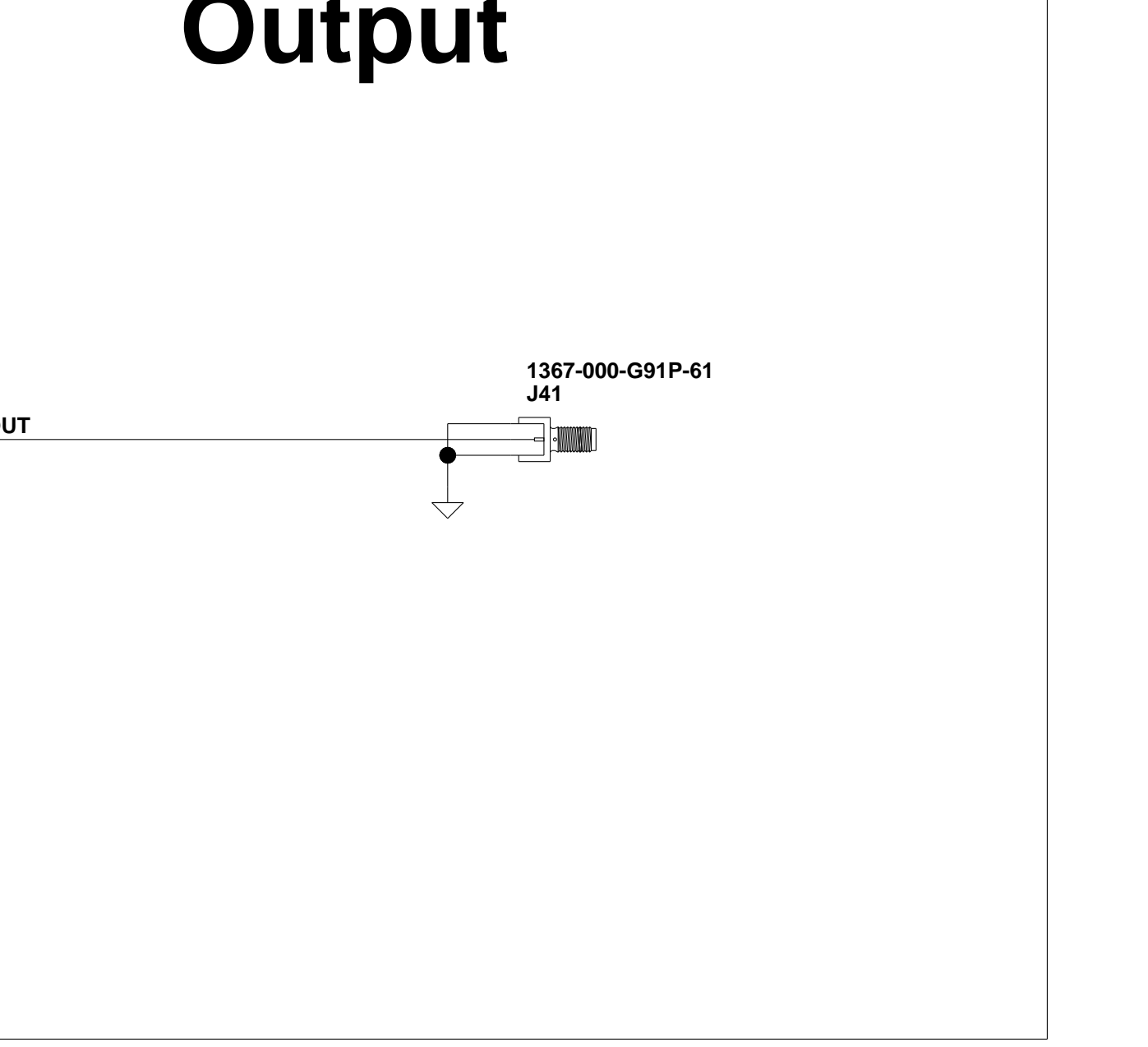


E 3dB PAD

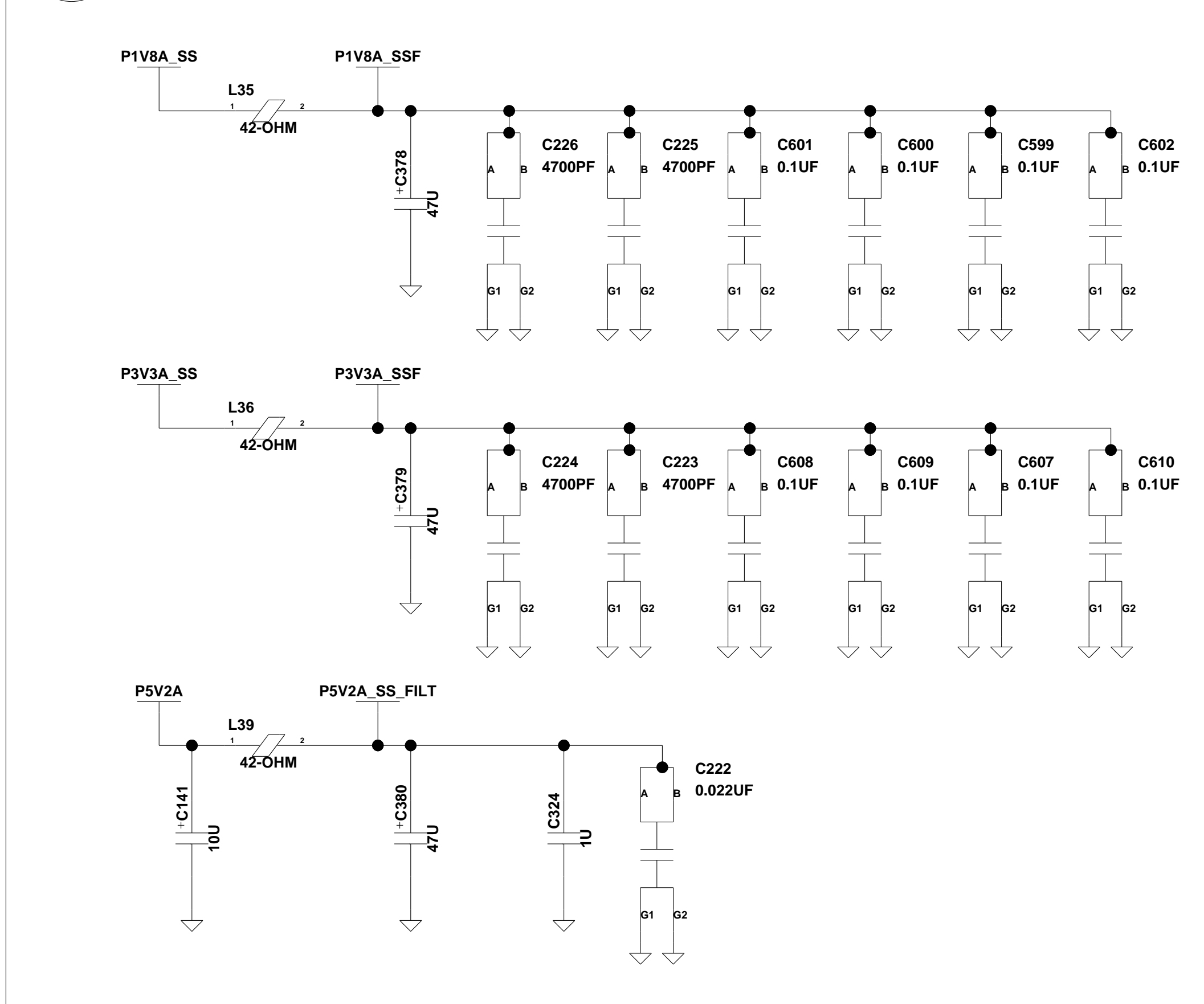
$Z_i = Z_o = 50$ Ohms
 $A = -3$ dB +/- 0.3 dB
 $NF = 3$ dB +/- 0.3 dB



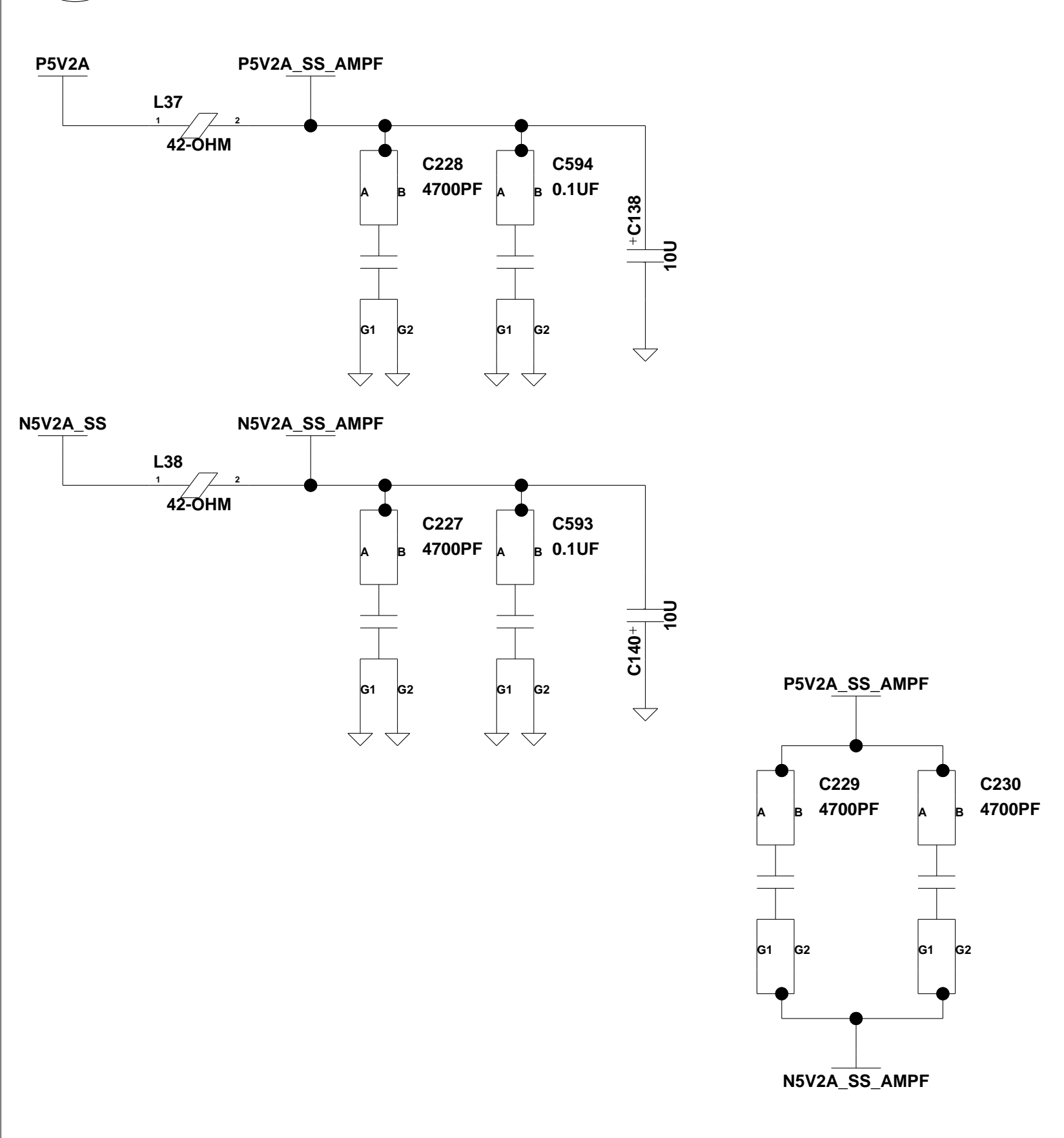
F Signal Source Output



G DAC5682 Decoupling



H OPA695 Decoupling



Trigger Input/Output and Auxiliary Input

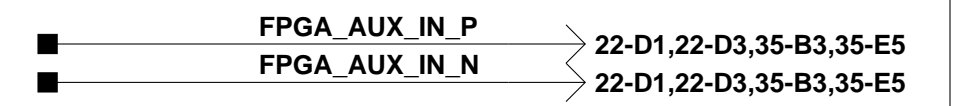
** INPUTS **

Trigger Output

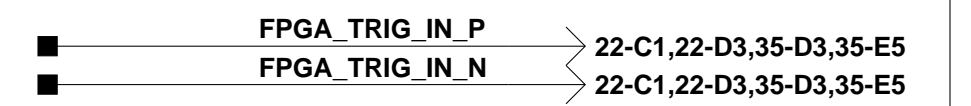


** OUTPUTS **

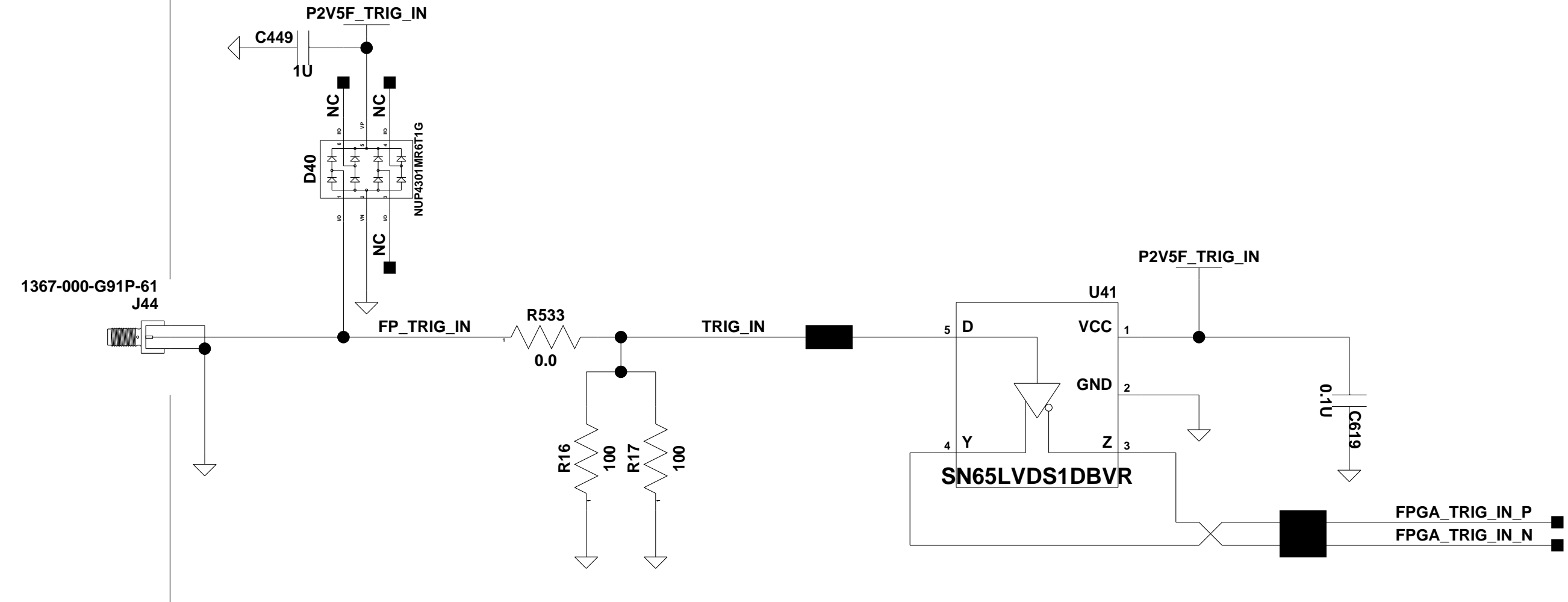
Auxiliary Input



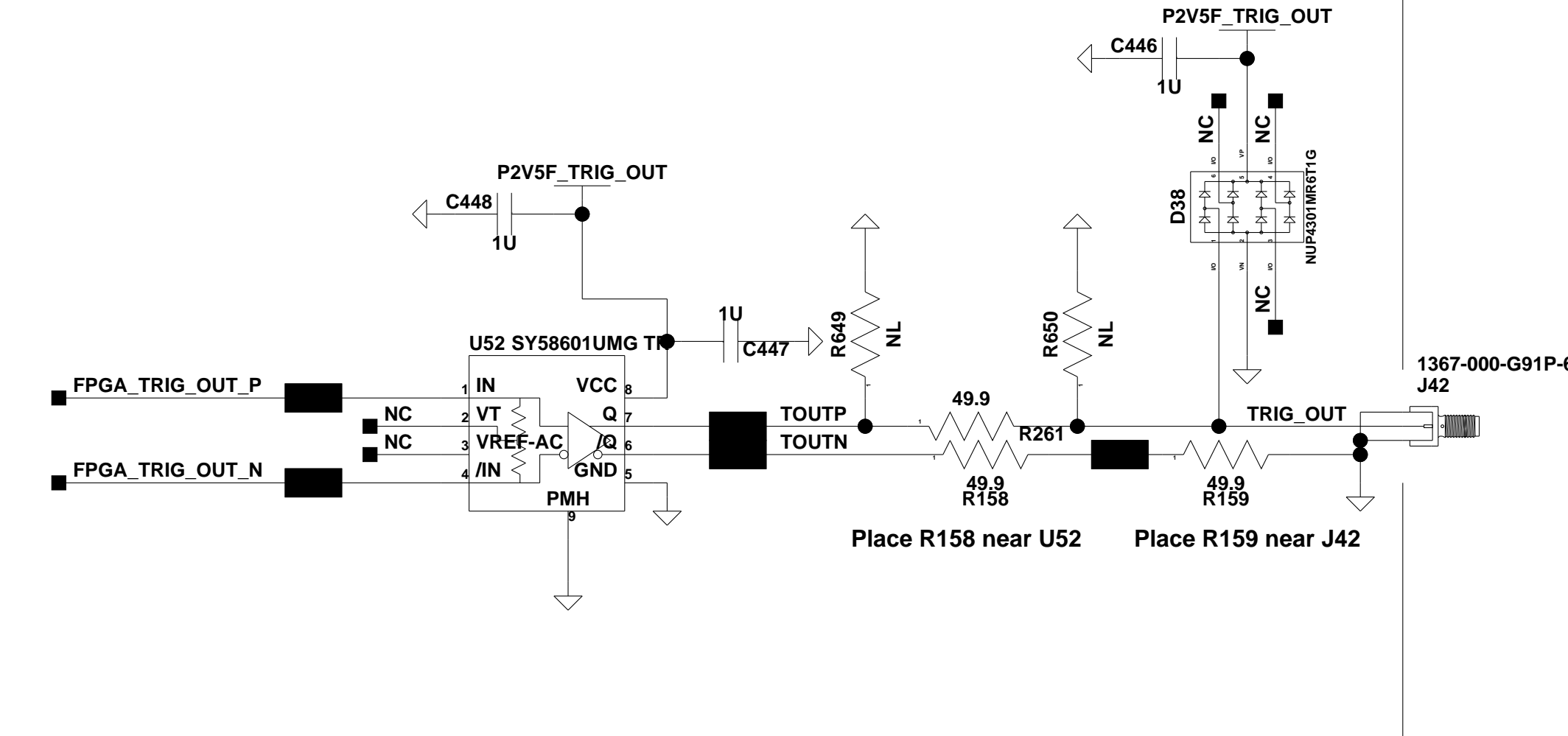
Trigger Input



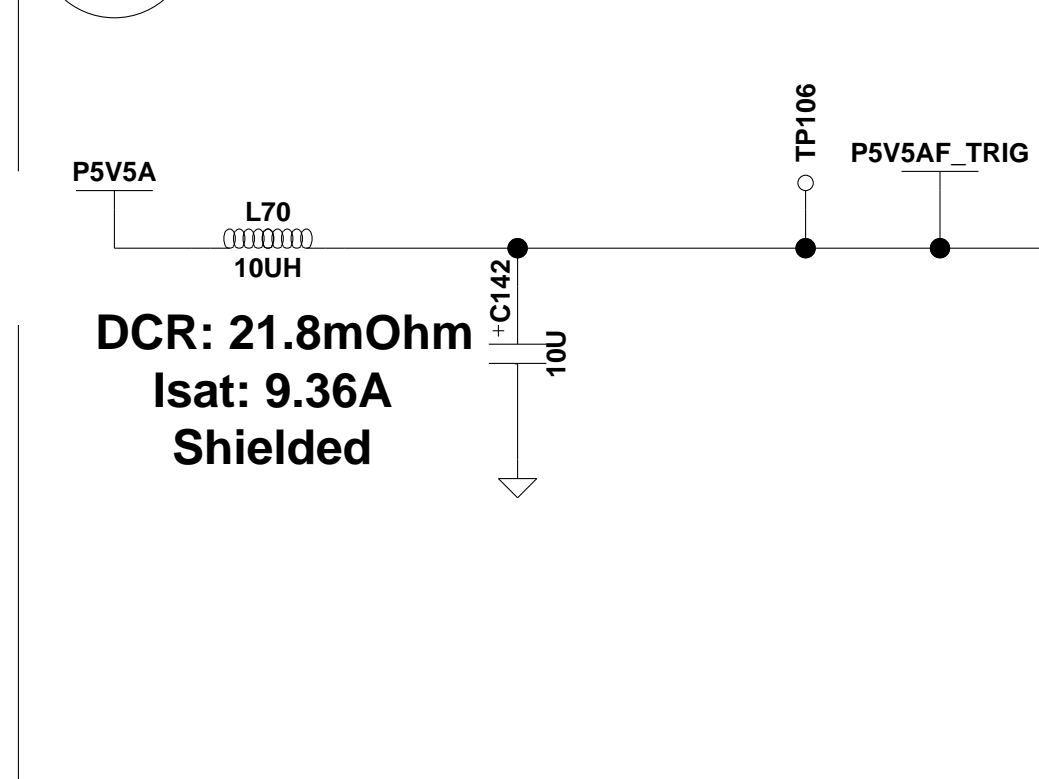
A Trigger Input Buffer



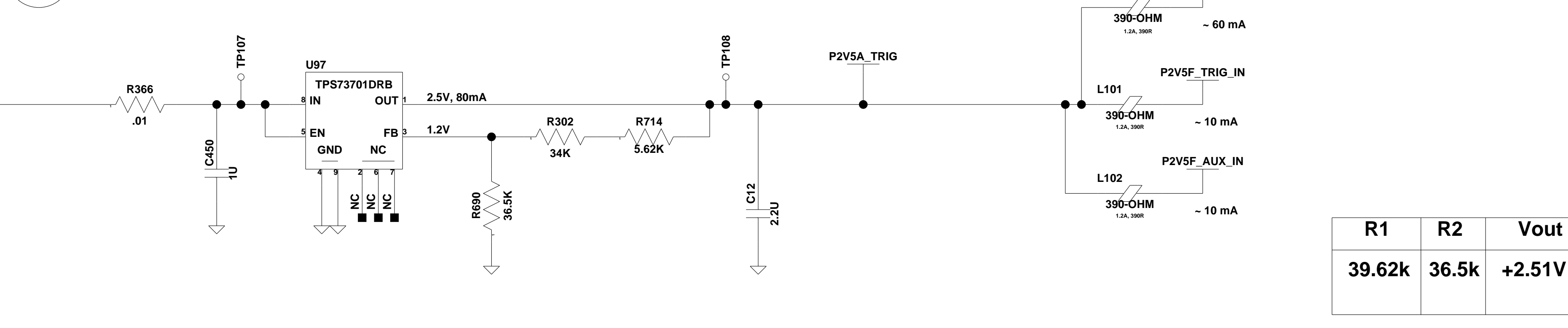
B Trigger Output Buffer



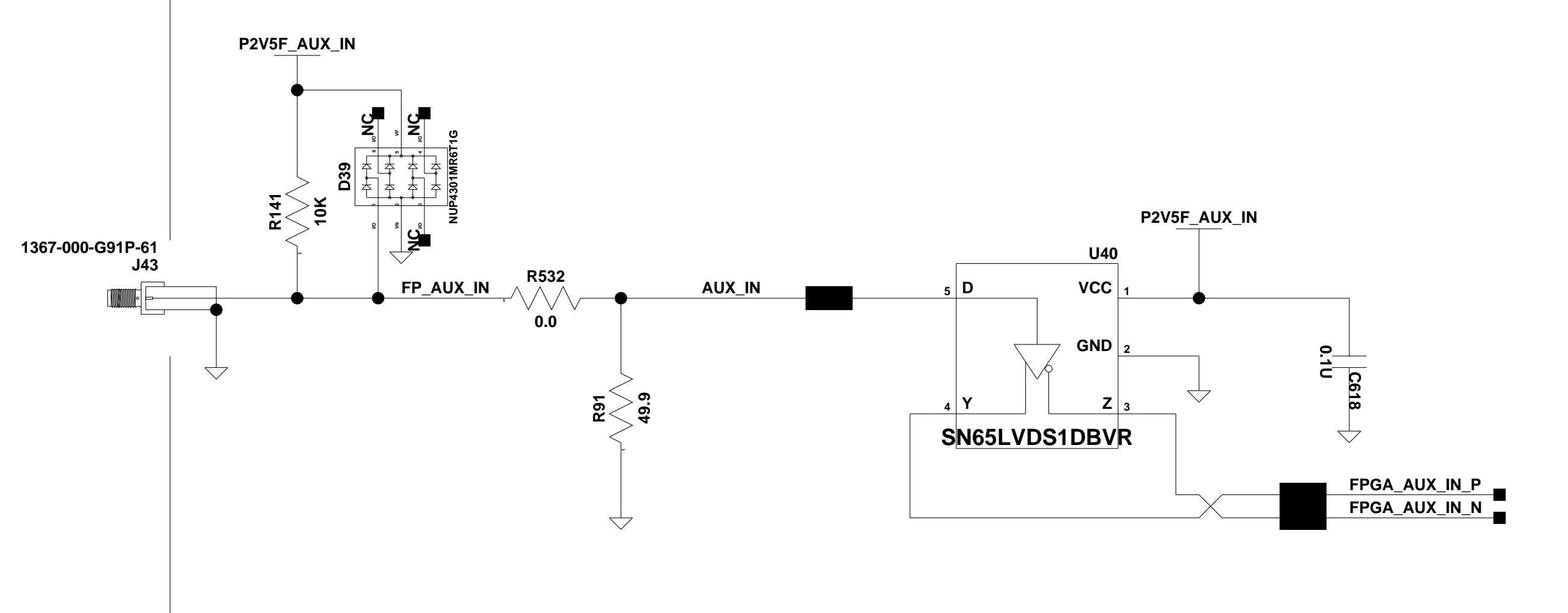
C +5.5V Filter



D +2.5V Trigger Analog Supply Regulation



E Auxillary Input



AsAPv2 #1 Data In/Out, Config, Analog, Test

** INPUTS **

AsAP 1 Data Output

23-C5,23-D3,36-C4,36-E1 → FPGA_ASAP1_REQ_OUT

AsAP 1 Data Input

23-C5,23-D3,23-E3,36-D3,36-E1,37-C2,37-C4,37-D1 → FPGA_ASAP1_DATA_IN[15:0]

23-C5,23-D3,36-C1,36-E1 → FPGA_ASAP1_CLK_IN

23-B5,23-B6,23-E3,36-B1,37-B2,37-D1,37-D2 → FPGA_ASAP1_VLD_IN

AsAP 1 Config Input

15-B5,15-D3,36-D1,36-E1 → FPGA_ASAP1_RESET_COLD

15-B5,15-D3,36-C1,36-E1 → FPGA_ASAP1_CFG_CLK

15-B5,15-D3,36-C1,36-E1 → FPGA_ASAP1_CFG_VALID

15-B5,15-D3,36-C1,36-E1 → FPGA_ASAP1_SPI_CLK

15-B5,15-D3,36-C1,36-E1 → FPGA_ASAP1_SPI_CSN

15-B5,15-D3,36-C2,36-E1 → FPGA_ASAP1_SPI_LOAD

15-B5,15-D3,36-C2,36-E1 → FPGA_ASAP1_MOSI

15-B5,15-D3,36-D1,36-E1 → FPGA_ASAP1_RST_CNTCLK

** OUTPUTS **

AsAP 1 Data Output

FPGA_ASAP1_DATA_OUT[15:0] → 23-D3,23-E1,36-D4,36-E5

FPGA_ASAP1_CLK_OUT → 23-D3,23-E1,36-D4,36-E5

FPGA_ASAP1_VLD_OUT → 23-D3,23-E1,36-C4,36-E5

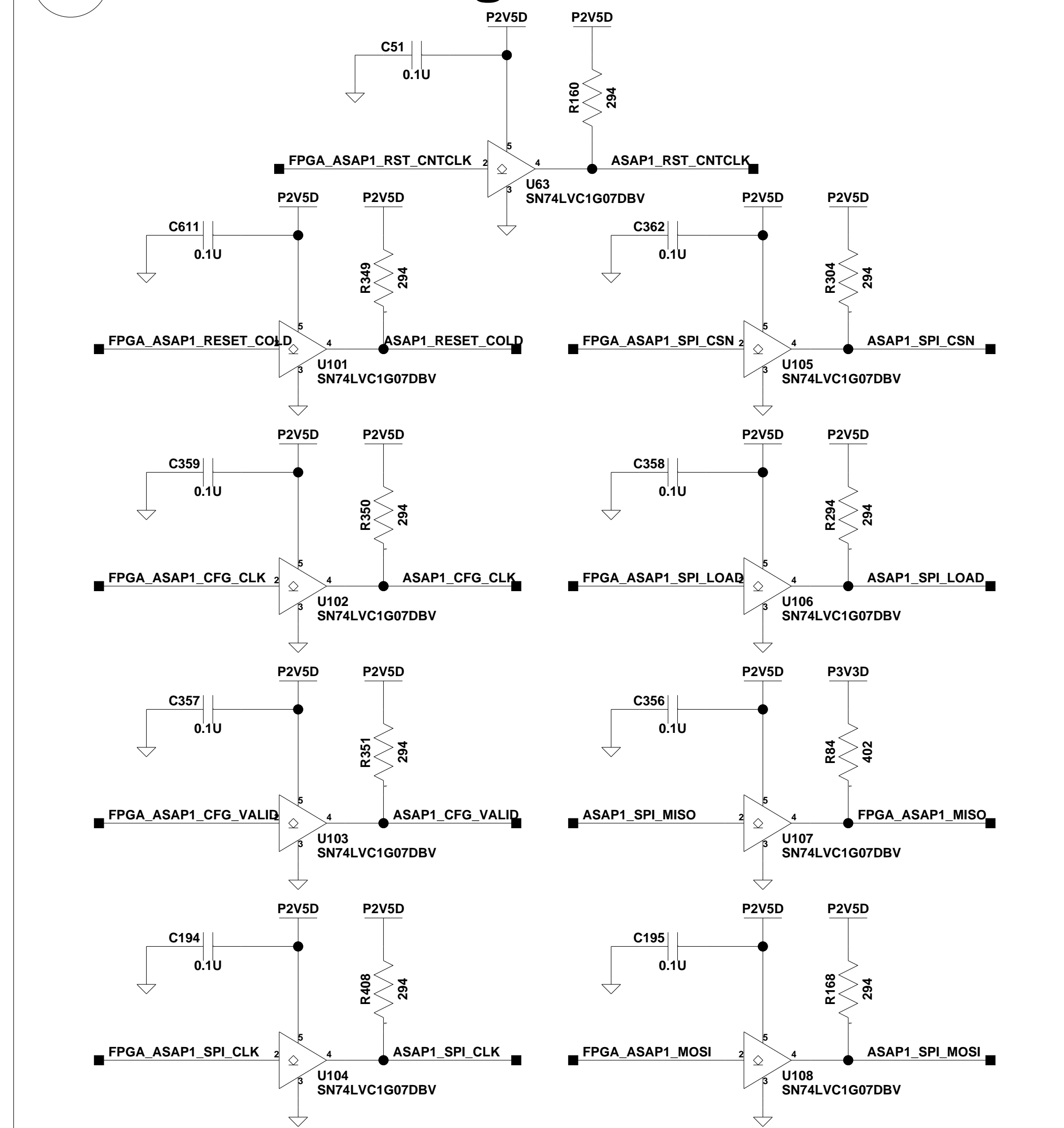
AsAP 1 Data Input

FPGA_ASAP1_REQ_IN → 23-D3,23-E1,36-C3,36-E5

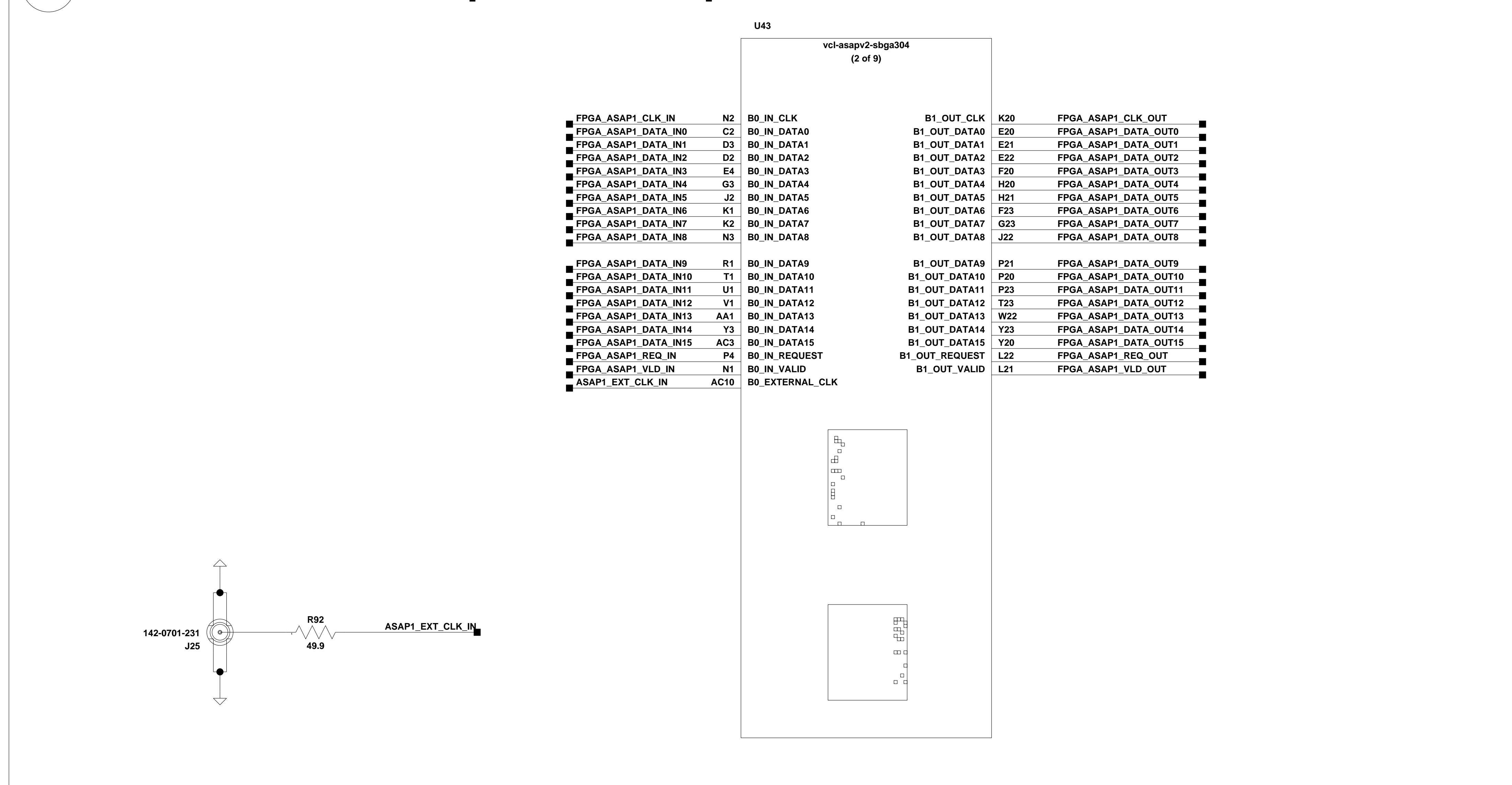
AsAP 1 Config Output

FPGA_ASAP1_MISO → 15-C1,15-D3,36-C2,36-E5

A AsAP Config Level Translate



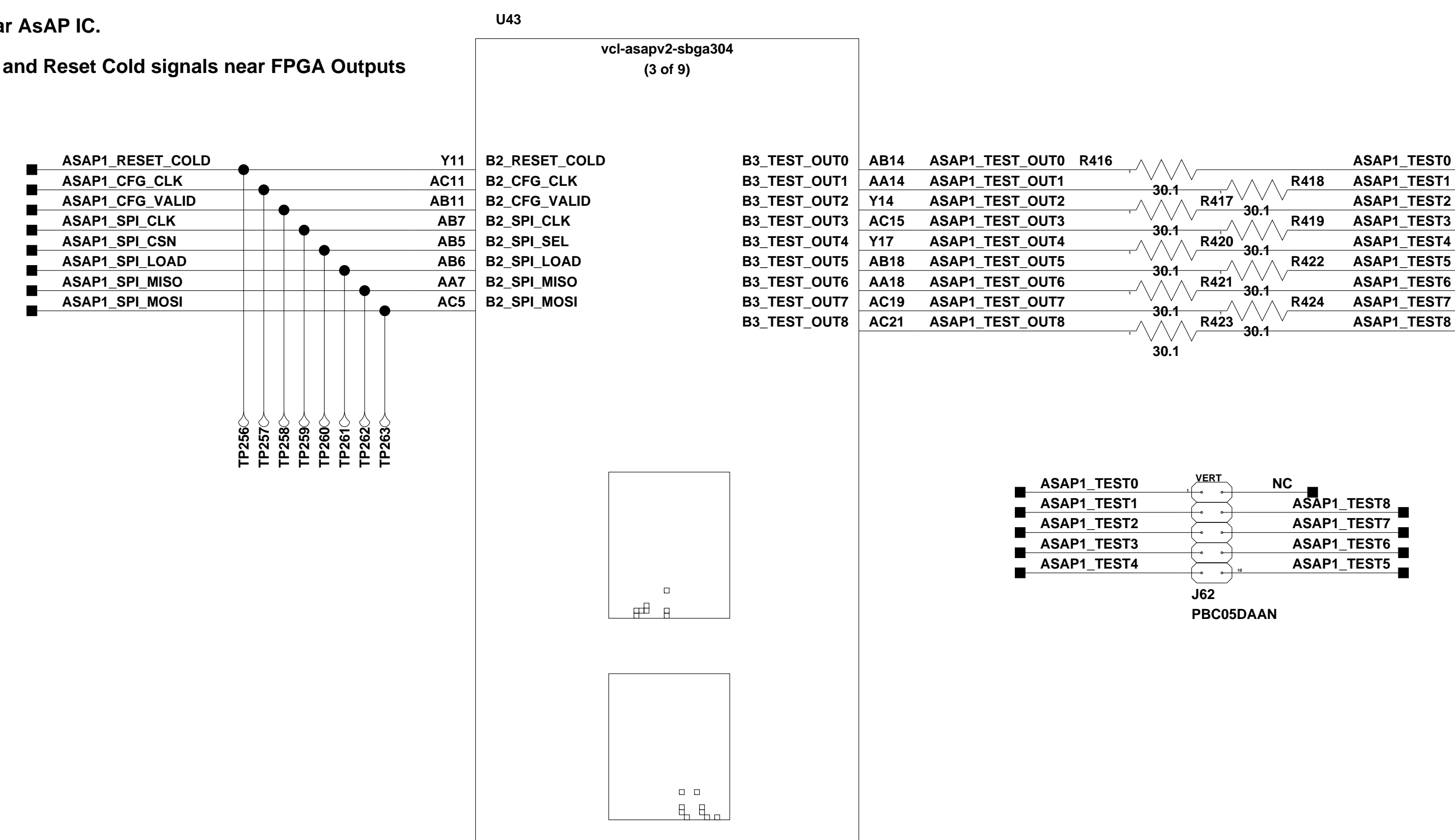
B AsAP Main Data Input and Output



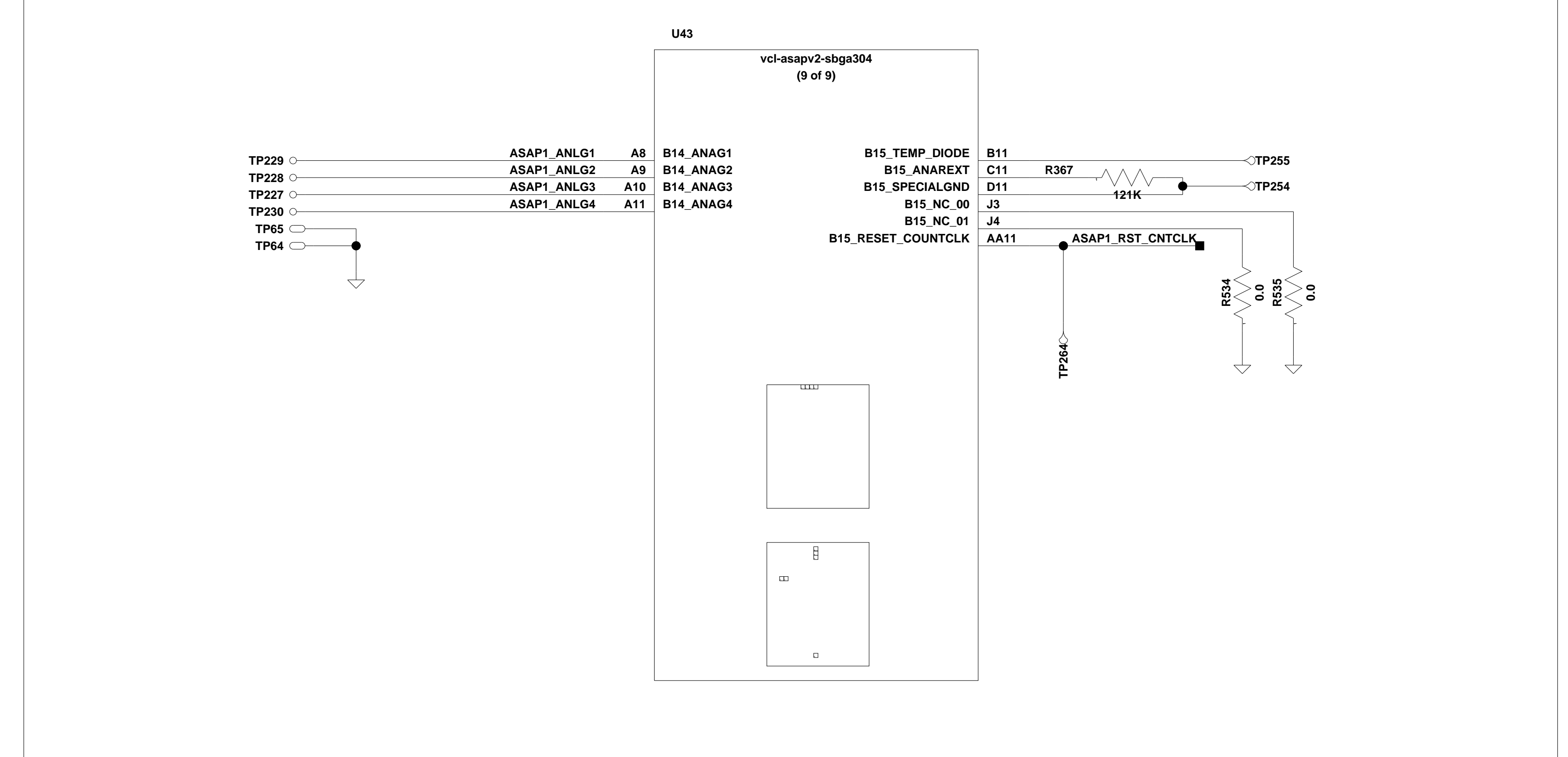
C AsAP Configuration and Test Port

Place 30.1 Ohm Series Resistor on AsAP SPI_MISO near AsAP IC.

Place 30.1 Ohm Series Resistors on all other SPI, CFG, and Reset Cold signals near FPGA Outputs



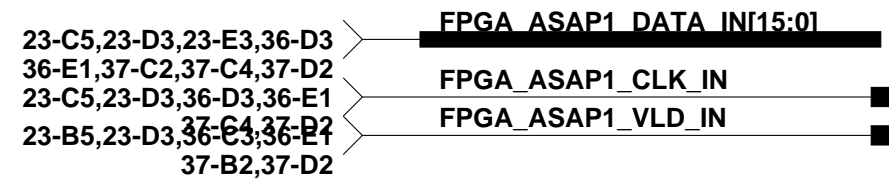
D AsAP Analog and Miscellaneous I/O



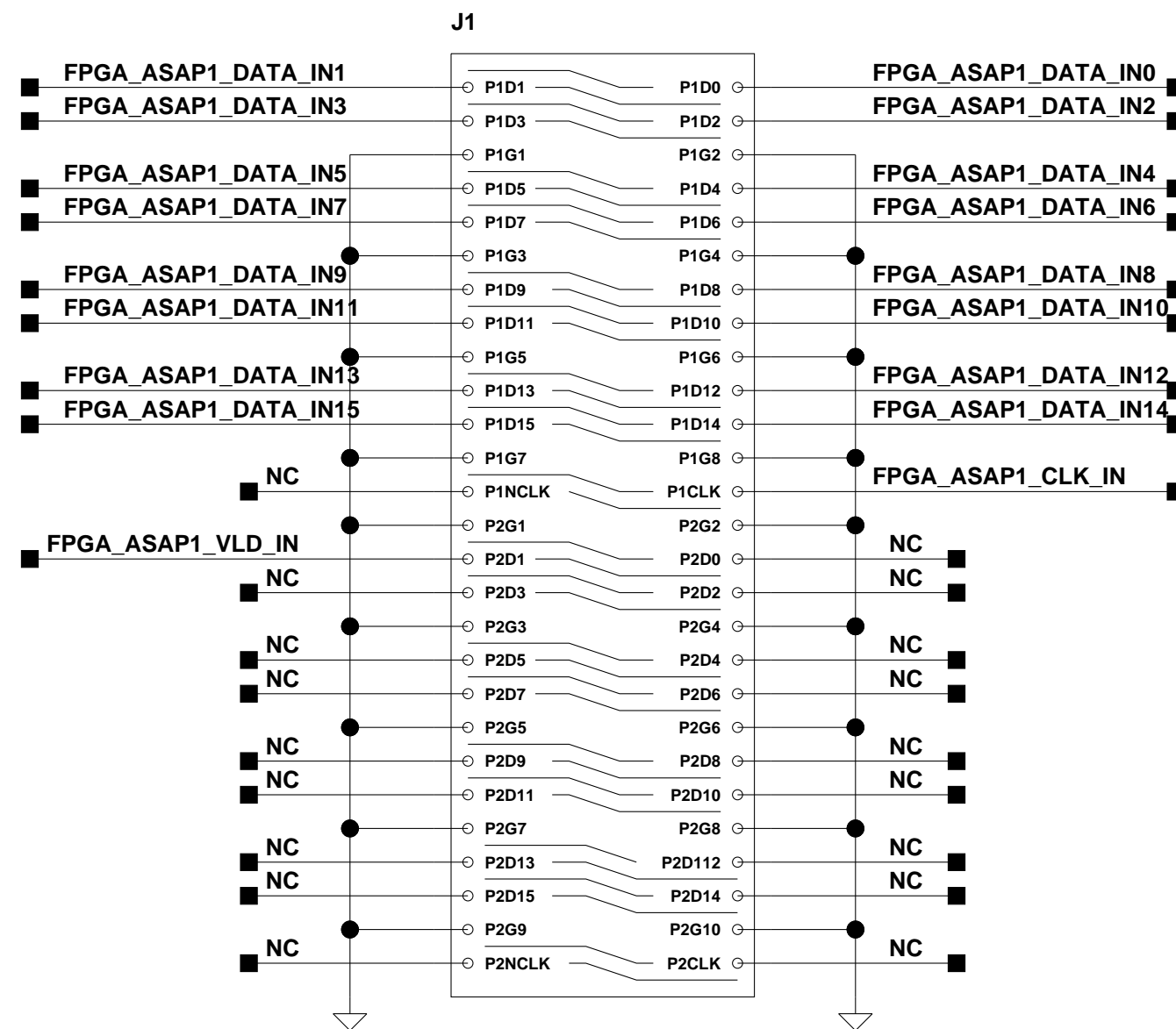
AGILENT 16902A Logic Analyzer E5390A SOFT-TOUCH CONNECTOR

**** INPUTS ****

AsAP 1 Data Input to Logic Analyzer



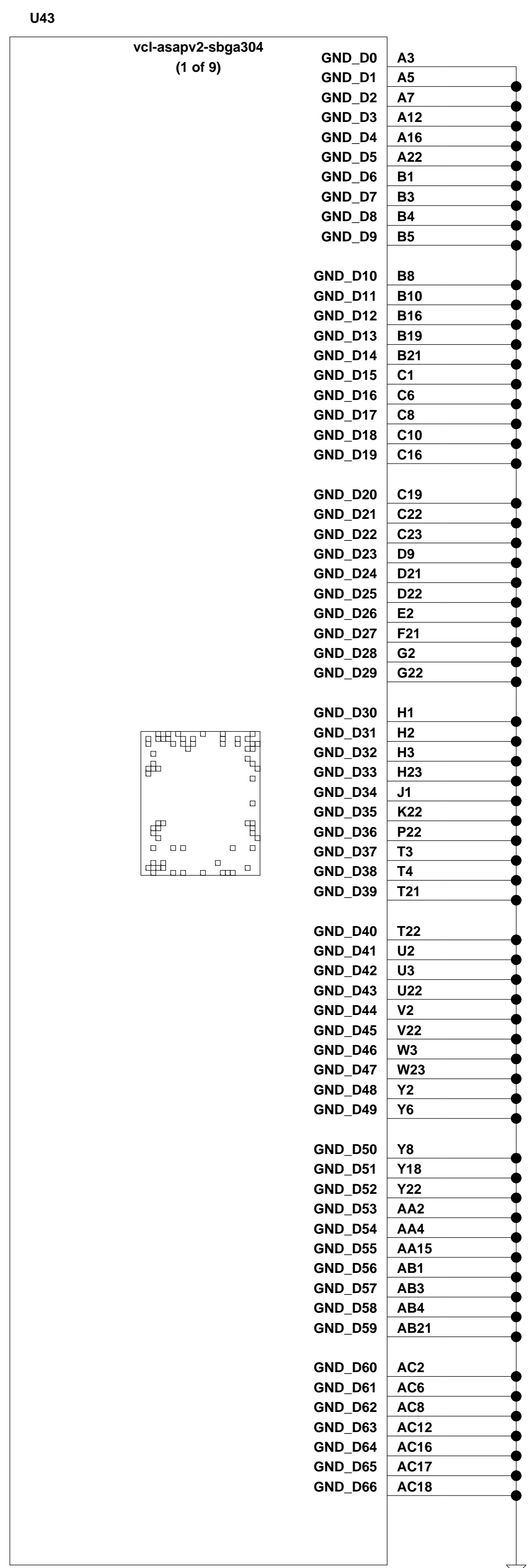
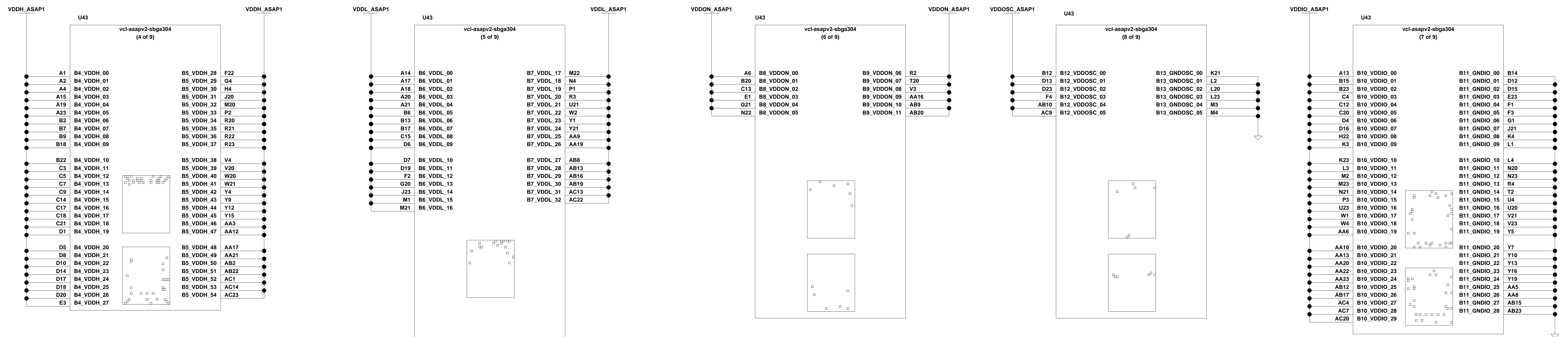
A SOFT-TOUCH SINGLE-ENDED PROBE (E5390A)



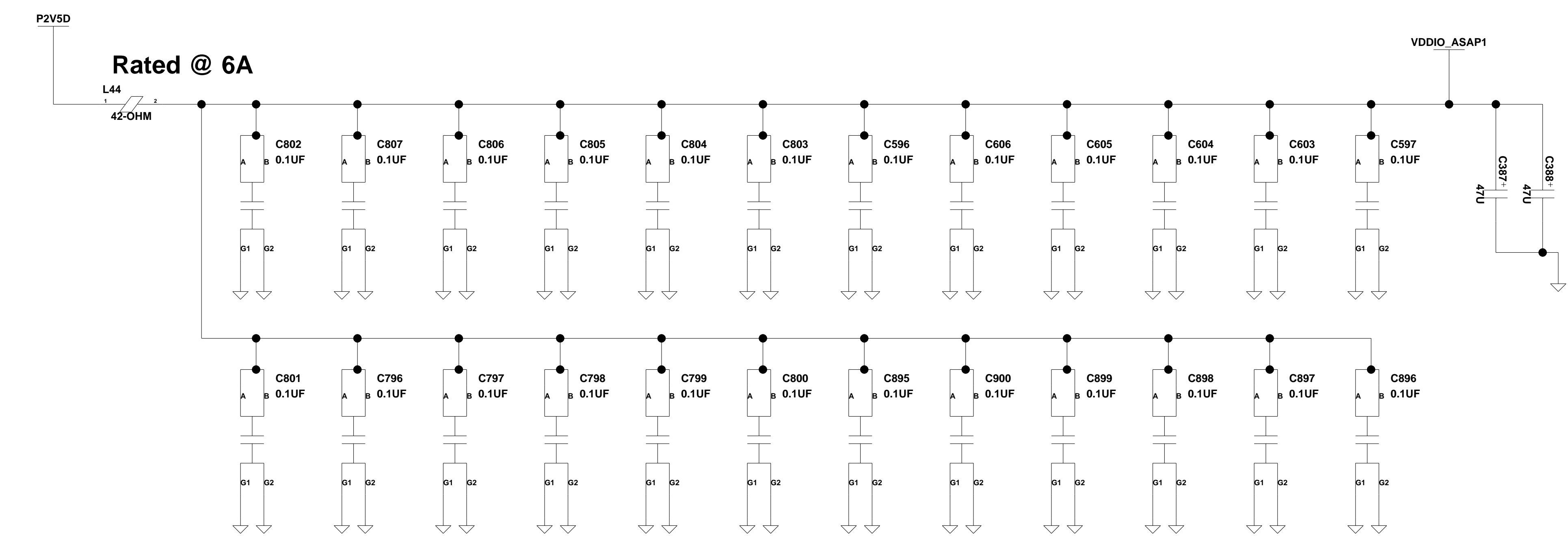
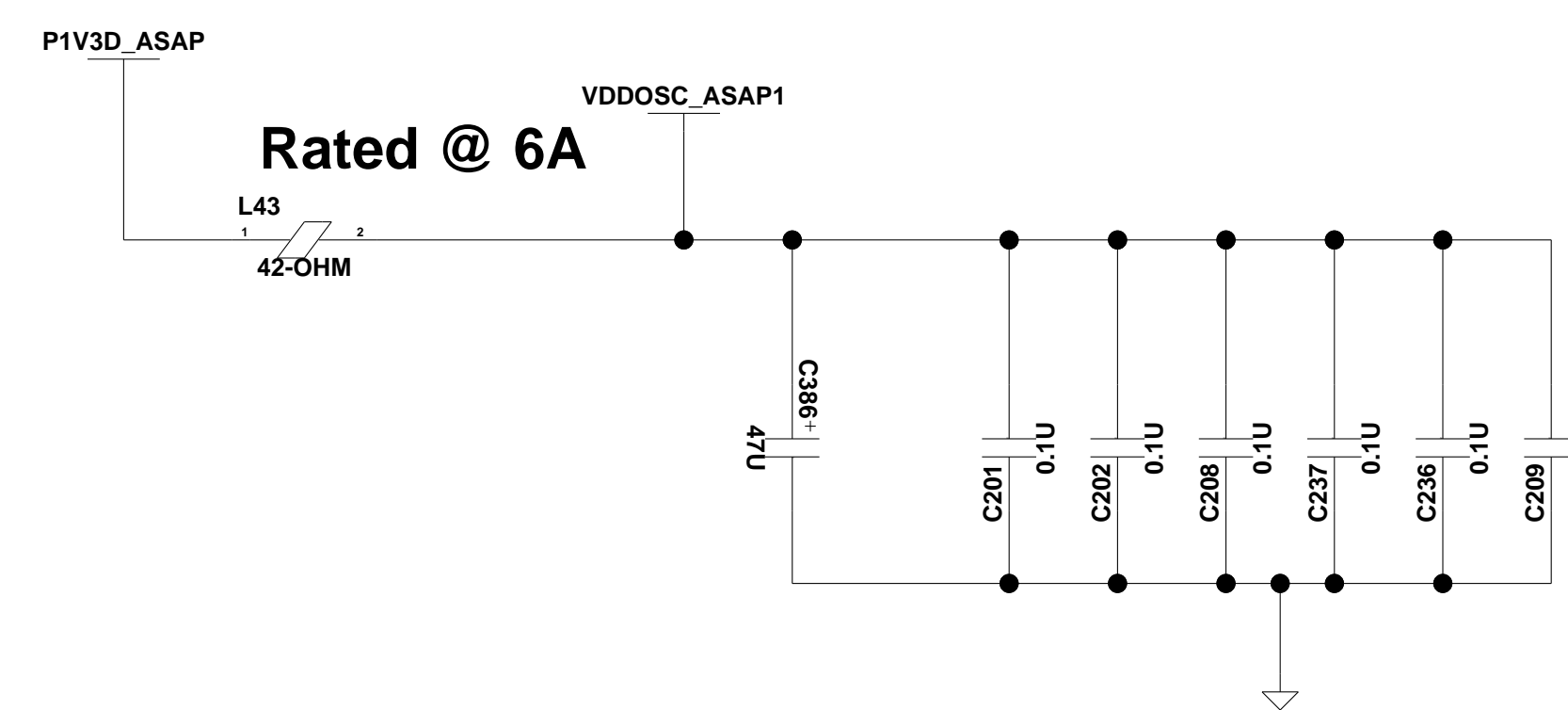
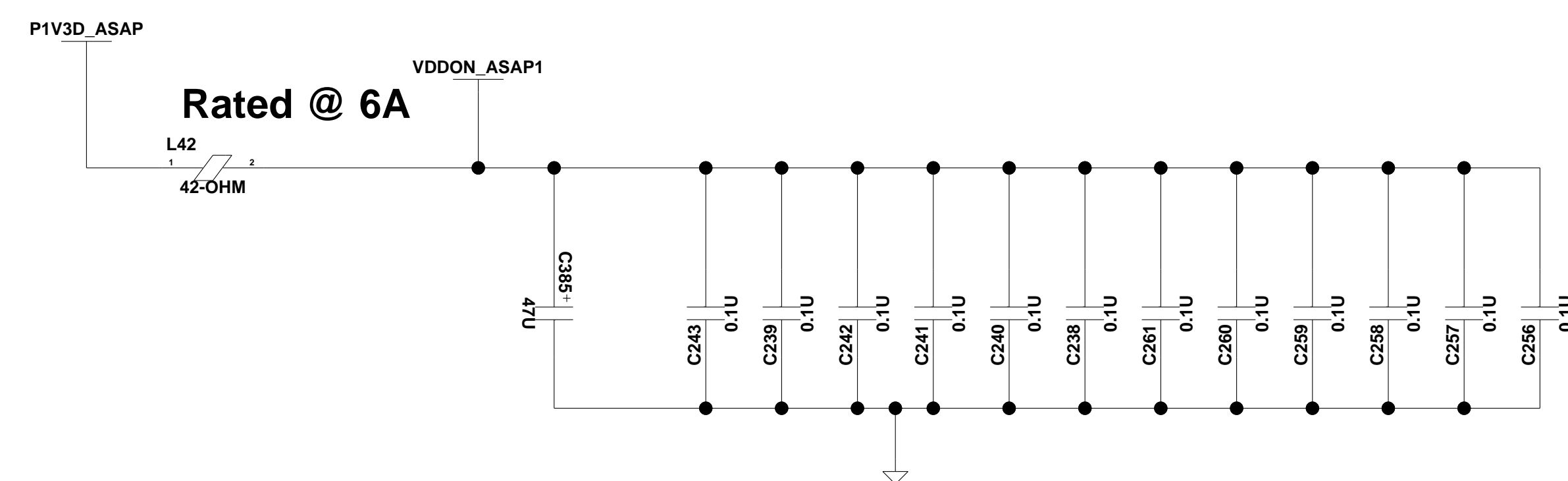
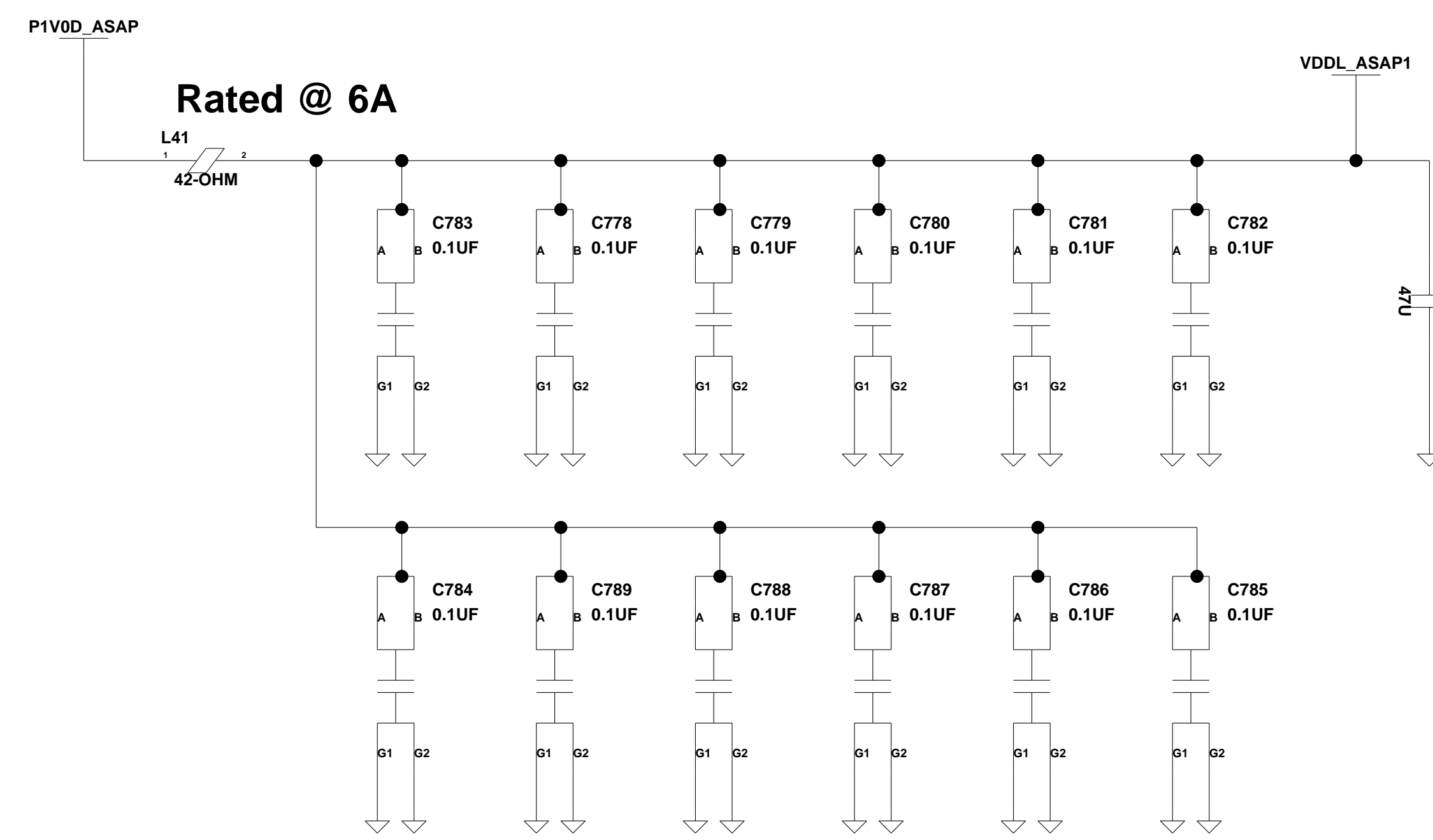
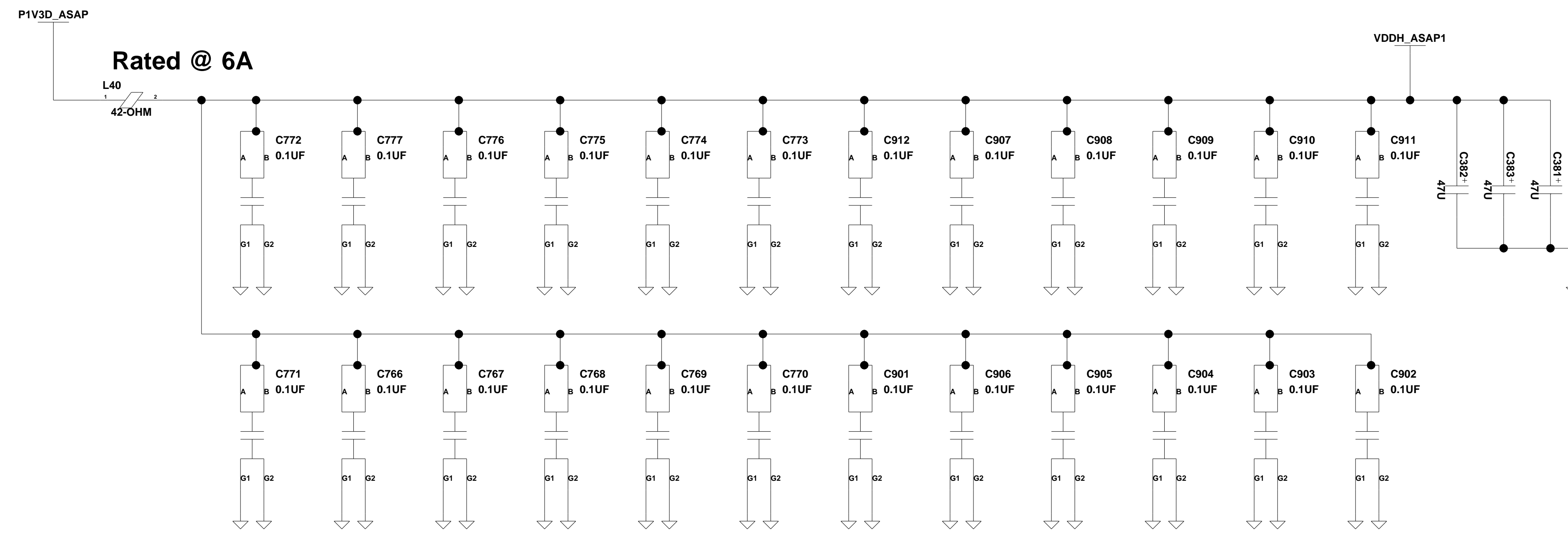
VLSI Computation LAB

Title:	AGILENT 16902A LOGIC ANALYZER E5390A SOFT-TOUCH CONNECTOR		
File:	MEAS_MAIN_BOARD		
Created by:	JEREMY W. WEBB	Date:	4-20-2009_13:35
Modified by:		Date:	
PCB NO:	342	Size:	C
Sheet	37	of	43
REV:	001		

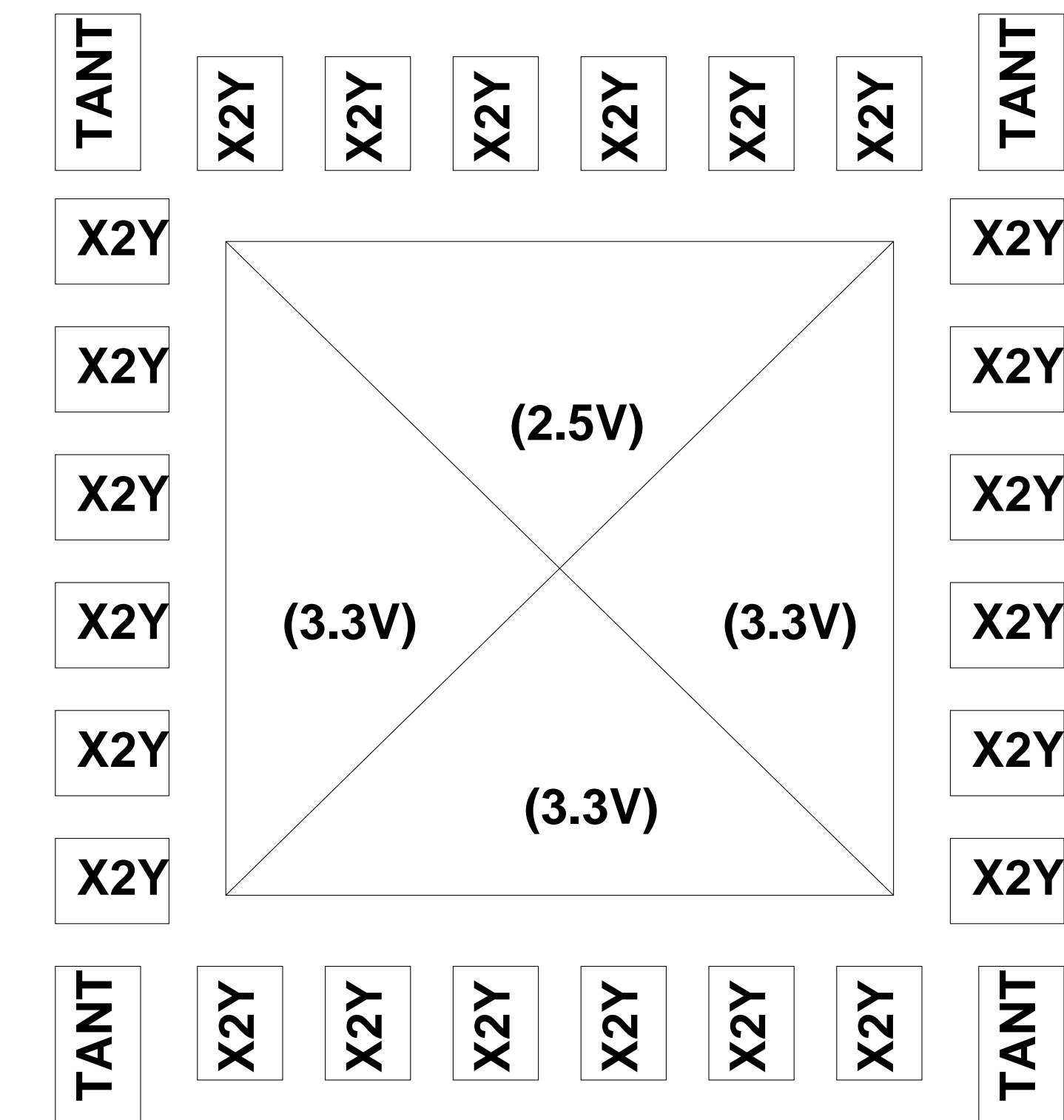
AsAPv2 #1 Power Supply Inputs



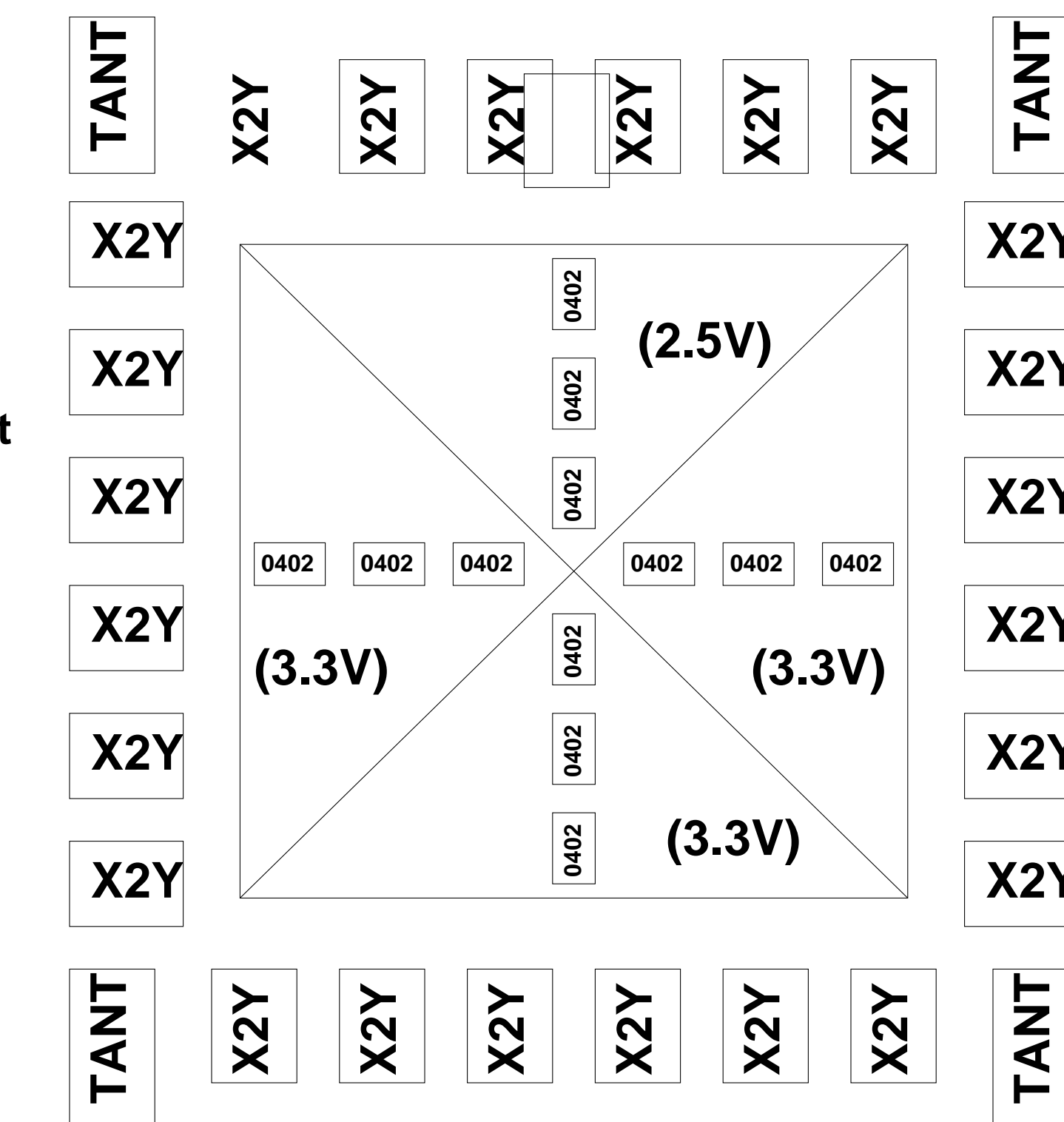
AsAPv2 #1 Power Supply Decoupling



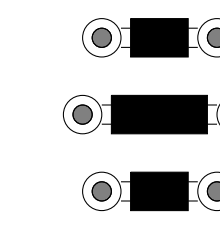
Capacitor Placement
(top side)



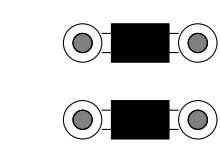
Capacitor Placement
(bottom side)



X2Y Capacitor Via Placement



Tantalum/O402 Via Placement



AsAPv2 #2 Data In/Out, Config, Analog, Test

** INPUTS **

AsAP 2 Data Output

24-D1,24-E5,40-D4,40-E1 FPGA_ASAP2_REQ_OUT

AsAP 2 Data Input

24-D1,24-E5,40-D3,40-E1 FPGA_ASAP2_DATA_IN[15:0]
 41-C2,41-C4,41-E1,41-E2 FPGA_ASAP2_CLK_IN
 24-D1,24-E5,40-D3,40-E1 FPGA_ASAP2_VLD_IN
 24-D1,24-E5,40-D3,40-E1 FPGA_ASAP2_RST_CNTCLK

AsAP 2 Config Input

15-B5,15-C3,40-D1,40-E1 FPGA_ASAP2_RESET_COLD
 15-B3,15-B5,40-C1,40-E1 FPGA_ASAP2_CFG_CLK
 15-A5,15-B3,40-C1,40-E1 FPGA_ASAP2_CFG_VALID
 15-A5,15-C3,40-C1,40-E1 FPGA_ASAP2_SPI_CLK
 15-A5,15-C3,40-D2,40-E1 FPGA_ASAP2_SPI_CSN
 15-A5,15-C3,40-C2,40-E1 FPGA_ASAP2_SPI_LOAD
 15-A5,15-B3,40-C2,40-E1 FPGA_ASAP2_MISO
 14-D4,14-E5,40-D1,40-E1 FPGA_ASAP2_RST_CNTCLK

** OUTPUTS **

AsAP 2 Data Output

FPGA_ASAP2_DATA_OUT[15:0] 24-C1,24-D1,24-E1,40-D4,40-E5
 FPGA_ASAP2_CLK_OUT 24-D1,24-E1,40-D4,40-E5
 FPGA_ASAP2_VLD_OUT 24-D1,24-E1,40-C4,40-E5

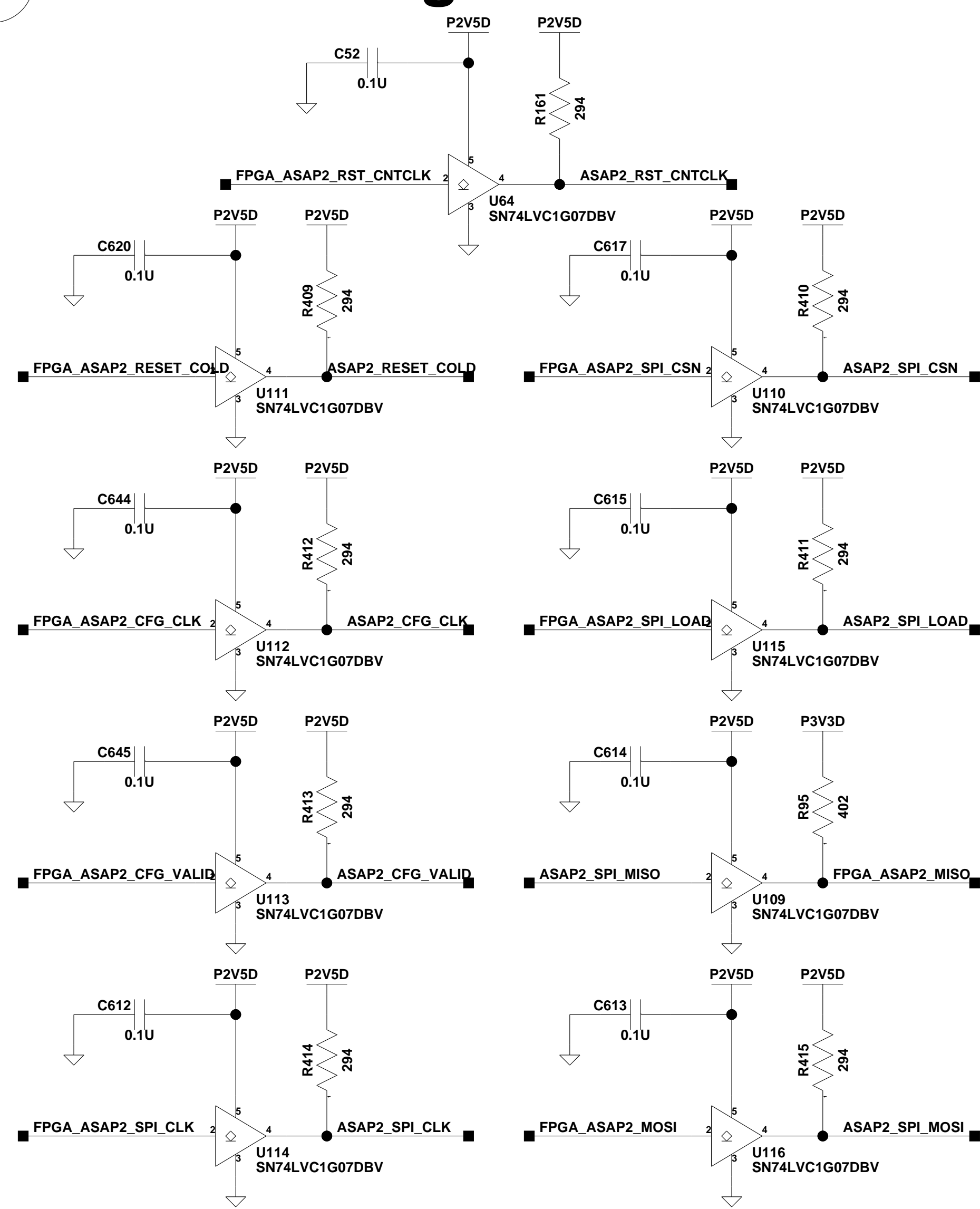
AsAP 2 Data Input

FPGA_ASAP2_REQ_IN 24-D1,24-E1,40-D3,40-E5

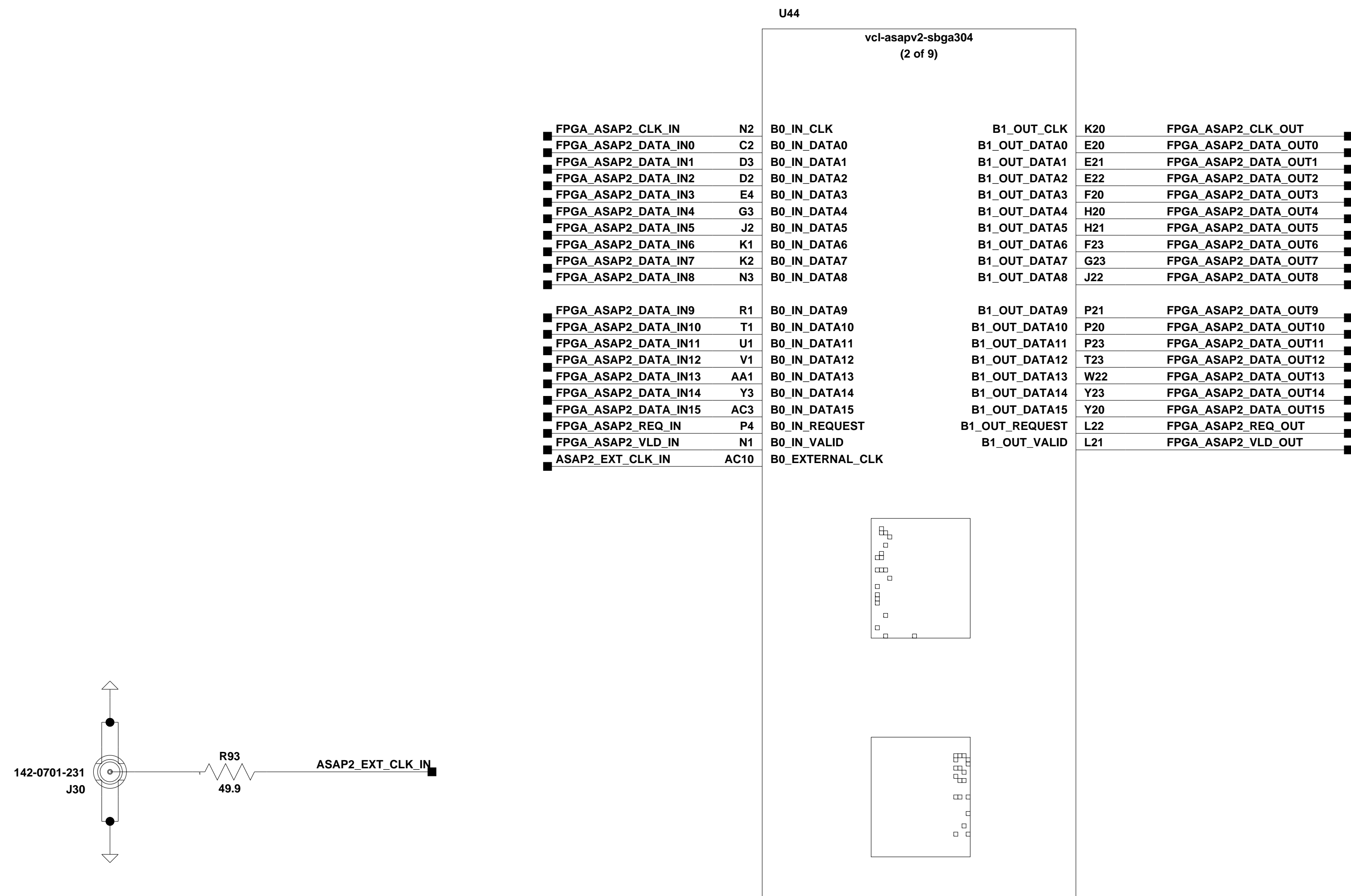
AsAP 2 Config Output

FPGA_ASAP2_MISO 15-C1,15-C3,40-C2,40-E5

A ASAP Config Level Translate



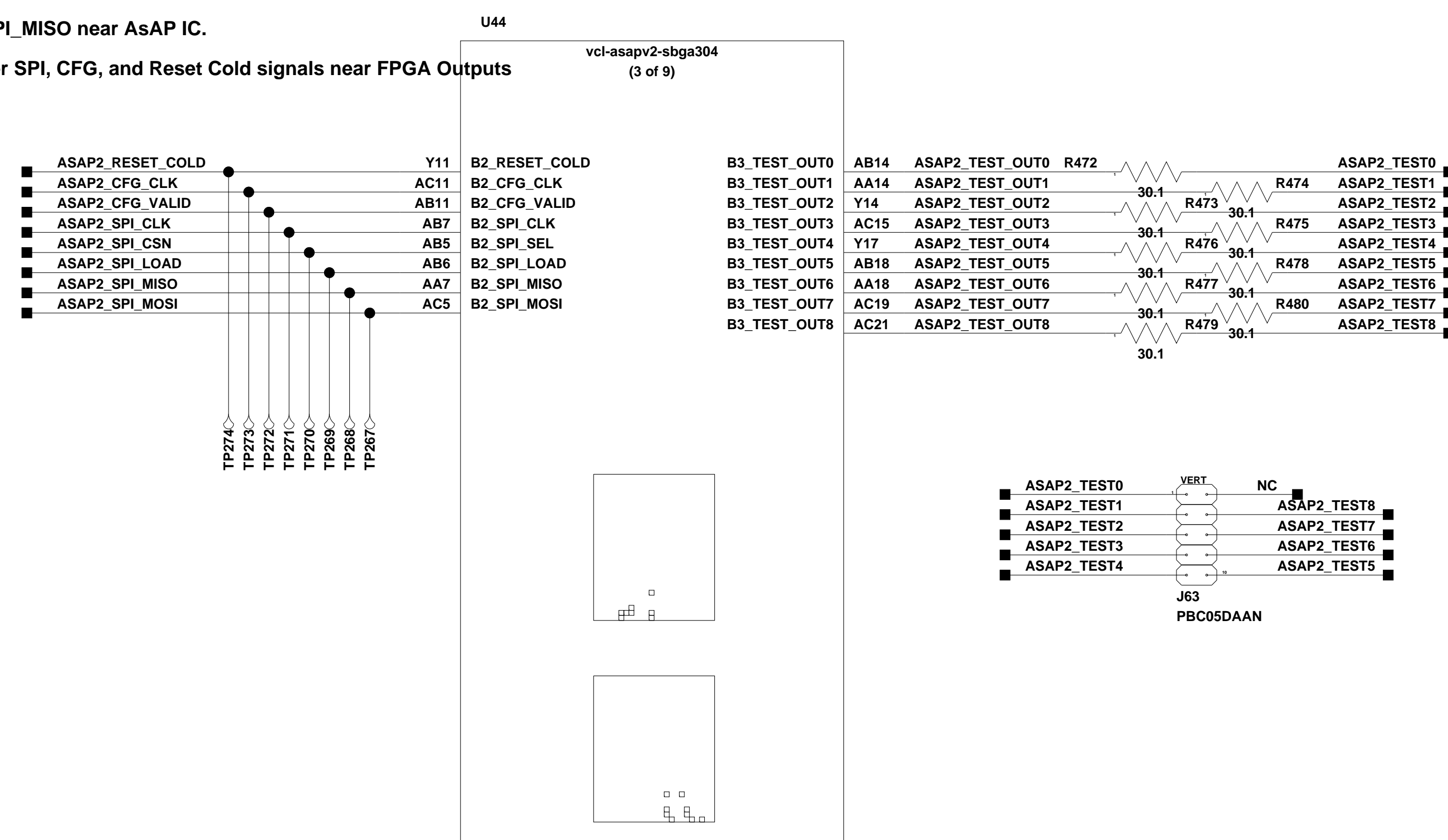
B ASAP Main Data Input and Output



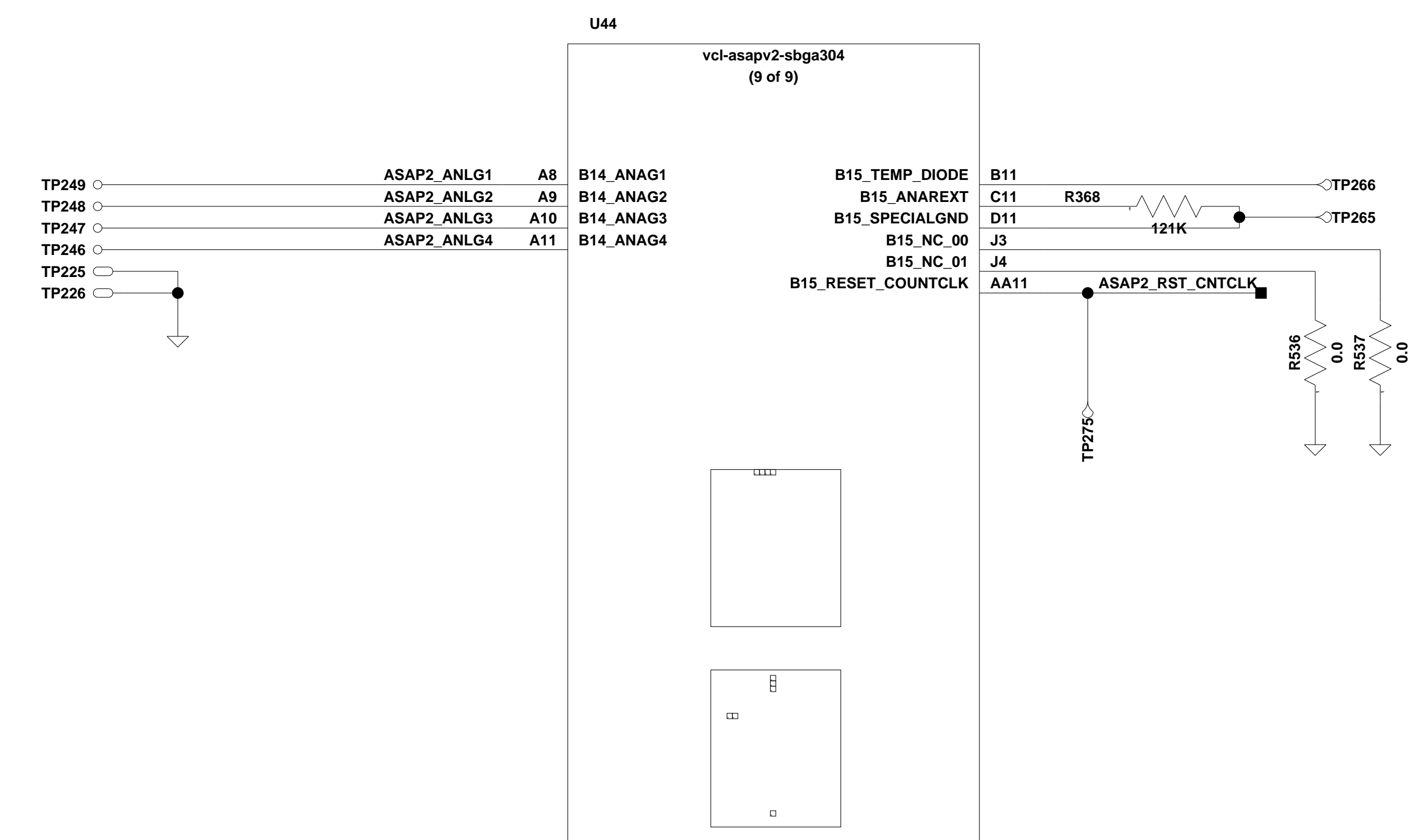
C ASAP Configuration and Test Port

Place 30.1 Ohm Series Resistor on AsAP SPI_MISO near AsAP IC.

Place 30.1 Ohm Series Resistors on all other SPI, CFG, and Reset Cold signals near FPGA Outputs



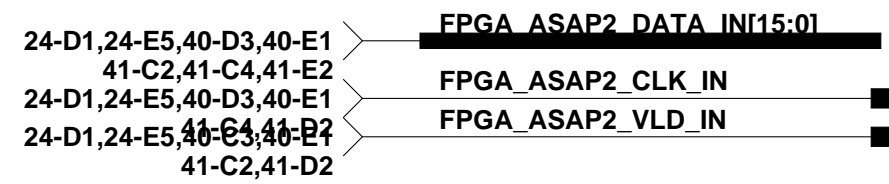
D ASAP Analog and Miscellaneous I/O



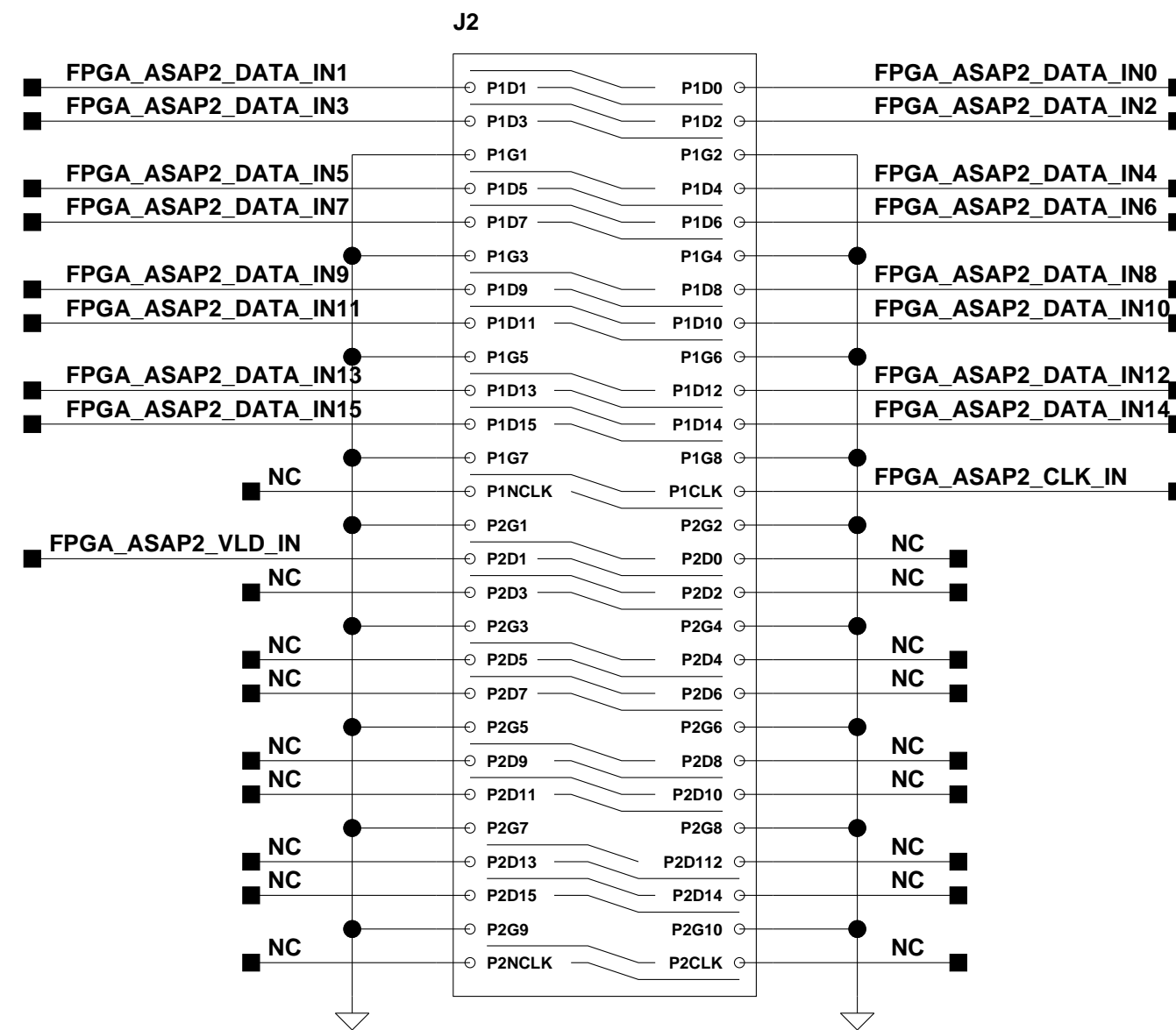
AGILENT 16902A Logic Analyzer E5390A SOFT-TOUCH CONNECTOR

** INPUTS **

AsAP 2 Data Input to Logic Analyzer

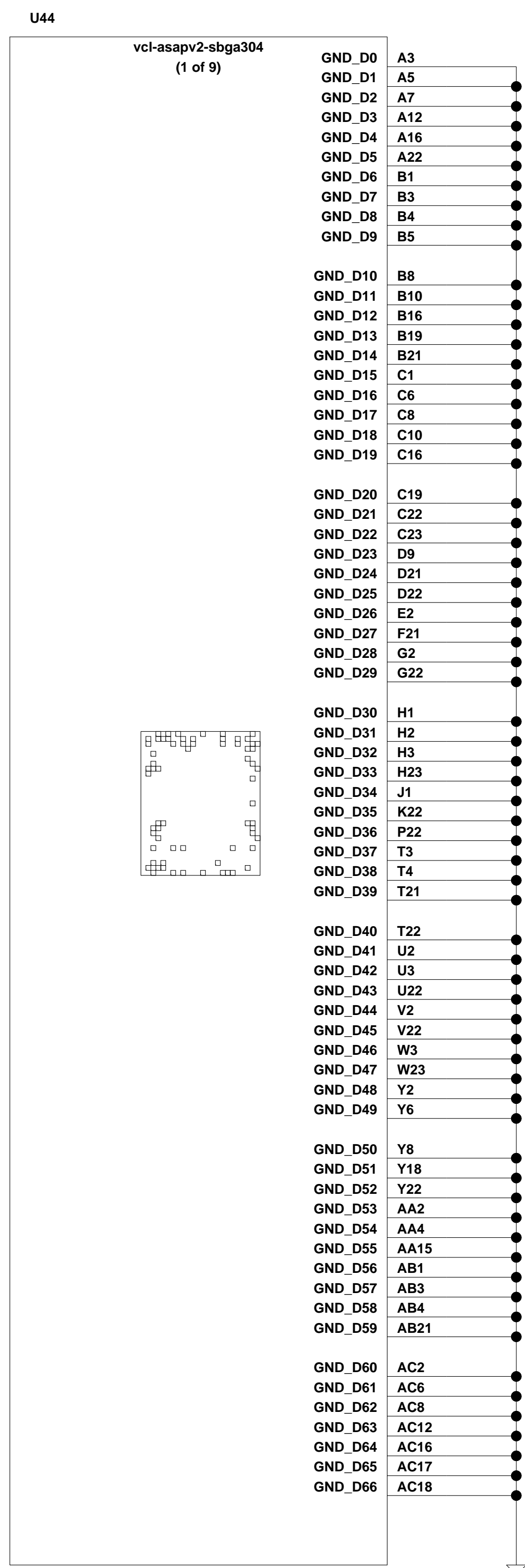
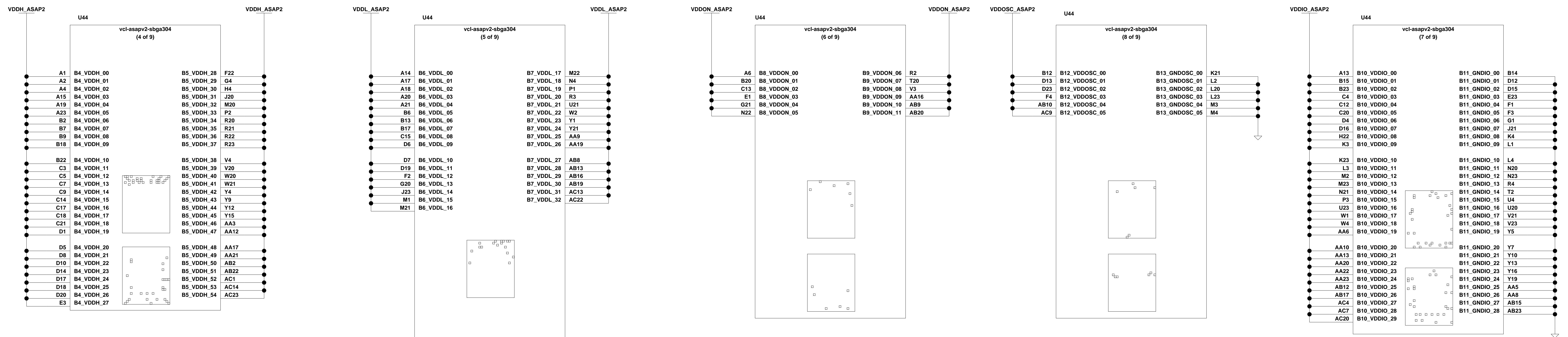


A SOFT-TOUCH SINGLE-ENDED PROBE (E5390A)



Title: AGILENT 16902A LOGIC ANALYZER E5390A SOFT-TOUCH CONNECTOR	
File: MEAS_MAIN_BOARD	
Created by: JEREMY W. WEBB	Date: 4-20-2009_13:35
Modified by:	Date:
PCB NO: 342	Size: C Sheet 41 of 43 REV: 001

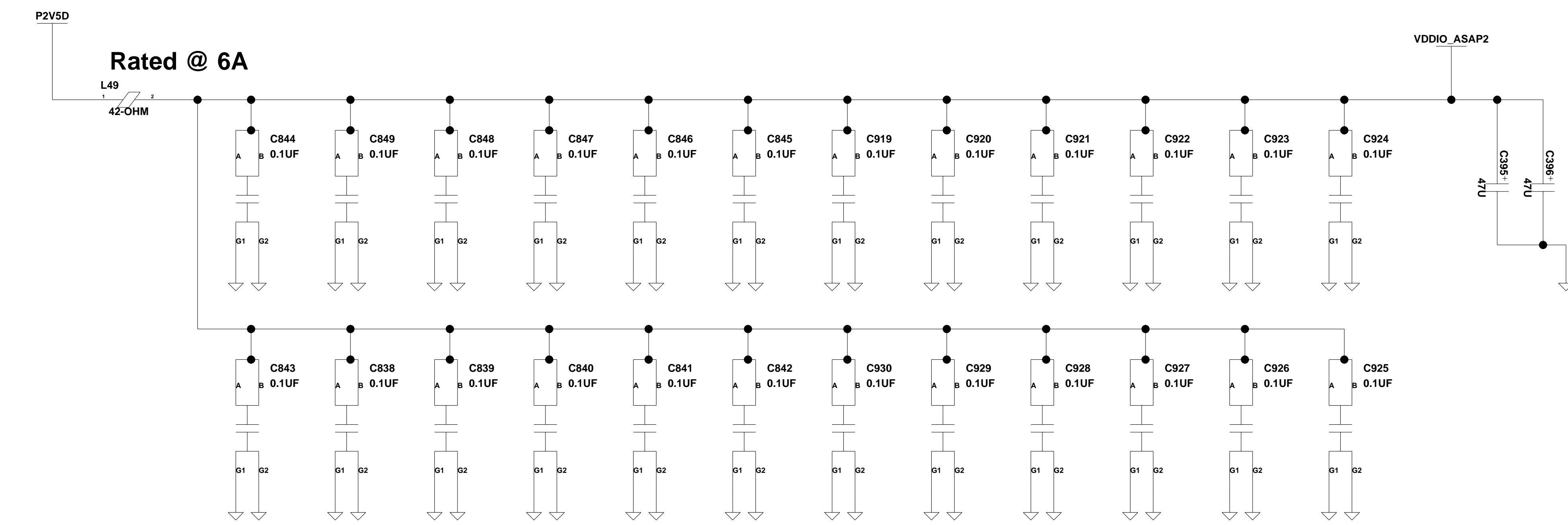
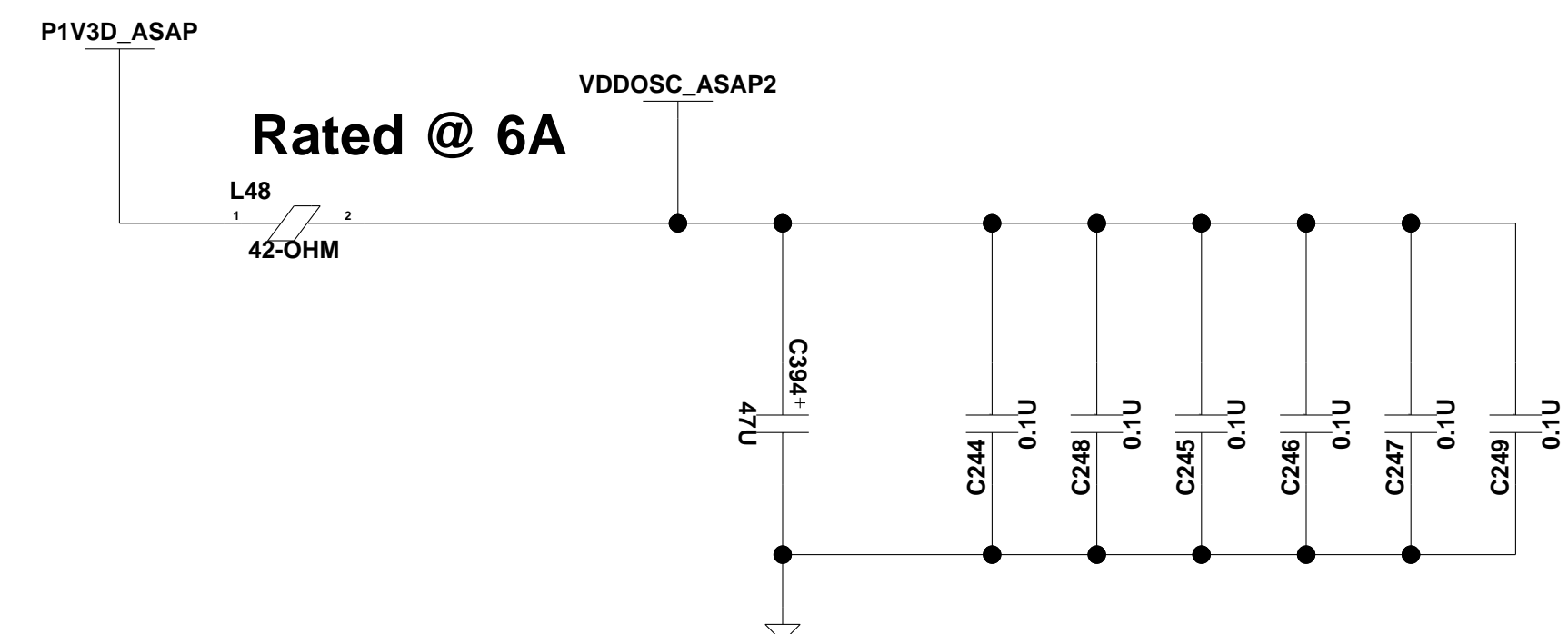
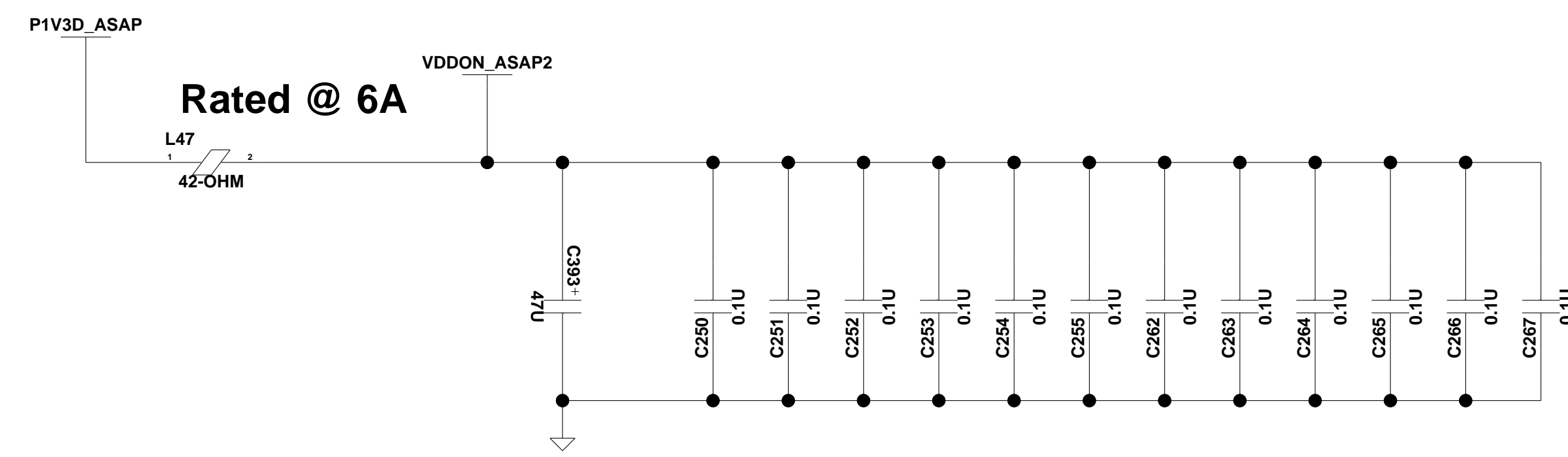
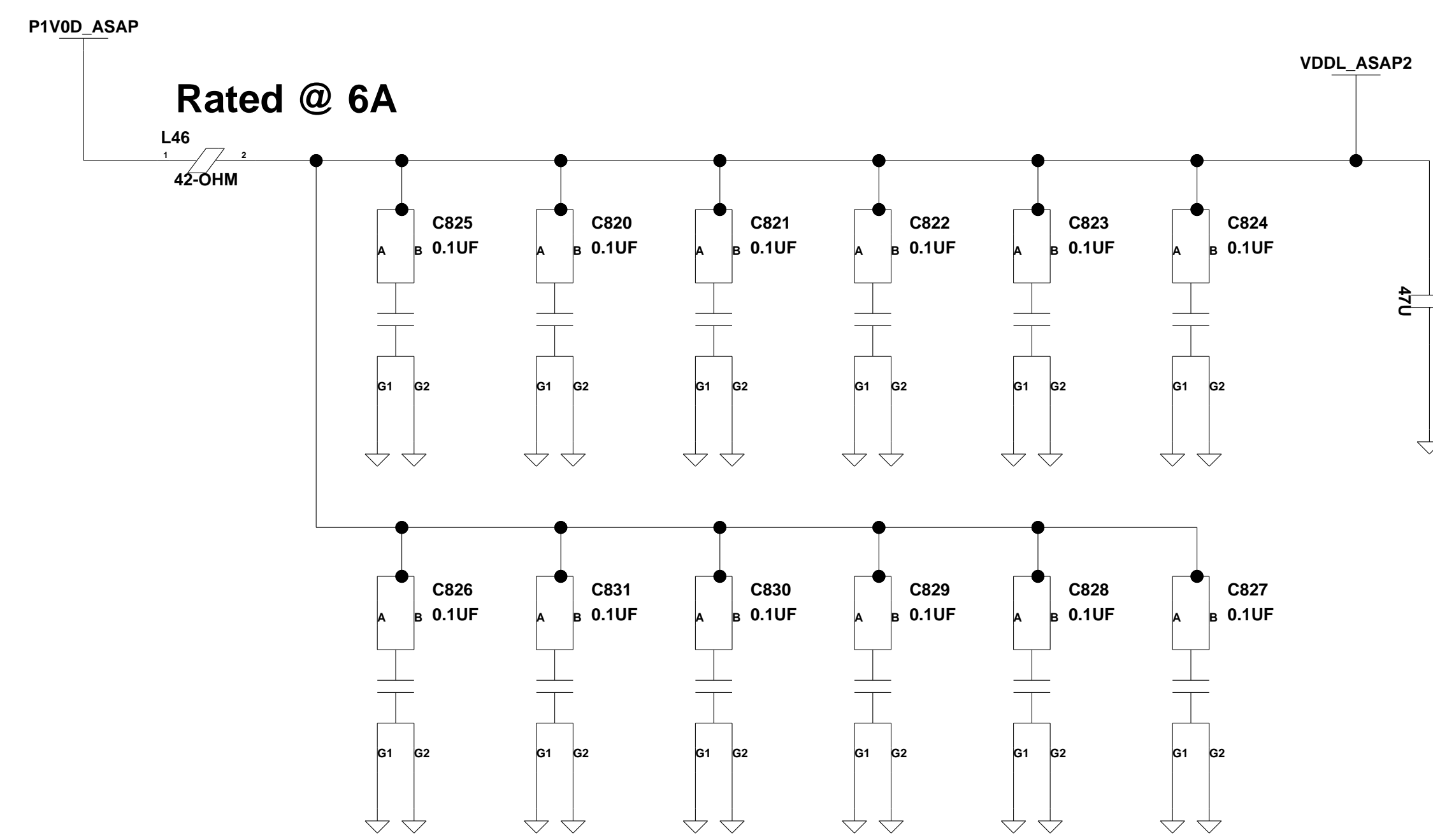
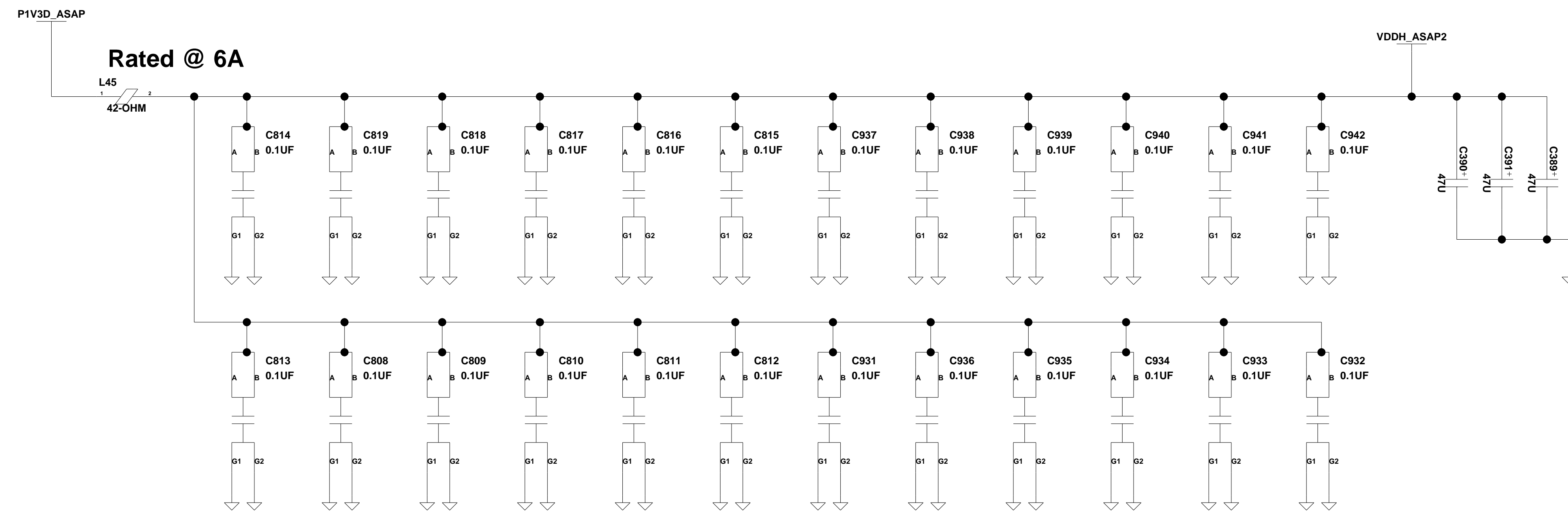
AsAPv2 #2 Power Supply Inputs



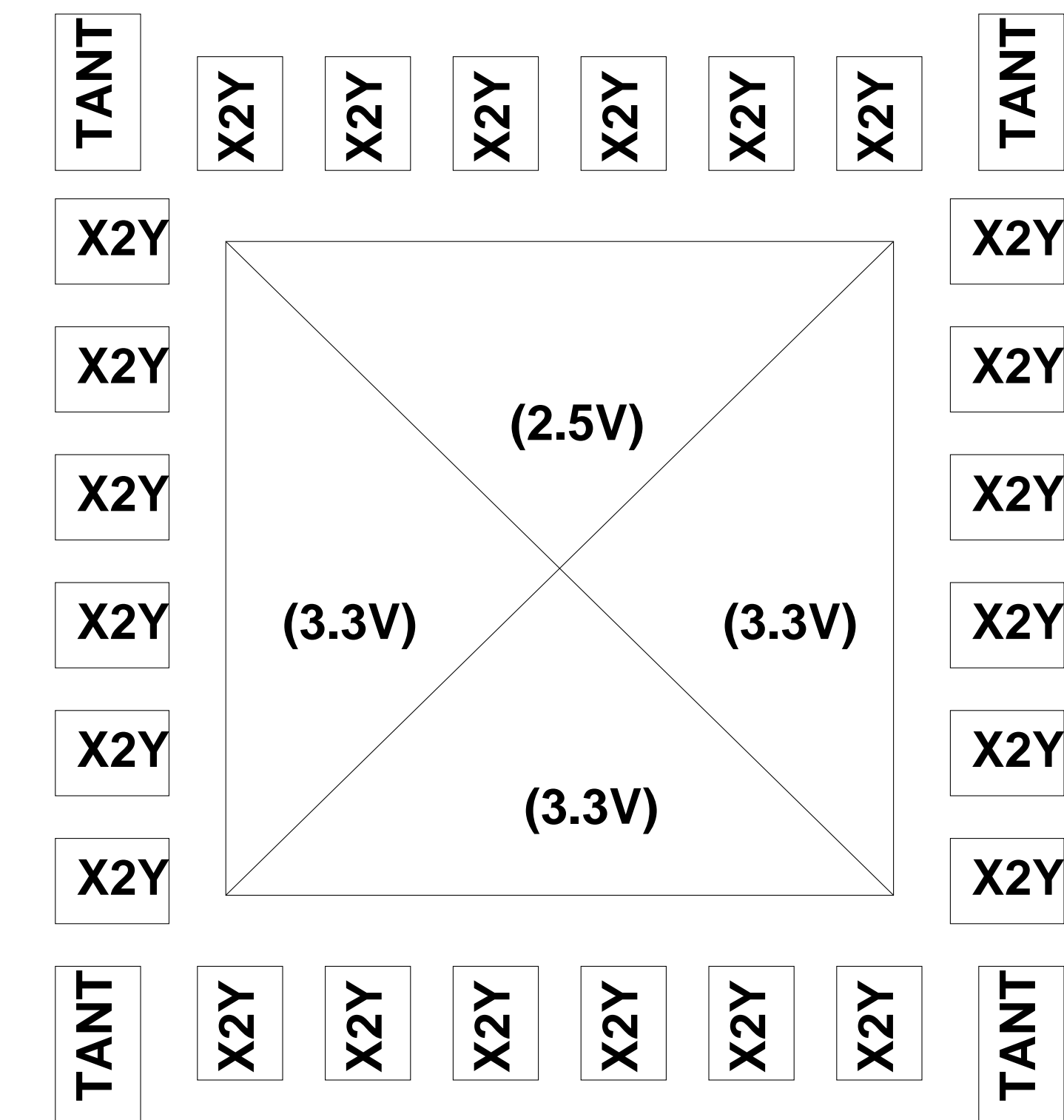
VLSI Computation LAB

Title: ASAPV2 #2 POWER SUPPLY INPUTS	
File: MEAS_MAIN_BOARD	
Created by: JEREMY W. WEBB	Date: 3-27-2009 12:24
Modified by:	Date:
PCB NO: 342	Size: E Sheet 42 of 43 REV: 001

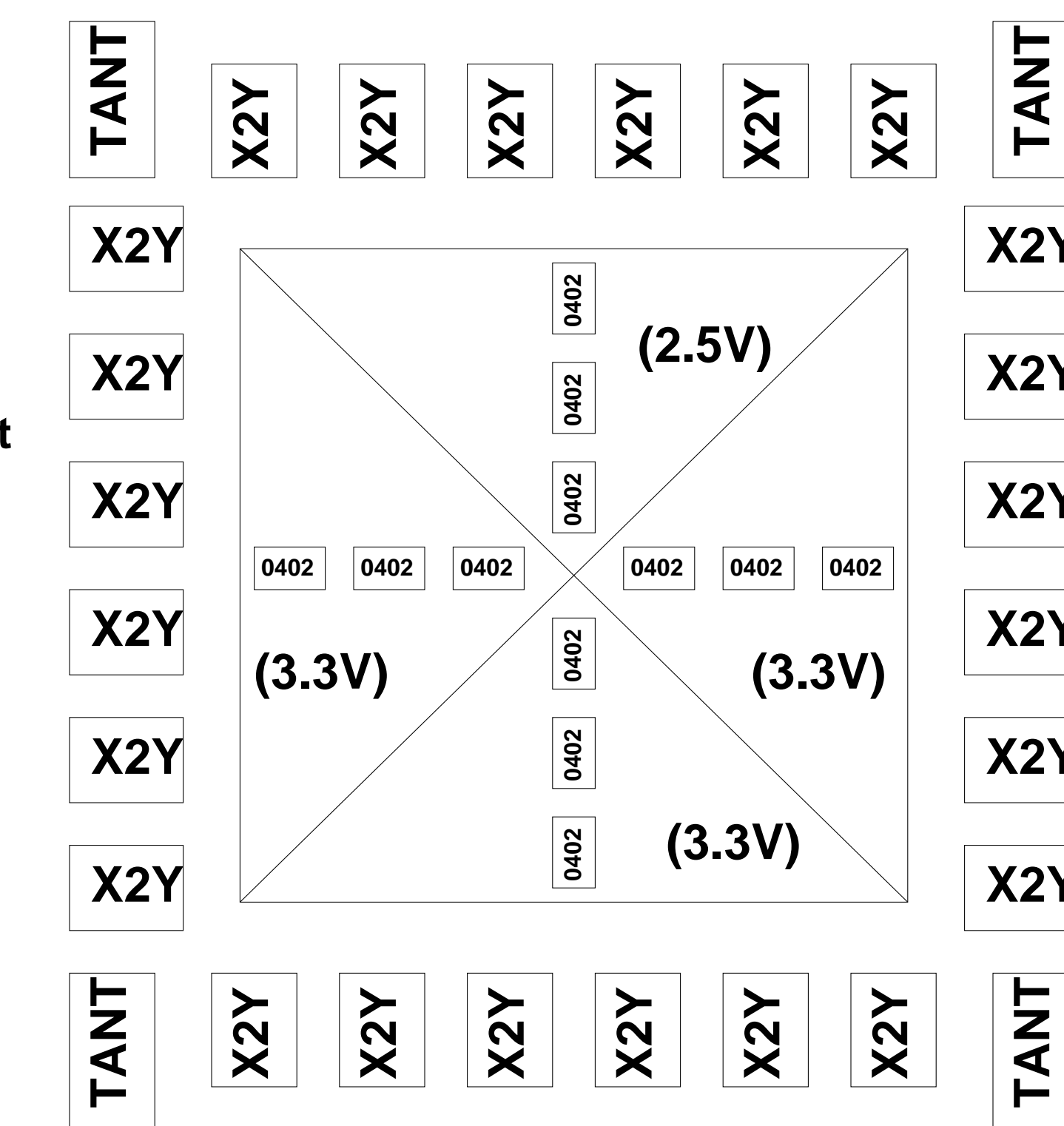
AsAPv2 #2 Power Supply Decoupling



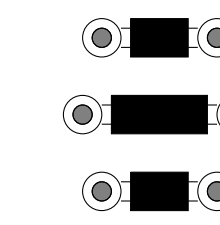
Capacitor Placement
(top side)



Capacitor Placement
(bottom side)



X2Y Capacitor Via Placement



Tantalum/O402 Via Placement

