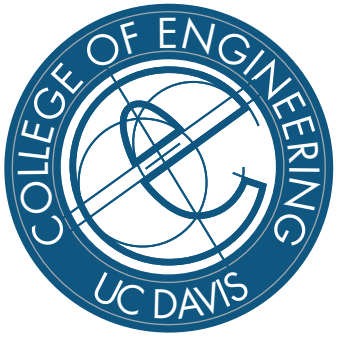

MSEE Thesis Project
Measurement Board ERS

Version: 1.04

Authors: Jeremy W. Webb

Email: jwwebb@ece.ucdavis.edu

Contents

List of Figures

List of Tables

Table 1: Revision History

Revision	Date	Description	Initials
1.00	06/12/2008	First Draft	JWW
1.01	09/18/2008	Updated Layout Constraints.	JWW
1.02	04/04/2009	Added Hardware Register Documentation.	JWW
1.03	04/26/2009	Updated Hardware Register Documentation and added FPGA Pinout.	JWW
1.04	11/21/2009	Removed Hardware Register Documentation. Added a list to FPGA Documentation.	JWW

1 Overview

This document is intended to document the requirements for my MSEE Thesis Measurement board. The purpose of the Measurement board is to demonstrate the DSP capabilities of the Asynchronous array of Simple Processors Version 2 (AsAPv2). The AsAPv2 is a 167-processor 65 nm computational platform well suited for DSP, communication, and multimedia workloads. It is made up of a homogeneous array of 164 programmable processors and 3 processors dedicated for signal processing:

1. Fast Fourier Transform (FFT)
2. Communication (Viterbi Decoder)
3. Multimedia (Video Motion Estimation)

The Measurement board contains an array of 2 AsAPv2 chips and supports several different operation modes:

1. Baseband Spectrum Analyzer
2. Oscilloscope
3. Arbitrary Waveform Generator
4. Signal Source
5. Network Analyzer

The operation mode can be changed on-the-fly, even when a signal is being measured. Each of the measurement boards operation modes will be described in Chapter 5.

The Measurement board receives +12V from a 125W Power Supply. For information on the power dissipation see Chapter 7. The Measurement board contains 6 temperature sensors arrayed across the board to monitor the temperature of the high-speed devices. For more information on Temperature Sensing refer to Section 5.2.10.

2 Reference Documents

2.1 Schematics

The Measurement board schematics are located at the following url:

http://jwebb-design/ucd_msee/schematics/meas_main_board.pdf

2.2 Datasheets and User Guides

2.2.1 Xilinx Virtex-5 SX50T

Manufacturer: Xilinx, Inc.
Manufactuers Part Number: XC5VSX50T-3FFG1136C

1. **Data Sheet**
   http://www.xilinx.com/support/documentation/data_sheets/ds100.pdf
2. **DC and Switching**
   http://www.xilinx.com/support/documentation/data_sheets/ds202.pdf
3. **User Guide**
   http://www.xilinx.com/support/documentation/user_guides/ug190.pdf
4. **Packaging and Pinout**
   http://www.xilinx.com/support/documentation/user_guides/ug195.pdf
5. **Configuration Guide**
   http://www.xilinx.com/support/documentation/user_guides/ug191.pdf
6. **PCB Designer's Guide**
   http://www.xilinx.com/support/documentation/user_guides/ug203.pdf
7. **System Monitor Guide**
   http://www.xilinx.com/support/documentation/user_guides/ug192.pdf

2.2.2 Xilinx Spartan-3A

Manufacturer: Xilinx, Inc.
Manufactuers Part Number: XC3S1400A-4FGG484C

1. **Data Sheet**
   http://www.xilinx.com/support/documentation/data_sheets/ds529.pdf
2. **User Guide**
   http://www.xilinx.com/support/documentation/user_guides/ug331.pdf
3. **Configuration Guide**
   http://www.xilinx.com/support/documentation/user_guides/ug332.pdf

2.2.3 Micron DDR2 SDRAM SODIMM

1. **MT16HTF25664HY-667E1 Data Sheet**
   http://download.micron.com/pdf/datasheets/modules/ddr2/HTF16C128_256x64H.pdf

2.2.4 Samsung QDR-II SRAM

1. **K7R323684C-EC250 Data Sheet**
   http://www.samsung.com/global/system/business/semiconductor/product/2007/7/30/948789ds_k7r32xx84c_rev11.pdf

2.2.5 Texas Instruments High-Speed 12-bit 500MS/s A/D Converter (ADC)

1. **ADS5463IPFP Data Sheet**
   http://focus.ti.com/lit/ds/symlink/ads5463.pdf

2.2.6 Texas Instruments High-Speed 16-bit 1GS/s D/A Converter (DAC)

1. **DAC5682ZIRGCT Data Sheet**
   http://focus.ti.com/lit/ds/symlink/dac5682z.pdf

2.2.7 Texas Instruments High-Speed Op-Amps

1. **THS4302RGT Data Sheet**
   http://focus.ti.com/lit/ds/symlink/ths4302.pdf
2. **THS4509RGTT Data Sheet**
   http://focus.ti.com/lit/ds/symlink/ths4509.pdf
3. **OPA695IDBV Data Sheet**
   http://focus.ti.com/lit/ds/symlink/opa695.pdf

2.2.8 Texas Instruments Power Supply Regulators and Sequencers

1. **PTH08T220WAZ Data Sheet**
   http://focus.ti.com/lit/ds/symlink/pth08t220w.pdf
2. **PTH08T260WAZ Data Sheet**
   http://focus.ti.com/lit/ds/symlink/pth08t260w.pdf
3. **PTH12050YAZ Data Sheet**
   http://focus.ti.com/lit/ds/symlink/pth12050y.pdf
4. **TPS79601 Data Sheet**
   http://focus.ti.com/lit/ds/symlink/tps79601.pdf
5. **TPS74201 Data Sheet**
   http://focus.ti.com/lit/ds/symlink/tps74201.pdf
6. **TPS73701 Data Sheet**
   http://focus.ti.com/lit/ds/symlink/tps73701.pdf
7. **LP2951D Data Sheet**
   http://focus.ti.com/lit/ds/symlink/lp2951.pdf
8. **TPS72301 Data Sheet**
   http://focus.ti.com/lit/ds/symlink/tps72301.pdf
9. **TL7733BCD Data Sheet**
   http://focus.ti.com/lit/ds/symlink/tl7733b.pdf
10. **TPS3808G25 Data Sheet**
    http://focus.ti.com/lit/ds/symlink/tps3808g25.pdf

2.2.9 Texas Instruments Temperature Sensors and Fan Controllers

1. **AMC6821 Data Sheet**
   http://focus.ti.com/lit/ds/symlink/amc6821.pdf
2. **TMP125 Data Sheet**
   http://focus.ti.com/lit/ds/symlink/tmp125.pdf

2.2.10 Analog Devices Clock PLL IC

1. **AD9516-3BCPZ Data Sheet**
   http://www.analog.com/UploadedFiles/Data_Sheets/AD9516_3.pdf

3 Measurement Board Block Diagrams

3.1 Xilinx Virtex-5 SX50T XC5VSX50T-3FF11356

The Measurement board uses a Xilinx Virtex-5 SX50T XC5VSX50T-3FF11356 FPGA for data path. The Data Path FPGA is responsible for:

- High-Speed 12-bit, 500MS/s ADC Interface
- High-Speed 16-bit, 1GS/s DAC Interface
- Polyphase, Decimate-by-2 Low-Pass Filter
- Polyphase, Interpolate-by-2 Low-Pass Filter
- AsAP Version 2 16-bit, 250MHz DSP Interface
- QDR-II SRAM 250MHz Memory Interface
- DDR2 SDRAM 250MHz SODIMM Memory Interface
- Arbitrary Waveform Storage and Retrieval
- FFT Post-Processing
- Spectrum Analysis Trigger Input
- Signal Source Trigger Output

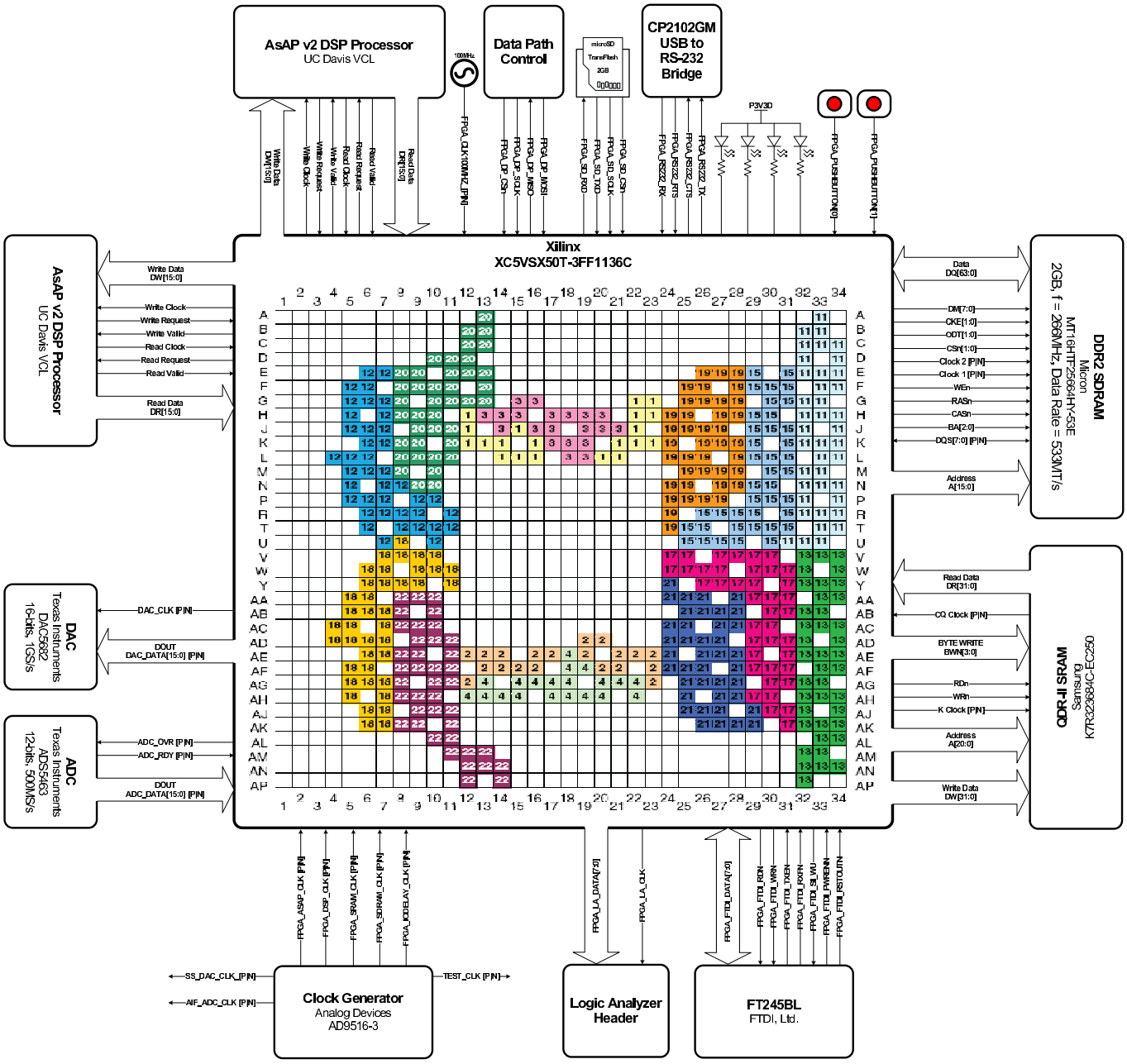

Figure 3.1: Measurement Board Data Path Block Diagram

3.2 Xilinx Spartan-3A XC3S1400A-4FGG484

The Measurement board uses a Xilinx Spartan-3A XC3S1400A-4FGG484 for the control implementation. The Control FPGA is responsible for:

- High-Speed 16-bit, 1Gs/s DAC Configuration
- AsAP Version 2 Configuration
- Data Path SPI Control Interface
- DDR SDRAM 100MHz Memory Interface
- AD9516-3 Clock Generation Configuration
- DDR2 SDRAM 250MHz SODIMM I^2C Configuration
- AMC6821 Fan Controller Configuration
- UI Board Control Interface
- FT245BL USB FIFO Interface
- Data Path Registers
- RS-232 Tx/Rx UARTs
- RS-232 User Interface Terminal

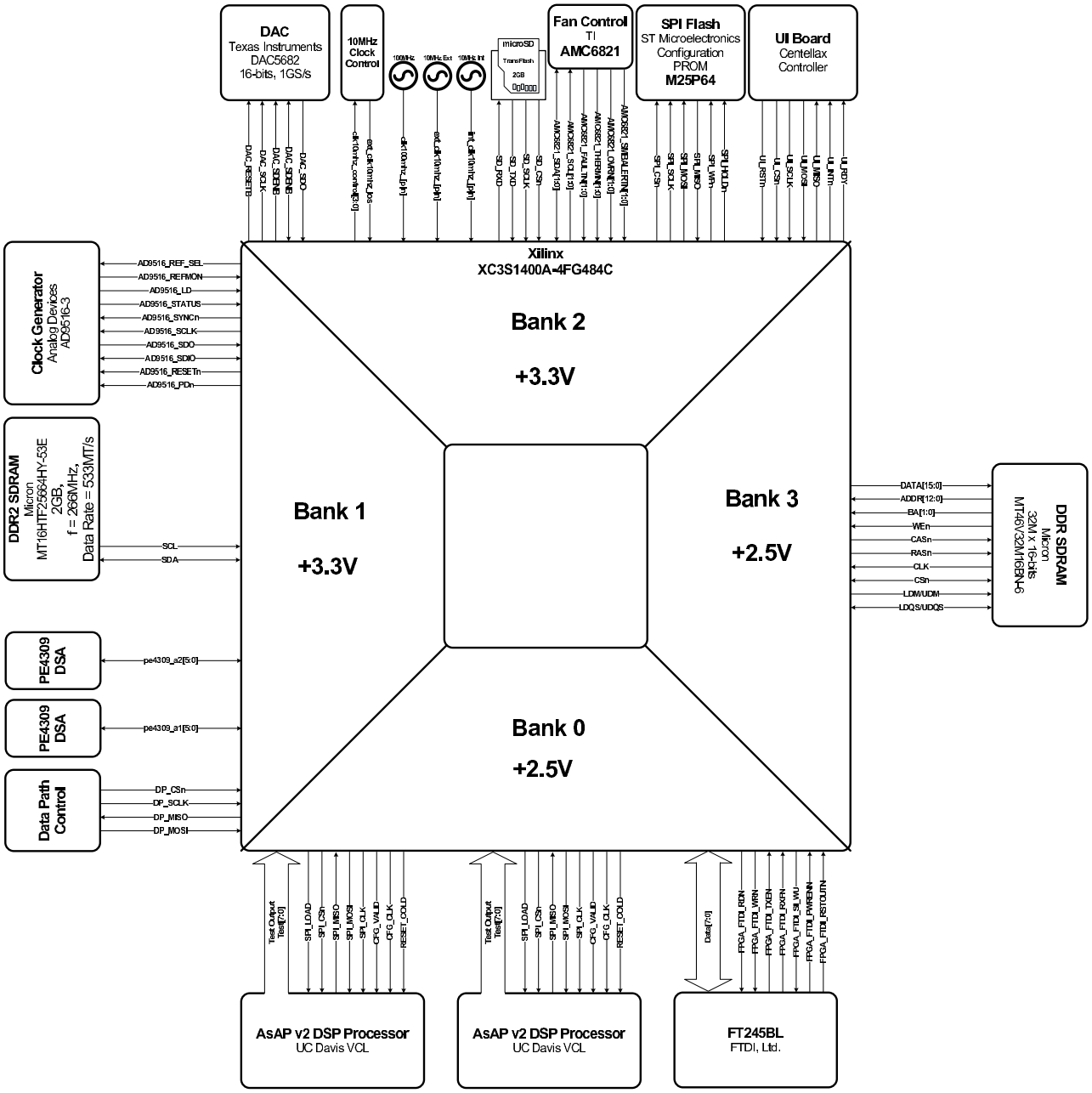

Figure 3.2: Measurement Board Control Block Diagram

4 AsAP Resources

4.1 AsAP Tasks

In order to determine how many AsAP Version 1 chips will be needed for the Measurement board, I will need to determine he number of AsAP resources required to do the biggest DSP task. The following DSP tasks will be performed by the AsAP processors:

1. Fast Fourier Transforms of length 8192 and 16384 samples.
2. Window FIR Filters: Hanning or Flat Top
3. Reconstruction FIR Filters
4. Signal Statistics: Minimum, Maximum, Average, Frequency, etc.

I will also need to determine if multiple FFT passes will be required, and figure out if AsAP can handle this sort of processing. It is possible that I will need to wait until AsAP Version 2 has been fabricated. Determine the length of FFTs required for Spectrum Analysis. For a maximum frequency of 120 MHz

5 Theory of Operation / Circuit Descriptions

5.1 Instrument Modes

The measurement board supports several different operation modes:

1. Spectrum Analyzer
2. Oscilloscope
3. Arbitrary Waveform Generator
4. Signal Source
5. Network Analyzer

The operation mode can be changed on-the-fly, even when a signal is being measured. Each of the measurement boards operation modes will be described in the following sections.

5.1.1 Spectrum Analyzer

In spectrum analyzer mode, the measurement board will use the on-board ADC to sample and digitize the time-domain data. The AsAP array will then perform an FFT of the digitized data in real-time.

The frequency resolution of the 120 MHz wide spectrum is calculated using the following equation:

$$FrequencyResolution = \frac{250\text{MHz}}{16384} = 15.2588\frac{\text{kHz}}{bin} \tag{5.1}$$

Dividing the frequency spectrum width by the number of points in the FFT yields the frequency resolution per bin. The amount of time required to capture 16384 samples of data is shown in Equation 5.2.

$$t_{capture} = \frac{16384\ Samples}{250\text{MHz}} = 65.536\mu seconds \tag{5.2}$$

As we can see by comparing Equations 5.1 and 5.2, the capture time is the inverse of the frequency resolution.

Another possibility is to oversample the ADC at 500 MHz. The oversample rate factor is shown in Equation 5.3.

$$\beta = \frac{f_s}{2 \cdot f_H} \tag{5.3}$$

where f_s is the sample rate and f_H is the highest frequency signal or the bandwidth. For a 500 MHz sample rate and a maximum frequency of 125 MHz, the oversample rate factor is 2. Using 4096 point FFTs to calculate over a million point FFT would require 256 individual FFTs. The total capture time to capture 2^{20} (or 1,048,576) samples of data is shown in Equation 5.4.

$$t_{capture} = \frac{1048576}{500\text{MHz}} = 0.002097152 = 2.097ms \tag{5.4}$$

The frequency resolution is shown in Equation 5.5.

$$FrequencyResolution = \frac{500\text{MHz}}{1048576} = 476.8372\text{Hz} \tag{5.5}$$

Oversampling the data by 2 allows the design of the anti-alias filter to be simplified. The transition band for a sample rate of 500 MHz is calculated in Equation 5.6.

$$f_{transition\ band} = f_s - 2 \cdot f_H = 500\text{MHz} - 2 \cdot 125\text{MHz} = 500\text{MHz} - 250\text{MHz} = 250\text{MHz} \tag{5.6}$$

For a sample rate of 250 MHz, the transition band would be 10 MHz. Comparing a transition band of 10 MHz to 250 MHz, we can see that the anti-alias filter does indeed become simpler. Normally, a sample rate is chosen such that the maximum input frequency is no more than 50% of the Nyquist frequency to avoid aliasing. For this design it is more likely that f_H will be 120 MHz, so for a 500 MHz sample rate we will use 48% of the Nyquist frequency and $f_{transition\ band}$ will be 260 MHz. The fact that we're oversampling will make this design a lot simpler. Due to the oversample process, we are required to decimate the digitized ADC data by 4 inside of the FPGA before sending the data to the AsAP array for the FFT processing. The TI ADS5463 500 MS/s ADC will be required in order to use a sample rate of 500 MHz. However, the ADS5463 ADC has only 12-bits of resolution, and 10.5 effective bits with an input signal $\leq$ 125 MHz. The theoretical SNR of the ADS5463 is 65 dB.

5.1.2 Oscilloscope

In oscilloscope mode, the measurement board will be process the time-domain data and perform statistical measurements. The data processing will consist of triggering and span adjustment. The statistical measurements involve analyzing the time-domain data in order to determine minimum/maximum amplitude, frequency, period, duty-cycle.

5.1.3 Arbitrary Waveform Generator

In arbitrary waveform generator mode, the measurement board will utilize the on-board AsAP array to generate sinusoidal, square, and triangle waveforms. In addition a user-defined waveform can be generated. The user-defined waveform will be stored in memory, and will be played back at the users request.

5.1.4 Signal Source

In signal source mode, the measurement board will use the on-board FPGA and DAC to perform direct-digital synthesis. The user will select a frequency, which will be translated to a frequency word for the DDS module residing in the FPGA. The maximum frequency sinisoidal waveform that can be generated is limited to the bandwidth of the reconstruction filter on the output of the DAC. The sample rate of the DAC is 500 MHz and the 3dB frequency is 133MHz, which means any signal between DC and 120 Mhz can be generated.

5.1.5 Network Analyzer

In network analyzer mode, the measurement board uses both te input and output to analyze the two port network. A sinusoidal signal is generated by the DAC and driven through the DUT being measured, then the DUT output is driven into the ADC.

5.2 Measurement Board Overview

This section describes the measurement board used in general purpose instrument. The measurement board is a single input, single output design. It contains a single input ADC with 12-bits resolution [1]. The baseband input has a bandwidth of 120MHz. The sampled input data is driven into an FPGA, where it can be routed to several different locations.

1. DDR2 SDRAM Capture Memory [2]
2. QDR-II SRAM Capture Memory [3]
3. AsAP Array for real time processing

Once the data is written to memory it is sent to the AsAP array to be processed. Once the digital signal processing is complete, the data can be sent to several different locations.

1. DDR2 SDRAM SDRAM Display Memory [2]
2. QDR-II SRAM Display Memory [3]

When the MicroBlaze Display Application is ready to display the next signal trace, it reads the processed data out of display memory located on the measurement board. The MicroBlaze Display Application communicates with the display via RS-232 commands.

In Spectrum Analyzer mode, the on-board DAC can be used as a tracking generator. The DAC has a resolution of 16-bits and a bandwidth of 120MHz.

5.2.1 Primary Power Supply Filtering

The main job of these filters is to keep noise generated on the board from polluting the instrument. Its secondary purpose is to remove instrument noise. Additional filtering is located near sensitive or noisy circuits.

5.2.2 JTAG Connector

The JTAG connector on the Measurement board serves several functions.

1. Allows reprogramming of the Xilinx Virtex 4 FPGA, Spartan 3 FPGA and Configuration PROM via a Xilinx PC4 programming cable.
2. Allows for logic analysis debug using ChipScope Pro and the Xilinx PC4 programming cable.

5.2.3 Data Path FPGA

The measurement board contains a single Xilinx Virtex-5 SX50T (XC5VSX50T-3FF1136).

5.2.3.1 FPGA Modules

- AsAP Write Data Module (x2)
- AsAP Read Data Module (x2)
- DDR2 SDRAM Memory Controller (x1)
- QDR-II SRAM Memory Controller (x1)
- microSD Card 2GB Memory Controller (x1)
- ADC FIR Low-Pass Decimation Filter (x1)
- MicroBlaze processor for USB/RS-232 interface, Display Control, and register peek/poke.

5.2.4 Control FPGA

The measurement board contains a single Xilinx Spartan-3A (XC3S1400A-4FGG484).

5.2.4.1 FPGA Modules

- microSD Card 2GB Memory Controller (x1)
- AD9516-3 Configuration Module
- DAC5682Z Configuration Module
- ACM6821 Fan Controller Configuration Module
- AsAP Configuration Module (x2)
- MicroBlaze processor for USB/RS-232 interface, AsAP Configuration, and register peek/poke.

5.2.5 Analog-to-Digital Converter

For most of the instrument modes dynamic range is very important; however, both high resolution and high sample rate in a single Analog-to-Digital Converter (ADC) are hard to find. A compromise was made for the measurement board to choose sample rate over resolution. A Texas Instruments 12-bit, 500MS/s ADC was chosen as the digitizer[1].

5.2.6 Digital-to-Analog Converter

For most of the instrument modes dynamic range is very important; however, both high resolution and high sample rate in a single Digital-to-Analog Converter (DAC) are hard to find. A trade-off must be made between sample rate and resolution. A Texas Instruments 16-bit, 1GS/s DAC was chosen for the signal output[4].

5.2.7 Clock Generation

The following Clock Generator is being used on the measurement board:

1. Analog Devices AD9516-3 14-Output Clock Generator with Integrated 2.0 GHz VCO [5]
   http://www.analog.com/UploadedFiles/Data_Sheets/AD9516_3.pdf

The Universal Microwave Corp UMX Series 1GHz VCO is used to drive the AD9516-3 External Clock Input.

- UMX-244-B14

5.2.8 Memory

There are a couple of options for capture/display memory on the measurement board. The obvious option is to use SODIMM SDRAM (i.e., laptop memory sticks), but these can prove hard to satisfy timing constraints in FPGAs. Recently, SD Cards have been made with capacities up to 16 GB. It provides the ability to take a microSD Card and transfer its contents to a Linux or Windows PC for further analysis via Matlab or other tools.

5.2.8.1 DDR2 SDRAM

Laptop DDR2 SDRAM SODIMM packages are small enough that I could fit up to one 2 Gigabyte sticks on a single measurement board.

5.2.8.2 QDR-II SRAM

A single measurement board contains 36 Mb of QDR-II SRAM, which provides simultaneous read and write at a rate of 250MS/s.

5.2.8.3 microSD Card

The microSD Card connector would take up one third as much space as the sodimm connector. The interface speed may be a limitation, but it would provide more portability of the sampled data.

5.2.9 AsAP Chip Array

The array of 2 AsAP chips has the job of performing the majority of the DSP processing on the Measurement board. When the Measurement board is in Spectrum Analyzer mode, the AsAP array will be performing the FFT on the incoming real-time data. When in the Oscilloscope mode, the AsAP array will be performing the real-time data statistics such as minimum and maximum amplitude and frequency. When in Arbitrary Waveform mode, the AsAP array will be in charge of generating the desired waveform whether it be square, sinusoid, triangle, or user defined. In the case of a user defined waveform, the AsAP will read in the desired waveform from the FPGA and play the waveform back.

5.2.10 Temperature Sensing

The Measurement board contains 9 digital temperature sensors in a 3x3 array. The Texas Instruments TMP125 [6] digital temperature sensor is accurate to $2^{\circ}\mathrm{C}$ over a temperature range of -25$^{\circ}\mathrm{C}$ to $+85^{\circ}\mathrm{C}$, and is controlled using a serial peripheral interface (SPI). The temperature measurement is made with a 10-bit resolution Delta-Σ Analog to Digital Converter, which translates to a temperature resolution of $0.25^{\circ}\mathrm{C}$. A block diagram of the TMP125 temperature sensor is shown in Figure 5.1.

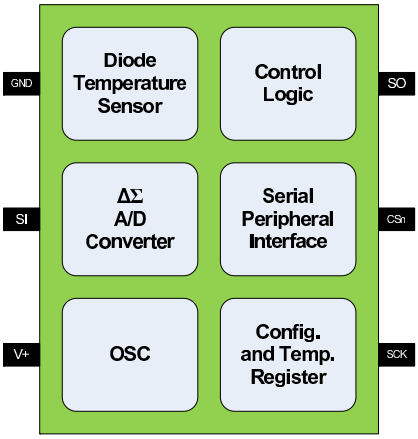

Figure 5.1: $2^{\circ}\mathrm{C}$ Accurate Digital Temperature Sensor with SPI Interface

An application running on the MicroBlaze 32-bit Soft-Core Processor will periodically sample the temperature of all nine sensors to determine if a temperature calibration is required for the various high-speed devices. Upon characterization of the Measurement board during normal operation within a Chassis, a set of temperature limits will be defined that denote when a recalibration is necessary. It is possible that there may be only three temperature zones:

1. Too Cold!!
2. Normal Operation
3. Too Hot!!

However, more zones may be necessary depending on the environment and performance limitations of the high-speed devices.

6 FPGA Pinouts

6.1 Data Path FPGA Pinout

The Measurement board contains an Xilinx Virtex-5 SX50T FPGA for controlling the high-speed circuitry. The Xilinx part number is: XC5VSX50T-3FFG1136C.

Table 6.1: Virtex-5 SX50T (XC5VSX50T-3FFG1136C) FPGA Pin Out

Virtex-5 SX50T (XC5VSX50T-3FFG1136C) FPGA Pin Out			
Signal Name	**Bank**	**Pin**	**Description**
Bank 0: 27 Pins			
Bank Voltage: +3.3V			
P3V3D_V5	0	AA22	VCCO_0
P3V3D_V5	0	AD23	VCCO_0
No Connect	0	W18	DXP_0
No Connect	0	W17	DXN_0
P2V5REF_FPGA	0	T18	AVDD_0
GNDA_FPGA	0	T17	AVSS_0
VP_VN_SM	0	U18	VP_0
VP_VN_SM	0	V17	VN_0
P2V5REF_FPGA	0	V18	VREFP_0
GNDA_FPGA	0	U17	VREFN_0
P3V3D_V5	0	L23	VBATT_0
V5_PROG_B	0	M22	PROGRAM_B_0
VS_HSWAPEN	0	M23	HSWAPEN_0
S3A_SPI_DATA_TO_V5	0	P15	D_IN_0
V5_CONFIG_DONE	0	M15	DONE_0
V5_CCLK	0	N15	CCLK_0
V5_INIT_B	0	N14	INIT_B_0
FPGA_CS_B	0	N22	CS_B_0
FPGA_RDWR_B	0	N23	RDWR_B_0
GND	0	AB23	RSVD_D0
GND	0	AC23	RSVD_D1
TCK	0	AB15	TCK_0
V5_M[0]	0	AD21	M0_0
V5_M[2]	0	AD22	M2_0
V5_M[1]	0	AC22	M1_0
TMS	0	AC14	TMS_0
TDI_TO_V5	0	AC15	TDI_0
No Connect	0	AD15	D_OUT_BUSY_0
TDO_TO_JTAG	0	AD14	TDO_0
Bank 1: 20 Pins			
Bank Voltage: +3.3V			
P3V3D_V5	1	D13	VCCO_1
P3V3D_V5	1	G14	VCCO_1
FPGA_V5_FTDI_DATA[6]	1	G22	IO_L4P_A11_D27_1
FPGA_DP_CTRL_RNW	1	G23	IO_L8P_CC_A3_D19_1
FPGA_DP_CTRL_DATA_CSN	1	H12	IO_L7N_A4_D20_1
			Continued on Next Page...

Virtex-5 SX50T (XC5VSX50T-3FFG1136C) FPGA Pin Out			
Signal Name	**Bank**	**Pin**	**Description**
FPGA_V5_FTDI_DATA[5]	1	H22	IO_L4N_VREF_A10_D26_1
FPGA_DP_CTRL_GPIO[2]	1	H23	IO_L8N_CC_A2_D18_1
FPGA_V5_FTDI_DATA[0]	1	J12	IO_L7P_A5_D21_1
FPGA_V5_FTDI_DATA[7]	1	J15	IO_L3N_A12_D28_1
FPGA_V5_FTDI_RDN	1	J22	IO_L2P_A15_D31_1
FPGA_DP_CTRL_GPIO[0]	1	K12	IO_L9N_CC_A0_D16_1
FPGA_DP_CTRL_GPIO[1]	1	K13	IO_L9P_CC_A1_D17_1
FPGA_V5_FTDI_DATA[3]	1	K14	IO_L5N_A8_D24_1
FPGA_V5_FTDI_SI_WU	1	K16	IO_L3P_A13_D29_1
FPGA_V5_FTDI_WRN	1	K21	IO_L2N_A14_D30_1
FPGA_V5_FTDI_DATA[1]	1	K22	IO_L6N_A6_D22_1
FPGA_V5_FTDI_DATA[2]	1	K23	IO_L6P_A7_D23_1
FPGA_V5_FTDI_DATA[4]	1	L14	IO_L5P_A9_D25_1
FPGA_V5_FTDI_PWRENN	1	L15	IO_L1P_A17_1
FPGA_V5_FTDI_RSTOUTN	1	L16	IO_L1N_A16_1
FPGA_V5_FTDI_RXFN	1	L20	IO_L0N_A18_1
FPGA_V5_FTDI_TXEN	1	L21	IO_L0P_A19_1
Bank 2: 20 Pins			
Bank Voltage: +3.3V			
P3V3D_V5	2	AH21	VCCO_2
P3V3D_V5	2	AM19	VCCO_2
FPGA_LA_DATA[7]	2	AE12	IO_L0N_CC_RS0_2
FPGA_LA_CLK	2	AE13	IO_L0P_CC_RS1_2
FPGA_LA_DATA[0]	2	AE14	IO_L4P_FCS_B_2
No Connect	2	AE16	IO_L6N_D6_2
V5_FS2	2	AE17	IO_L8N_D2_FS2_2
V5_FS1	2	AE19	IO_L9P_D1_FS1_2
V5_FS0	2	AD19	IO_L9N_D0_FS0_2
FPGA_V5_PUSHBUTTON[0]	2	AD20	IO_L7N_D4_2
FPGA_V5_PUSHBUTTON[1]	2	AE21	IO_L7P_D5_2
FPGA_LA_DATA[2]	2	AE22	IO_L3P_A21_2
FPGA_LA_DATA[1]	2	AE23	IO_L3N_A20_2
FPGA_LA_DATA[4]	2	AF13	IO_L2P_A23_2
No Connect	2	AF14	IO_L4N_VREF_FOE_B_MOSI_2
No Connect	2	AF15	IO_L6P_D7_2
No Connect	2	AF16	IO_L8P_D3_2
No Connect	2	AF20	IO_L5P_FWE_B_2
No Connect	2	AF21	IO_L5N_CSO_B_2
FPGA_LA_DATA[6]	2	AF23	IO_L1P_CC_A25_2
FPGA_LA_DATA[3]	2	AG12	IO_L2N_A22_2
FPGA_LA_DATA[5]	2	AG23	IO_L1N_CC_A24_2
Bank 3: 20 Pins			
Bank Voltage: +3.3V			
P3V3D_V5	3	D23	VCCO_3
P3V3D_V5	3	E20	VCCO_3
FPGA_BANK3_VRN	3	G15	IO_L2P_GC_VRN_3
FPGA_BANK3_VRP	3	G16	IO_L2N_GC_VRP_3
FPGA_V5_SD_BUSY_LED	3	H13	IO_L8N_GC_3
FPGA_DP_CTRL_SCK	3	H14	IO_L6P_GC_3
FPGA_V5_SD_RXD	3	H15	IO_L6N_GC_3
			Continued on Next Page...

Virtex-5 SX50T (XC5VSX50T-3FFG1136C) FPGA Pin Out			
Signal Name	**Bank**	**Pin**	**Description**
FPGA_V5_RS232_RTS	3	H17	IO_L0P_CC_GC_3
FPGA_V5_RS232_RX	3	H18	IO_L0N_CC_GC_3
No Connect	3	H19	IO_L9P_GC_3
No Connect	3	H20	IO_L9N_GC_3
FPGA_V5_SD_CARD_DETECT	3	J14	IO_L8P_GC_3
FPGA_DP_CTRL_MOSI	3	J16	IO_L4P_GC_3
FPGA_DP_CTRL_SRQN	3	J17	IO_L4N_GC_VREF_3
FPGA_DP_CTRL_MISO	3	J19	IO_L3N_GC_3
FPGA_V5_SD_TXD	3	J20	IO_L7P_GC_3
FPGA_V5_SD_CLK	3	J21	IO_L7N_GC_3
FPGA_V5_RS232_TX	3	K17	IO_L1P_CC_GC_3
FPGA_DP_CTRL_ADDR_CSN	3	K18	IO_L3P_GC_3
FPGA_BOARD_RSTN	3	K19	IO_L5N_GC_3
FPGA_V5_RS232_CTS	3	L18	IO_L1N_CC_GC_3
FPGA_DP_CTRL_RSTN	3	L19	IO_L5P_GC_3
Bank 4: 20 Pins			
Bank Voltage: +2.5V			
P2V5D_V5	4	AG14	VCCO_4
P2V5D_V5	4	AL12	VCCO_4
FPGA_TRIG_OUT_N	4	AE18	IO_L8N_CC_GC_4
FPGA_TRIG_OUT_P	4	AF18	IO_L8P_CC_GC_4
FPGA_DEBUG_LEDS[0]	4	AF19	IO_L6N_GC_4
FPGA_DSP_CLKIN_N	4	AG13	IO_L1N_GC_D12_4
FPGA_DEBUG_LEDS[2]	4	AG15	IO_L5N_GC_4
FPGA_TRIG_IN_N	4	AG16	IO_L7N_GC_VRP_4
FPGA_AUX_IN_N	4	AG17	IO_L9N_CC_GC_4
FPGA_DEBUG_LEDS[1]	4	AG18	IO_L6P_GC_4
FPGA_CLK100MHZ_N	4	AG20	IO_L4N_GC_VREF_4
FPGA_CLK100MHZ_P	4	AG21	IO_L4P_GC_4
FPGA_ASAP_CLKIN_P	4	AG22	IO_L0P_GC_D15_4
FPGA_DSP_CLKIN_P	4	AH12	IO_L1P_GC_D13_4
FPGA_SDRAM_CLK_N	4	AH13	IO_L3N_GC_D8_4
FPGA_SDRAM_CLK_P	4	AH14	IO_L3P_GC_D9_4
FPGA_DEBUG_LEDS[3]	4	AH15	IO_L5P_GC_4
FPGA_TRIG_IN_P	4	AH17	IO_L7P_GC_VRN_4
FPGA_AUX_IN_P	4	AH18	IO_L9P_CC_GC_4
FPGA_SRAM_CLK_N	4	AH19	IO_L2N_GC_D10_4
FPGA_SRAM_CLK_P	4	AH20	IO_L2P_GC_D11_4
FPGA_ASAP_CLKIN_N	4	AH22	IO_L0N_GC_D14_4
Bank 5: 40 Pins			
Bank Voltage: +3.3V			
P3V3D_V5	5	B19	VCCO_5
P3V3D_V5	5	C16	VCCO_5
P3V3D_V5	5	F17	VCCO_5
NOPAD			
Bank 6: 40 Pins			
Bank Voltage: +2.5V			
P3V3D_V5	6	AJ18	VCCO_6
P3V3D_V5	6	AK15	VCCO_6
P3V3D_V5	6	AN16	VCCO_6
			Continued on Next Page...

Virtex-5 SX50T (XC5VSX50T-3FFG1136C) FPGA Pin Out			
Signal Name	**Bank**	**Pin**	**Description**
NOPAD			
Bank 11: 40 Pins			
Bank Voltage: +1.8V			
P1V8D_V5	11	R30	VCCO_11
P1V8D_V5	11	T27	VCCO_11
P1V8D_V5	11	V31	VCCO_11
FPGA_DDR2_SDRAM_DQ[55]	11	A33	IO_L0N_11
FPGA_DDR2_SDRAM_DQ[50]	11	B32	IO_L0P_11
FPGA_DDR2_SDRAM_DQS[6]	11	B33	IO_L1P_11
FPGA_DDR2_SDRAM_DQ[54]	11	C32	IO_L2P_11
FPGA_DDR2_SDRAM_DQSN_NC[6]	11	C33	IO_L1N_11
FPGA_DDR2_SDRAM_DQ[51]	11	C34	IO_L3P_11
FPGA_DDR2_SDRAM_DQ[49]	11	D32	IO_L2N_11
FPGA_DDR2_SDRAM_DM[6]	11	D34	IO_L3N_11
FPGA_DDR2_SDRAM_DQ[58]	11	E32	IO_L6P_11
FPGA_DDR2_SDRAM_DQ[59]	11	E33	IO_L6N_11
FPGA_DDR2_SDRAM_DQ[63]	11	E34	IO_L5N_11
FPGA_DDR2_SDRAM_DM[7]	11	F33	IO_L5P_11
FPGA_DDR2_SDRAM_DQ[62]	11	F34	IO_L7N_11
FPGA_DDR2_SDRAM_DQ[53]	11	G32	IO_L4P_11
FPGA_DDR2_SDRAM_DQ[57]	11	G33	IO_L7P_11
P0V9D_MEM_VREF	11	H32	IO_L4N_VREF_11
FPGA_DDR2_SDRAM_DQ[52]	11	H33	IO_L8N_CC_11
FPGA_DDR2_SDRAM_DQS[7]	11	H34	IO_L9P_CC_11
FPGA_DDR2_SDRAM_DQ[48]	11	J32	IO_L8P_CC_11
FPGA_DDR2_SDRAM_DQSN_NC[7]	11	J34	IO_L9N_CC_11
FPGA_DDR2_SDRAM_A[6]	11	K32	IO_L11N_CC_SM14N_11
FPGA_DDR2_SDRAM_A[2]	11	K33	IO_L11P_CC_SM14P_11
FPGA_DDR2_SDRAM_A[1]	11	K34	IO_L10N_CC_SM15N_11
FPGA_DDR2_SDRAM_DQ[61]	11	L33	IO_L13P_11
FPGA_DDR2_SDRAM_A[4]	11	L34	IO_L10P_CC_SM15P_11
FPGA_DDR2_SDRAM_DQ[60]	11	M32	IO_L13N_11
FPGA_BANK11_VRP	11	M33	IO_L12N_VRP_11
FPGA_DDR2_SDRAM_A[7]	11	N32	IO_L15N_SM13N_11
FPGA_BANK11_VRN	11	N33	IO_L12P_VRN_11
P0V9D_MEM_VREF	11	N34	IO_L14N_VREF_11
FPGA_DDR2_SDRAM_A[11]	11	P32	IO_L15P_SM13P_11
FPGA_DDR2_SDRAM_DQ[56]	11	P34	IO_L14P_11
FPGA_DDR2_SDRAM_A[9]	11	R32	IO_L17N_SM11N_11
FPGA_DDR2_SDRAM_A[3]	11	R33	IO_L17P_SM11P_11
FPGA_DDR2_SDRAM_A[0]	11	R34	IO_L16N_SM12N_11
FPGA_DDR2_SDRAM_A[8]	11	T33	IO_L16P_SM12P_11
FPGA_DDR2_SDRAM_A[5]	11	T34	IO_L18N_SM10N_11
FPGA_DDR2_SDRAM_BA[1]	11	U31	IO_L19N_SM9N_11
FPGA_DDR2_SDRAM_BA[2]	11	U32	IO_L19P_SM9P_11
FPGA_DDR2_SDRAM_A[12]	11	U33	IO_L18P_SM10P_11
Bank 12: 40 Pins			
Bank Voltage: +2.5V			
P2V5D_V5	12	M9	VCCO_12
P2V5D_V5	12	N6	VCCO_12
			Continued on Next Page...

Virtex-5 SX50T (XC5VSX50T-3FFG1136C) FPGA Pin Out			
Signal Name	**Bank**	**Pin**	**Description**
P2V5D_V5	12	T7	VCCO_12
FPGA_ASAP1_DATA_OUT[1]	12	E6	IO_L19P_12
FPGA_ASAP1_DATA_OUT[0]	12	E7	IO_L19N_12
FPGA_ASAP1_DATA_OUT[9]	12	F5	IO_L15P_12
FPGA_ASAP1_DATA_OUT[8]	12	F6	IO_L15N_12
FPGA_ASAP1_DATA_OUT[12]	12	G5	IO_L13N_12
FPGA_ASAP1_DATA_OUT[5]	12	G6	IO_L17P_12
FPGA_ASAP1_DATA_OUT[4]	12	G7	IO_L17N_12
FPGA_ASAP1_DATA_OUT[13]	12	H5	IO_L13P_12
FPGA_ASAP1_DATA_OUT[15]	12	H7	IO_L11P_CC_12
FPGA_ASAP1_REQ_IN	12	J5	IO_L8N_CC_12
FPGA_ASAP1_CLK_IN	12	J6	IO_L8P_CC_12
FPGA_ASAP1_DATA_OUT[14]	12	J7	IO_L11N_CC_12
FPGA_ASAP1_DATA_IN[2]	12	K6	IO_L6N_12
FPGA_ASAP1_DATA_IN[3]	12	K7	IO_L6P_12
FPGA_ASAP1_DATA_IN[7]	12	L4	IO_L4P_12
FPGA_ASAP1_DATA_IN[6]	12	L5	IO_L4N_VREF_12
FPGA_ASAP1_DATA_IN[10]	12	L6	IO_L2N_12
FPGA_ASAP1_DATA_IN[14]	12	M5	IO_L0N_12
FPGA_ASAP1_DATA_IN[15]	12	M6	IO_L0P_12
FPGA_ASAP1_DATA_IN[11]	12	M7	IO_L2P_12
FPGA_ASAP1_DATA_IN[9]	12	N5	IO_L3P_12
FPGA_ASAP1_DATA_IN[12]	12	N7	IO_L1N_12
FPGA_ASAP1_DATA_IN[13]	12	N8	IO_L1P_12
FPGA_ASAP1_DATA_IN[8]	12	P5	IO_L3N_12
FPGA_ASAP1_DATA_IN[4]	12	P6	IO_L5N_12
FPGA_ASAP1_DATA_IN[5]	12	P7	IO_L5P_12
FPGA_BANK12_VRP	12	P9	IO_L12N_VRP_12
FPGA_ASAP1_DATA_OUT[10]	12	P10	IO_L14N_VREF_12
FPGA_ASAP1_DATA_IN[1]	12	R6	IO_L7P_12
FPGA_ASAP1_VLD_IN	12	R7	IO_L9P_CC_12
FPGA_ASAP1_REQ_OUT	12	R8	IO_L9N_CC_12
FPGA_BANK12_VRN	12	R9	IO_L12P_VRN_12
FPGA_ASAP1_DATA_OUT[11]	12	R11	IO_L14P_12
FPGA_ASAP1_DATA_IN[0]	12	T6	IO_L7N_12
FPGA_ASAP1_CLK_OUT	12	T8	IO_L10P_CC_12
FPGA_ASAP1_DATA_OUT[3]	12	T9	IO_L18P_12
FPGA_ASAP1_DATA_OUT[7]	12	T10	IO_L16P_12
FPGA_ASAP1_DATA_OUT[6]	12	T11	IO_L16N_12
FPGA_ASAP1_VLD_OUT	12	U7	IO_L10N_CC_12
FPGA_ASAP1_DATA_OUT[2]	12	U10	IO_L18N_12
Bank 13: 40 Pins			
Bank Voltage: +1.8V			
P1V8D_V5	13	AA32	VCCO_13
P1V8D_V5	13	AB29	VCCO_13
P1V8D_V5	13	W28	VCCO_13
FPGA_QDRII_SRAM_RDATA[12]	13	AA33	IO_L2N_SM6N_13
FPGA_QDRII_SRAM_RDATA[4]	13	AA34	IO_L3P_SM5P_13
FPGA_QDRII_SRAM_RDATA[13]	13	AB32	IO_L6N_SM3N_13
FPGA_QDRII_SRAM_RDATA[5]	13	AB33	IO_L7N_SM2N_13
			Continued on Next Page...

Virtex-5 SX50T (XC5VSX50T-3FFG1136C) FPGA Pin Out			
Signal Name	**Bank**	**Pin**	**Description**
FPGA_QDRII_SRAM_RDATA[7]	13	AC32	IO_L6P_SM3P_13
FPGA_QDRII_SRAM_RDATA[15]	13	AC33	IO_L7P_SM2P_13
FPGA_QDRII_SRAM_RDATA[14]	13	AC34	IO_L5P_SM4P_13
FPGA_QDRII_SRAM_RDATA[26]	13	AD32	IO_L11P_CC_13
FPGA_QDRII_SRAM_RDATA[6]	13	AD34	IO_L5N_SM4N_13
FPGA_QDRII_SRAM_RDATA[35]	13	AE32	IO_L11N_CC_13
FPGA_QDRII_SRAM_RDATA[8]	13	AE33	IO_L8N_CC_SM1N_13
FPGA_QDRII_SRAM_RDATA[16]	13	AE34	IO_L9N_CC_SM0N_13
FPGA_QDRII_SRAM_CQ_CLK_P	13	AF33	IO_L8P_CC_SM1P_13
FPGA_QDRII_SRAM_CQ_CLK_N	13	AF34	IO_L9P_CC_SM0P_13
FPGA_QDRII_SRAM_RDATA[25]	13	AG32	IO_L14P_13
FPGA_QDRII_SRAM_RDATA[34]	13	AG33	IO_L12P_VRN_13
P0V9D_MEM_VREF	13	AH32	IO_L14N_VREF_13
FPGA_QDRII_SRAM_RDATA[24]	13	AH33	IO_L12N_VRP_13
FPGA_QDRII_SRAM_RDATA[17]	13	AH34	IO_L10P_CC_13
FPGA_QDRII_SRAM_RDATA[33]	13	AJ32	IO_L15P_13
FPGA_QDRII_SRAM_RDATA[18]	13	AJ34	IO_L10N_CC_13
FPGA_QDRII_SRAM_RDATA[23]	13	AK32	IO_L15N_13
FPGA_QDRII_SRAM_RDATA[32]	13	AK33	IO_L13N_13
FPGA_QDRII_SRAM_RDATA[27]	13	AK34	IO_L13P_13
FPGA_QDRII_SRAM_RDATA[31]	13	AL33	IO_L16N_13
FPGA_QDRII_SRAM_RDATA[28]	13	AL34	IO_L16P_13
FPGA_QDRII_SRAM_RDATA[22]	13	AM32	IO_L17N_13
FPGA_QDRII_SRAM_RDATA[20]	13	AM33	IO_L17P_13
FPGA_QDRII_SRAM_RDATA[21]	13	AN32	IO_L19P_13
FPGA_QDRII_SRAM_RDATA[29]	13	AN33	IO_L18N_13
FPGA_QDRII_SRAM_RDATA[19]	13	AN34	IO_L18P_13
FPGA_QDRII_SRAM_RDATA[30]	13	AP32	IO_L19N_13
FPGA_QDRII_SRAM_RDATA[9]	13	V32	IO_L0P_SM8P_13
FPGA_QDRII_SRAM_RDATA[0]	13	V33	IO_L0N_SM8N_13
FPGA_QDRII_SRAM_RDATA[10]	13	V34	IO_L1N_SM7N_13
P0V9D_MEM_VREF	13	W32	IO_L4N_VREF_13
FPGA_QDRII_SRAM_RDATA[11]	13	W34	IO_L1P_SM7P_13
FPGA_QDRII_SRAM_RDATA[1]	13	Y32	IO_L4P_13
FPGA_QDRII_SRAM_RDATA[2]	13	Y33	IO_L2P_SM6P_13
FPGA_QDRII_SRAM_RDATA[3]	13	Y34	IO_L3N_SM5N_13
Bank 15: 40 Pins			
Bank Voltage: +1.8V			
P1V8D_V5	15	L32	VCCO_15
P1V8D_V5	15	M29	VCCO_15
P1V8D_V5	15	P33	VCCO_15
FPGA_DDR2_SDRAM_DQ[27]	15	E29	IO_L0P_15
FPGA_DDR2_SDRAM_DQ[31]	15	E31	IO_L3N_15
FPGA_DDR2_SDRAM_DQ[24]	15	F29	IO_L0N_15
FPGA_DDR2_SDRAM_DM[3]	15	F30	IO_L1N_15
FPGA_DDR2_SDRAM_DQ[25]	15	F31	IO_L3P_15
FPGA_DDR2_SDRAM_DQ[26]	15	G30	IO_L1P_15
FPGA_DDR2_SDRAM_DQSN_NC[4]	15	G31	IO_L5N_15
FPGA_DDR2_SDRAM_DQ[30]	15	H29	IO_L2P_15
FPGA_DDR2_SDRAM_DQS[4]	15	H30	IO_L5P_15
			Continued on Next Page...

Virtex-5 SX50T (XC5VSX50T-3FFG1136C) FPGA Pin Out			
Signal Name	**Bank**	**Pin**	**Description**
FPGA_DDR2_SDRAM_DQ[29]	15	J29	IO_L2N_15
FPGA_DDR2_SDRAM_DM[4]	15	J30	IO_L6P_15
FPGA_DDR2_SDRAM_DQ[36]	15	J31	IO_L6N_15
P0V9D_MEM_VREF	15	K29	IO_L4N_VREF_15
FPGA_DDR2_SDRAM_DQ[33]	15	K31	IO_L9P_CC_15
FPGA_DDR2_SDRAM_DQ[28]	15	L29	IO_L4P_15
FPGA_DDR2_SDRAM_DQ[34]	15	L30	IO_L7P_15
FPGA_DDR2_SDRAM_DQ[37]	15	L31	IO_L9N_CC_15
FPGA_DDR2_SDRAM_DQ[38]	15	M30	IO_L7N_15
FPGA_DDR2_SDRAM_CK_P[1]	15	M31	IO_L11P_CC_15
FPGA_DDR2_SDRAM_DQS[3]	15	N29	IO_L8P_CC_15
FPGA_DDR2_SDRAM_CK_N[1]	15	N30	IO_L11N_CC_15
FPGA_DDR2_SDRAM_DQSN_NC[3]	15	P29	IO_L8N_CC_15
FPGA_DDR2_SDRAM_DQ[44]	15	P30	IO_L10N_CC_15
FPGA_DDR2_SDRAM_DQ[45]	15	P31	IO_L10P_CC_15
FPGA_DDR2_SDRAM_DQ[46]	15	R26	IO_L17P_15
FPGA_DDR2_SDRAM_DQ[47]	15	R27	IO_L17N_15
FPGA_BANK15_VRN	15	R28	IO_L12P_VRN_15
FPGA_BANK15_VRP	15	R29	IO_L12N_VRP_15
FPGA_DDR2_SDRAM_DQ[32]	15	R31	IO_L13N_15
FPGA_DDR2_SDRAM_A[10]	15	T25	IO_L19N_15
FPGA_DDR2_SDRAM_DQ[43]	15	T26	IO_L18N_15
FPGA_DDR2_SDRAM_DM[5]	15	T28	IO_L15P_15
FPGA_DDR2_SDRAM_DQ[41]	15	T29	IO_L15N_15
P0V9D_MEM_VREF	15	T30	IO_L14N_VREF_15
FPGA_DDR2_SDRAM_DQ[39]	15	T31	IO_L13P_15
FPGA_DDR2_SDRAM_DQ[40]	15	U25	IO_L19P_15
FPGA_DDR2_SDRAM_DQ[42]	15	U26	IO_L18P_15
FPGA_DDR2_SDRAM_DQS[5]	15	U27	IO_L16P_15
FPGA_DDR2_SDRAM_DQSN_NC[5]	15	U28	IO_L16N_15
FPGA_DDR2_SDRAM_DQ[35]	15	U30	IO_L14P_15
Bank 17: 40 Pins			
Bank Voltage: +1.8V			
P1V8D_V5	17	AD33	VCCO_17
P1V8D_V5	17	AE30	VCCO_17
P1V8D_V5	17	AH31	VCCO_17
FPGA_QDRII_SRAM_WDATA[26]	17	AA29	IO_L11P_CC_17
FPGA_QDRII_SRAM_WDATA[18]	17	AA30	IO_L11N_CC_17
FPGA_QDRII_SRAM_WDATA[8]	17	AA31	IO_L9N_CC_17
FPGA_QDRII_SRAM_BWN[1]	17	AB30	IO_L10P_CC_17
FPGA_QDRII_SRAM_WDATA[16]	17	AB31	IO_L9P_CC_17
FPGA_QDRII_SRAM_WDATA[25]	17	AC29	IO_L13N_17
FPGA_QDRII_SRAM_WDATA[34]	17	AC30	IO_L10N_CC_17
FPGA_QDRII_SRAM_BWN[2]	17	AD29	IO_L15N_17
FPGA_QDRII_SRAM_WDATA[33]	17	AD30	IO_L13P_17
FPGA_QDRII_SRAM_WDATA[24]	17	AD31	IO_L12P_VRN_17
FPGA_QDRII_SRAM_WDATA[32]	17	AE29	IO_L15P_17
FPGA_QDRII_SRAM_WDATA[23]	17	AE31	IO_L12N_VRP_17
FPGA_QDRII_SRAM_WDATA[31]	17	AF29	IO_L17P_17
FPGA_QDRII_SRAM_WDATA[30]	17	AF30	IO_L17N_17
			Continued on Next Page...

Virtex-5 SX50T (XC5VSX50T-3FFG1136C) FPGA Pin Out			
Signal Name	**Bank**	**Pin**	**Description**
FPGA_QDRII_SRAM_WDATA[19]	17	AF31	IO_L14P_17
FPGA_QDRII_SRAM_WDATA[27]	17	AG30	IO_L19N_17
P0V9D_MEM_VREF	17	AG31	IO_L14N_VREF_17
FPGA_QDRII_SRAM_WDATA[22]	17	AH29	IO_L19P_17
FPGA_QDRII_SRAM_WDATA[21]	17	AH30	IO_L18N_17
FPGA_QDRII_SRAM_WDATA[29]	17	AJ30	IO_L18P_17
FPGA_QDRII_SRAM_WDATA[20]	17	AJ31	IO_L16P_17
FPGA_QDRII_SRAM_WDATA[28]	17	AK31	IO_L16N_17
FPGA_QDRII_SRAM_WDATA[13]	17	V24	IO_L0N_17
FPGA_QDRII_SRAM_WDATA[12]	17	V25	IO_L2P_17
FPGA_QDRII_SRAM_WDATA[9]	17	V27	IO_L5N_17
FPGA_QDRII_SRAM_BWN[0]	17	V28	IO_L5P_17
FPGA_QDRII_SRAM_WDATA[0]	17	V29	IO_L7N_17
FPGA_QDRII_SRAM_WDATA[14]	17	V30	IO_L4P_17
FPGA_QDRII_SRAM_WDATA[5]	17	W24	IO_L0P_17
FPGA_QDRII_SRAM_WDATA[4]	17	W25	IO_L2N_17
FPGA_QDRII_SRAM_WDATA[11]	17	W26	IO_L1N_17
FPGA_QDRII_SRAM_WDATA[10]	17	W27	IO_L3N_17
FPGA_QDRII_SRAM_WDATA[1]	17	W29	IO_L7P_17
P0V9D_MEM_VREF	17	W30	IO_L4N_VREF_17
FPGA_QDRII_SRAM_WDATA[6]	17	W31	IO_L6P_17
FPGA_QDRII_SRAM_WDATA[3]	17	Y26	IO_L1P_17
FPGA_QDRII_SRAM_WDATA[2]	17	Y27	IO_L3P_17
FPGA_QDRII_SRAM_WDATA[7]	17	Y28	IO_L8P_CC_17
FPGA_QDRII_SRAM_WDATA[17]	17	Y29	IO_L8N_CC_17
FPGA_QDRII_SRAM_WDATA[15]	17	Y31	IO_L6N_17
Bank 18: 40 Pins			
Bank Voltage: +2.5V			
P2V5D_V5	18	AB9	VCCO_18
P2V5D_V5	18	AC6	VCCO_18
P2V5D_V5	18	W8	VCCO_18
FPGA_DAC_DATA_P[13]	18	AA5	IO_L2P_18
FPGA_DAC_DATA_P[9]	18	AA6	IO_L6P_18
FPGA_DAC_DATA_N[13]	18	AB5	IO_L2N_18
FPGA_DAC_DATA_P[14]	18	AB6	IO_L1P_18
FPGA_DAC_DATA_N[14]	18	AB7	IO_L1N_18
FPGA_DAC_DATA_P[15]	18	AC4	IO_L0P_18
FPGA_DAC_DATA_N[15]	18	AC5	IO_L0N_18
FPGA_DAC_DATA_P[12]	18	AC7	IO_L3P_18
FPGA_DAC_DATA_P[10]	18	AD4	IO_L5P_18
FPGA_DAC_DATA_N[10]	18	AD5	IO_L5N_18
FPGA_DAC_DATA_P[8]	18	AD6	IO_L7P_18
FPGA_DAC_DATA_N[12]	18	AD7	IO_L3N_18
FPGA_DAC_DATA_N[8]	18	AE6	IO_L7N_18
FPGA_DAC_DATA_P[6]	18	AE7	IO_L9P_CC_18
FPGA_DAC_DATA_N[5]	18	AF5	IO_L10N_CC_18
FPGA_DAC_DATA_N[6]	18	AF6	IO_L9N_CC_18
FPGA_DAC_DATA_P[5]	18	AG5	IO_L10P_CC_18
FPGA_DAC_DATA_N[3]	18	AG6	IO_L12N_VRP_18
FPGA_DAC_DATA_N[1]	18	AG7	IO_L14N_VREF_18
			Continued on Next Page...

Virtex-5 SX50T (XC5VSX50T-3FFG1136C) FPGA Pin Out			
Signal Name	**Bank**	**Pin**	**Description**
FPGA_DAC_DATA_P[3]	18	AH5	IO_L12P_VRN_18
FPGA_DAC_DATA_P[1]	18	AH7	IO_L14P_18
FPGA_DAC_CLK_IN_N	18	AJ6	IO_L16N_18
FPGA_DAC_CLK_IN_P	18	AJ7	IO_L16P_18
No Connect	18	AK6	IO_L18N_18
No Connect	18	AK7	IO_L18P_18
FPGA_DAC_SYNC_N	18	U8	IO_L17N_18
FPGA_DAC_DATA_N[4]	18	V7	IO_L11N_CC_18
FPGA_DAC_SYNC_P	18	V8	IO_L17P_18
No Connect	18	V9	IO_L19N_18
No Connect	18	V10	IO_L19P_18
FPGA_DAC_DATA_P[7]	18	W6	IO_L8P_CC_18
FPGA_DAC_DATA_P[4]	18	W7	IO_L11P_CC_18
FPGA_DAC_DATA_N[0]	18	W9	IO_L15N_18
FPGA_DAC_DATA_P[0]	18	W10	IO_L15P_18
FPGA_DAC_DATA_N[2]	18	W11	IO_L13N_18
FPGA_DAC_DATA_N[7]	18	Y6	IO_L8N_CC_18
FPGA_DAC_DATA_N[9]	18	Y7	IO_L6N_18
FPGA_DAC_DATA_P[11]	18	Y8	IO_L4P_18
FPGA_DAC_DATA_N[11]	18	Y9	IO_L4N_VREF_18
FPGA_DAC_DATA_P[2]	18	Y11	IO_L13P_18
Bank 19: 40 Pins			
Bank Voltage: +1.8V			
P1V8D_V5	19	E30	VCCO_19
P1V8D_V5	19	H31	VCCO_19
P1V8D_V5	19	J28	VCCO_19
FPGA_DDR2_SDRAM_CK_P[0]	19	E26	IO_L11P_CC_19
FPGA_DDR2_SDRAM_CK_N[0]	19	E27	IO_L11N_CC_19
FPGA_DDR2_SDRAM_DQS[2]	19	E28	IO_L10P_CC_19
FPGA_DDR2_SDRAM_DQ[8]	19	F25	IO_L7P_19
FPGA_DDR2_SDRAM_DM[1]	19	F26	IO_L7N_19
FPGA_DDR2_SDRAM_DQSN_NC[2]	19	F28	IO_L10N_CC_19
FPGA_DDR2_SDRAM_DQ[14]	19	G25	IO_L5P_19
FPGA_DDR2_SDRAM_DQ[10]	19	G26	IO_L5N_19
FPGA_DDR2_SDRAM_DQS[0]	19	G27	IO_L8P_CC_19
FPGA_DDR2_SDRAM_DQSN_NC[1]	19	G28	IO_L9N_CC_19
FPGA_DDR2_SDRAM_DQ[11]	19	H24	IO_L6N_19
FPGA_DDR2_SDRAM_DQ[15]	19	H25	IO_L6P_19
FPGA_DDR2_SDRAM_DQSN_NC[0]	19	H27	IO_L8N_CC_19
FPGA_DDR2_SDRAM_DQS[1]	19	H28	IO_L9P_CC_19
FPGA_DDR2_SDRAM_DM[0]	19	J24	IO_L2P_19
FPGA_DDR2_SDRAM_DQ[0]	19	J25	IO_L2N_19
P0V9D_MEM_VREF	19	J26	IO_L4N_VREF_19
FPGA_DDR2_SDRAM_DQ[4]	19	J27	IO_L4P_19
FPGA_DDR2_SDRAM_DQ[1]	19	K24	IO_L0P_19
P0V9D_MEM_VREF	19	K26	IO_L14N_VREF_19
FPGA_DDR2_SDRAM_DQ[13]	19	K27	IO_L14P_19
FPGA_DDR2_SDRAM_DQ[12]	19	K28	IO_L13P_19
FPGA_DDR2_SDRAM_DQ[7]	19	L24	IO_L0N_19
FPGA_DDR2_SDRAM_DQ[6]	19	L25	IO_L1P_19
			Continued on Next Page...

Virtex-5 SX50T (XC5VSX50T-3FFG1136C) FPGA Pin Out			
Signal Name	**Bank**	**Pin**	**Description**
FPGA_DDR2_SDRAM_DQ[2]	19	L26	IO_L1N_19
FPGA_DDR2_SDRAM_DQ[9]	19	L28	IO_L13N_19
FPGA_DDR2_SDRAM_DQ[3]	19	M25	IO_L3P_19
FPGA_DDR2_SDRAM_DQ[5]	19	M26	IO_L3N_19
FPGA_BANK19_VRP	19	M27	IO_L12N_VRP_19
FPGA_DDR2_SDRAM_DM[2]	19	M28	IO_L15P_19
FPGA_DDR2_SDRAM_DQ[21]	19	N24	IO_L17P_19
FPGA_DDR2_SDRAM_DQ[17]	19	N25	IO_L18N_19
FPGA_BANK19_VRN	19	N27	IO_L12P_VRN_19
FPGA_DDR2_SDRAM_DQ[22]	19	N28	IO_L15N_19
FPGA_DDR2_SDRAM_DQ[18]	19	P24	IO_L17N_19
FPGA_DDR2_SDRAM_DQ[20]	19	P25	IO_L18P_19
FPGA_DDR2_SDRAM_DQ[19]	19	P26	IO_L16P_19
FPGA_DDR2_SDRAM_DQ[23]	19	P27	IO_L16N_19
FPGA_DDR2_SDRAM_DQ[16]	19	R24	IO_L19P_19
FPGA_DDR2_SDRAM_A[13]	19	T24	IO_L19N_19
Bank 20: 40 Pins			
Bank Voltage: +2.5V			
P2V5D_V5	20	E10	VCCO_20
P2V5D_V5	20	H11	VCCO_20
P2V5D_V5	20	J8	VCCO_20
FPGA_ASAP2_CLK_IN	20	A13	IO_L8P_CC_20
FPGA_ASAP2_REQ_IN	20	B12	IO_L8N_CC_20
FPGA_ASAP2_DATA_OUT[15]	20	B13	IO_L11P_CC_20
FPGA_ASAP2_DATA_IN[2]	20	C12	IO_L6N_20
FPGA_ASAP2_DATA_OUT[14]	20	C13	IO_L11N_CC_20
FPGA_ASAP2_DATA_IN[6]	20	D10	IO_L4N_VREF_20
FPGA_ASAP2_DATA_IN[7]	20	D11	IO_L4P_20
FPGA_ASAP2_DATA_IN[3]	20	D12	IO_L6P_20
FPGA_ASAP2_DATA_IN[14]	20	E8	IO_L0N_20
FPGA_ASAP2_DATA_IN[15]	20	E9	IO_L0P_20
FPGA_ASAP2_DATA_OUT[8]	20	E11	IO_L15N_20
FPGA_ASAP2_DATA_OUT[5]	20	E12	IO_L17P_20
FPGA_ASAP2_DATA_OUT[4]	20	E13	IO_L17N_20
FPGA_ASAP2_DATA_IN[12]	20	F8	IO_L1N_20
FPGA_ASAP2_DATA_IN[13]	20	F9	IO_L1P_20
FPGA_ASAP2_DATA_IN[11]	20	F10	IO_L2P_20
FPGA_ASAP2_DATA_OUT[9]	20	F11	IO_L15P_20
FPGA_ASAP2_DATA_OUT[1]	20	F13	IO_L19P_20
FPGA_ASAP2_DATA_IN[9]	20	G8	IO_L3P_20
FPGA_ASAP2_DATA_IN[10]	20	G10	IO_L2N_20
FPGA_ASAP2_DATA_OUT[13]	20	G11	IO_L13P_20
FPGA_ASAP2_DATA_OUT[12]	20	G12	IO_L13N_20
FPGA_ASAP2_DATA_OUT[0]	20	G13	IO_L19N_20
FPGA_ASAP2_DATA_IN[8]	20	H8	IO_L3N_20
FPGA_ASAP2_DATA_IN[0]	20	H9	IO_L7N_20
FPGA_ASAP2_DATA_IN[1]	20	H10	IO_L7P_20
FPGA_ASAP2_REQ_OUT	20	J9	IO_L9N_CC_20
FPGA_ASAP2_VLD_IN	20	J10	IO_L9P_CC_20
FPGA_ASAP2_DATA_IN[4]	20	J11	IO_L5N_20
			Continued on Next Page...

Virtex-5 SX50T (XC5VSX50T-3FFG1136C) FPGA Pin Out			
Signal Name	**Bank**	**Pin**	**Description**
FPGA_ASAP2_CLK_OUT	20	K8	IO_L10P_CC_20
FPGA_ASAP2_VLD_OUT	20	K9	IO_L10N_CC_20
FPGA_ASAP2_DATA_IN[5]	20	K11	IO_L5P_20
FPGA_ASAP2_DATA_OUT[10]	20	L8	IO_L14N_VREF_20
FPGA_ASAP2_DATA_OUT[6]	20	L9	IO_L16N_20
FPGA_BANK20_VRN	20	L10	IO_L12P_VRN_20
FPGA_BANK20_VRP	20	L11	IO_L12N_VRP_20
FPGA_ASAP2_DATA_OUT[11]	20	M8	IO_L14P_20
FPGA_ASAP2_DATA_OUT[7]	20	M10	IO_L16P_20
FPGA_ASAP2_DATA_OUT[2]	20	N9	IO_L18N_20
FPGA_ASAP2_DATA_OUT[3]	20	N10	IO_L18P_20
Bank 21: 40 Pins			
Bank Voltage: +1.8V			
P1V8D_V5	21	AJ28	VCCO_21
P1V8D_V5	21	AL32	VCCO_21
P1V8D_V5	21	AM29	VCCO_21
FPGA_QDRII_SRAM_BWN[3]	21	AA24	IO_L2N_21
FPGA_QDRII_SRAM_K_CLK_P	21	AA25	IO_L0P_21
FPGA_QDRII_SRAM_K_CLK_N	21	AA26	IO_L0N_21
FPGA_QDRII_SRAM_ADDR[4]	21	AA28	IO_L5N_21
FPGA_QDRII_SRAM_ADDR[17]	21	AB25	IO_L3P_21
FPGA_QDRII_SRAM_ADDR[1]	21	AB26	IO_L3N_21
FPGA_QDRII_SRAM_DUMMY_IN	21	AB27	IO_L1P_21
FPGA_QDRII_SRAM_ADDR[2]	21	AB28	IO_L5P_21
FPGA_DDR2_SDRAM_SN[0]	21	AC24	IO_L17N_21
FPGA_DDR2_SDRAM_SN[1]	21	AC25	IO_L17P_21
FPGA_QDRII_SRAM_DLL_OFFN	21	AC27	IO_L1N_21
FPGA_QDRII_SRAM_ADDR[0]	21	AC28	IO_L4P_21
FPGA_DDR2_SDRAM_CKE[1]	21	AD24	IO_L19P_21
FPGA_DDR2_SDRAM_ODT[0]	21	AD25	IO_L18N_21
FPGA_DDR2_SDRAM_ODT[1]	21	AD26	IO_L18P_21
P0V9D_MEM_VREF	21	AD27	IO_L4N_VREF_21
FPGA_DDR2_SDRAM_CKE[0]	21	AE24	IO_L19N_21
FPGA_DDR2_SDRAM_WEN	21	AE26	IO_L16N_21
FPGA_DDR2_SDRAM_CASN	21	AE27	IO_L16P_21
FPGA_QDRII_SRAM_ADDR[3]	21	AE28	IO_L7P_21
FPGA_QDRII_SRAM_ADDR[11]	21	AF24	IO_L13P_21
FPGA_DDR2_SDRAM_BA[0]	21	AF25	IO_L15P_21
FPGA_DDR2_SDRAM_RASN	21	AF26	IO_L15N_21
FPGA_QDRII_SRAM_ADDR[16]	21	AF28	IO_L7N_21
FPGA_QDRII_SRAM_WRN	21	AG25	IO_L13N_21
P0V9D_MEM_VREF	21	AG26	IO_L14N_VREF_21
FPGA_QDRII_SRAM_RDN	21	AG27	IO_L14P_21
FPGA_QDRII_SRAM_ADDR[12]	21	AG28	IO_L6P_21
FPGA_BANK21_VRP	21	AH25	IO_L12N_VRP_21
FPGA_QDRII_SRAM_ADDR[10]	21	AH27	IO_L11P_CC_21
FPGA_QDRII_SRAM_ADDR[8]	21	AH28	IO_L6N_21
FPGA_BANK21_VRN	21	AJ25	IO_L12P_VRN_21
FPGA_QDRII_SRAM_ADDR[15]	21	AJ26	IO_L11N_CC_21
FPGA_QDRII_SRAM_ADDR[7]	21	AJ27	IO_L8N_CC_21
			Continued on Next Page...

Virtex-5 SX50T (XC5VSX50T-3FFG1136C) FPGA Pin Out			
Signal Name	**Bank**	**Pin**	**Description**
FPGA_QDRII_SRAM_ADDR[13]	21	AJ29	IO_L9N_CC_21
FPGA_QDRII_SRAM_ADDR[6]	21	AK26	IO_L8P_CC_21
FPGA_QDRII_SRAM_ADDR[9]	21	AK27	IO_L10N_CC_21
FPGA_QDRII_SRAM_ADDR[14]	21	AK28	IO_L10P_CC_21
FPGA_QDRII_SRAM_ADDR[5]	21	AK29	IO_L9P_CC_21
FPGA_QDRII_SRAM_WDATA[35]	21	Y24	IO_L2P_21
Bank 22: 40 Pins			
Bank Voltage: +2.5V			
P2V5D_V5	22	AF7	VCCO_22
P2V5D_V5	22	AH11	VCCO_22
P2V5D_V5	22	AJ8	VCCO_22
FPGA_ADC_DATA_P[12]	22	AA8	IO_L3P_22
FPGA_ADC_DATA_N[12]	22	AA9	IO_L3N_22
FPGA_ADC_DATA_N[14]	22	AA10	IO_L1N_22
FPGA_ADC_DATA_N[10]	22	AB8	IO_L5N_22
FPGA_ADC_DATA_P[14]	22	AB10	IO_L1P_22
FPGA_ADC_DATA_P[10]	22	AC8	IO_L5P_22
FPGA_ADC_DATA_N[8]	22	AC9	IO_L7N_22
FPGA_ADC_DATA_P[8]	22	AC10	IO_L7P_22
FPGA_ADC_DATA_N[7]	22	AD9	IO_L9N_CC_22
FPGA_ADC_DATA_P[6]	22	AD10	IO_L10P_CC_22
FPGA_ADC_DATA_N[6]	22	AD11	IO_L10N_CC_22
FPGA_ADC_DATA_P[7]	22	AE8	IO_L9P_CC_22
FPGA_ADC_DATA_N[4]	22	AE9	IO_L12N_VRP_22
FPGA_ADC_DATA_N[0]	22	AE11	IO_L16N_22
FPGA_ADC_DATA_P[4]	22	AF8	IO_L12P_VRN_22
FPGA_ADC_DATA_P[2]	22	AF9	IO_L14P_22
FPGA_ADC_DATA_N[2]	22	AF10	IO_L14N_VREF_22
FPGA_ADC_DATA_P[0]	22	AF11	IO_L16P_22
No Connect	22	AG8	IO_L18P_22
No Connect	22	AG10	IO_L19P_22
No Connect	22	AG11	IO_L19N_22
No Connect	22	AH8	IO_L18N_22
FPGA_ADC_OVR_P	22	AH9	IO_L17P_22
FPGA_ADC_OVR_N	22	AH10	IO_L17N_22
FPGA_ADC_DATA_P[1]	22	AJ9	IO_L15P_22
FPGA_ADC_DATA_N[1]	22	AJ10	IO_L15N_22
FPGA_ADC_DATA_N[5]	22	AJ11	IO_L11N_CC_22
FPGA_ADC_DATA_P[3]	22	AK8	IO_L13P_22
FPGA_ADC_DATA_N[3]	22	AK9	IO_L13N_22
FPGA_ADC_DATA_P[5]	22	AK11	IO_L11P_CC_22
FPGA_ADC_DATA_RDY_N	22	AL10	IO_L8N_CC_22
FPGA_ADC_DATA_RDY_P	22	AL11	IO_L8P_CC_22
FPGA_ADC_DATA_N[9]	22	AM11	IO_L6N_22
FPGA_ADC_DATA_P[9]	22	AM12	IO_L6P_22
FPGA_ADC_DATA_N[13]	22	AM13	IO_L2N_22
FPGA_ADC_DATA_N[11]	22	AN12	IO_L4N_VREF_22
FPGA_ADC_DATA_P[13]	22	AN13	IO_L2P_22
FPGA_ADC_DATA_P[15]	22	AN14	IO_L0P_22
FPGA_ADC_DATA_P[11]	22	AP12	IO_L4P_22
			Continued on Next Page...

Virtex-5 SX50T (XC5VSX50T-3FFG1136C) FPGA Pin Out			
Signal Name	**Bank**	**Pin**	**Description**
FPGA_ADC_DATA_N[15]	22	AP14	IO_L0N_22
Bank 23: 40 Pins			
Bank Voltage: +3.3V			
P3V3D_V5	23	C26	VCCO_23
P3V3D_V5	23	F27	VCCO_23
P3V3D_V5	23	G24	VCCO_23
NOPAD			
Bank 25: 40 Pins			
Bank Voltage: +2.5V			
P2V5D_V5	25	AK25	VCCO_25
P2V5D_V5	25	AL22	VCCO_25
P2V5D_V5	25	AN26	VCCO_25
NOPAD			

6.2 Control FPGA Pinout

The Measurement board contains an Xilinx Spartan 3A XC3S1400A FPGA for controlling the measurement control circuitry. The Xilinx part number is: XC3S1400A-4FG484.

Table 6.2: Xilinx Spartan 3A XC3S1400A FPGA Pin Out

Xilinx Spartan 3A XC3S1400A FPGA Pin Out			
Signal Name	**Bank #**	**Pin #**	**Description**
Dedicated Configuration Signals			
S3A_PROG_B	NA	C4	Spartan-3A Program Signal (Active Low).
S3A_CONFIG_DONE	NA	Y19	Spartan-3A Configuration Done (Active High).
TCK	NA	A21	JTAG Configuration TCK Signal.
TDI_TO_S3A	NA	F5	JTAG Configuration TDI Signal.
TDO_TO_V5	NA	E19	JTAG Configuration TDO Signal.
TMS	NA	D4	JTAG Configuration TMS Signal.
Bank 0			
No Connect	0	D19	Unused Pin.
No Connect	0	B19	Unused Pin.
No Connect	0	A20	Unused Pin.
No Connect	0	C19	Unused Pin.
No Connect	0	B20	Unused Pin.
No Connect	0	E17	Unused Pin.
No Connect	0	A18	Unused Pin.
No Connect	0	C18	Unused Pin.
No Connect	0	D18	Unused Pin.
No Connect	0	A19	Unused Pin.
No Connect	0	D16	Unused Pin.
No Connect	0	B17	Unused Pin.
No Connect	0	C17	Unused Pin.
FPGA_TMPSENS_2C_MOSI	0	D17	Temperature Sensor 2C Master-Out-Slave-In (MOSI).
FPGA_TMPSENS_2C_CSN	0	A17	Temperature Sensor 2C Chip Select (Active Low).
FPGA_CLK10MHZ_REF_CTRL[0]	0	B2	10MHz Reference Control Bit 0.
FPGA_CLK10MHZ_REF_CTRL[2]	0	A3	10MHz Reference Control Bit 2.
FPGA_CLK10MHZ_REF_CTRL[1]	0	B3	10MHz Reference Control Bit 1.
FPGA_EXT_CLK10MHZ_LOS	0	A2	10MHz Reference Loss of Signal (Active High).
FPGA_UI_MOSI	0	B4	User Interface Board SPI Master-Out-Slave-In (MOSI).
FPGA_UI_RDY	0	A5	User Interface Board Ready (Active High).
FPGA_UI_RSTN	0	C5	User Interface Board Reset (Active Low).
FPGA_CLK10MHZ_REF_CTRL[3]	0	A4	10MHz Reference Control Bit 3.
FPGA_TMPSENS_1B_SCK	0	F7	Temperature Sensor 1B Serial Clock.
FPGA_TMPSENS_1B_MISO	0	E6	Temperature Sensor 1B Master-In-Slave-Out (MISO).
FPGA_TMPSENS_1B_CSN	0	E7	Temperature Sensor 1B Chip Select (Active Low).
FPGA_UI_SCK	0	D5	User Interface Board SPI Serial Clock.
FPGA_UI_INTN	0	B6	User Interface Board Interrupt (Active Low).
FPGA_UI_CSN	0	C6	User Interface Board SPI Chip Select (Active Low).
FPGA_LOCAL_RSTN	0	D6	Measurement Board Local Reset (Active Low).
FPGA_UI_MISO	0	A6	User Interface Board SPI Master-In-Slave-Out (MISO).
FPGA_LEDS[1]	0	C7	LED 1 (Active Low).
No Connect	0	A7	Unused Pin.
No Connect	0	A8	Unused Pin.
FPGA_S3A_BOARD_RSTN	0	D7	Measurement Board Reset (Active Low).
FPGA_PUSHBUTTON[0]	0	H9	Push-Button 0 (Active Low).

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Xilinx Spartan 3A XC3S1400A FPGA Pin Out			
Signal Name	**Bank #**	**Pin #**	**Description**
FPGA_LEDS[3]	0	B8	LED 3 (Active Low).
No Connect	0	A9	Unused Pin.
No Connect	0	H10	Unused Pin.
No Connect	0	G10	Unused Pin.
No Connect	0	F10	Unused Pin.
No Connect	0	E10	Unused Pin.
No Connect	0	D10	Unused Pin.
No Connect	0	C10	Unused Pin.
No Connect	0	A10	Unused Pin.
FPGA_INT_CLK10MHZ_REF_N	0	A11	Internal 10MHz Reference Clock (Negative Differential).
FPGA_EXT_CLK10MHZ_REF_P	0	B11	External 10MHz Reference Clock (Positive Differential).
FPGA_EXT_CLK10MHZ_REF_N	0	C11	External 10MHz Reference Clock (Negative Differential).
No Connect	0	D11	Unused Pin.
No Connect	0	E11	Unused Pin.
No Connect	0	G11	Unused Pin.
No Connect	0	G12	Unused Pin.
No Connect	0	H12	Unused Pin.
No Connect	0	H13	Unused Pin.
FPGA_LEDS[2]	0	C8	LED 2 (Active Low).
No Connect	0	B9	Unused Pin.
No Connect	0	C9	Unused Pin.
FPGA_LEDS[0]	0	D8	LED 0 (Active Low).
No Connect	0	C12	Unused Pin.
No Connect	0	E12	Unused Pin.
FPGA_INT_CLK10MHZ_REF_P	0	A12	Internal 10MHz Reference Clock (Positive Differential).
No Connect	0	F16	Unused Pin.
No Connect	0	E16	Unused Pin.
No Connect	0	G15	Unused Pin.
No Connect	0	E15	Unused Pin.
No Connect	0	F15	Unused Pin.
No Connect	0	G16	Unused Pin.
No Connect	0	G14	Unused Pin.
No Connect	0	C16	Unused Pin.
No Connect	0	C14	Unused Pin.
FPGA_LA_DATA[1]	0	E14	Logic Analyzer Data 1.
No Connect	0	H14	Unused Pin.
FPGA_LA_DATA[4]	0	D15	Logic Analyzer Data 4.
No Connect	0	C15	Unused Pin.
No Connect	0	A16	Unused Pin.
FPGA_DDR2_SDRAM_SCL	0	A15	DDR2 SDRAM SODIMM I^2C Serial Clock.
FPGA_DDR2_SDRAM_SDA	0	B15	DDR2 SDRAM SODIMM I^2C Serial Data.
FPGA_LA_CLK	0	A14	Logic Analyzer Clock.
No Connect	0	G13	Unused Pin.
FPGA_LA_DATA[0]	0	F13	Logic Analyzer Data 0.
FPGA_LA_DATA[2]	0	E13	Logic Analyzer Data 2.
FPGA_LA_DATA[3]	0	D13	Logic Analyzer Data 3.
FPGA_LA_DATA[5]	0	C13	Logic Analyzer Data 5.
No Connect	0	F12	Unused Pin.
FPGA_LA_DATA[6]	0	B13	Logic Analyzer Data 6.
FPGA_LA_DATA[7]	0	A13	Logic Analyzer Data 7.

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Xilinx Spartan 3A XC3S1400A FPGA Pin Out			
Signal Name	**Bank #**	**Pin #**	**Description**
No Connect	0	E9	Unused Pin.
No Connect	0	E8	Unused Pin.
No Connect	0	G9	Unused Pin.
FPGA_TMPSENS_1B_MOSI	0	F8	Temperature Sensor 1B Master-Out-Slave-In (MOSI).
FPGA_PUSHBUTTON[1]	0	G8	Push-Button 1 (Active Low).
FPGA_PUSHBUTTON[2]	0	G7	Push-Button 2 (Active Low).
Bank 1			
FPGA_ASAP1_SPI_LOAD	1	W21	AsAP #1 Serial Load Enable (Active High).
FPGA_ASAP1_SPI_CLK	1	Y21	AsAP #1 Serial Clock.
FPGA_ASAP1_CFG_CLK	1	W20	AsAP #1 Configuration Clock.
FPGA_ASAP1_SPI_MOSI	1	Y22	AsAP #1 Serial Master-Out-Slave-In (MOSI).
FPGA_ASAP1_SPI_CSN	1	W22	AsAP #1 Serial Chip Select (Active Low).
No Connect	1	T17	Unused Pin.
No Connect	1	T18	Unused Pin.
FPGA_DAC5682_SDO	1	U19	DAC5682Z Serial Data Output.
FPGA_ASAP1_RESET_COLD	1	V19	AsAP #1 Reset Cold (Active High).
FPGA_ASAP1_CFG_VALID	1	W19	AsAP #1 Configuration Valid.
FPGA_ASAP1_RST_CNTCLK	1	V20	AsAP #1 Reset Counter Clock.
FPGA_DAC5682_RSTB	1	U20	DAC5682Z Reset (Active Low).
FPGA_DAC5682_SDENB	1	U21	DAC5682Z Serial Data Enable (Active Low).
FPGA_DAC5682_SCLK	1	V22	DAC5682Z Serial Clock.
No Connect	1	T19	Unused Pin.
No Connect	1	T20	Unused Pin.
FPGA_DAC5682_SDIO	1	U22	DAC5682Z Serial Data Input.
FPGA_TMPSENS_2A_SCK	1	R19	Temperature Sensor 2A Serial Clock.
FPGA_TMPSENS_2A_MOSI	1	R20	Temperature Sensor 2A Master-Out-Slave-In (MOSI).
No Connect	1	T22	Unused Pin.
FPGA_TMPSENS_2A_CSN	1	R21	Temperature Sensor 2A Chip Select (Active Low).
No Connect	1	R22	Unused Pin.
FPGA_AD9516_PD	1	P20	AD9516 Power Down (Active Low).
CUST_INIT_B	1	B21	Virtex-5 INIT_B (Active Low).
FPGA_DP_CTRL_GPIO[4]	1	E22	Data Path Control GPIO Bit 4.
CUST_CCLK	1	C21	Virtex-5 Configuration Clock.
CUST_PROG_B	1	C22	Virtex-5 PROG_B (Active Low).
No Connect	1	E20	Unused Pin.
FPGA_DP_CTRL_GPIO[3]	1	D22	Data Path Control GPIO Bit 3.
FPGA_DP_CTRL_GPIO[2]	1	D21	Data Path Control GPIO Bit 2.
FPGA_DP_CTRL_MISO	1	F18	Data Path Control Serial Master-In-Slave-Out (MISO).
FPGA_DP_CTRL_RSTN	1	F19	Data Path Control Reset (Active Low).
FPGA_DP_CTRL_SCK	1	F20	Data Path Control Serial Clock.
FPGA_DP_CTRL_CSN	1	F21	Data Path Control Serial Chip Select (Active Low).
FPGA_DP_CTRL_MOSI	1	F22	Data Path Control Serial Master-Out-Slave-In (MOSI).
No Connect	1	G22	Unused Pin.
FPGA_DP_CTRL_GPIO[1]	1	D20	Data Path Control GPIO Bit 1.
FPGA_ASAP1_SPI_MISO	1	AA22	AsAP #1 Serial Master-In-Slave-Out (MISO).
CUST_CFG_DONE	1	B22	Virtex-5 Configuration Done (Active High).
FPGA_AD9516_SYNC	1	M22	AD9516 Sync.
No Connect	1	K17	Unused Pin.
No Connect	1	K18	Unused Pin.
No Connect	1	K19	Unused Pin.

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Xilinx Spartan 3A XC3S1400A FPGA Pin Out			
Signal Name	**Bank #**	**Pin #**	**Description**
No Connect	1	L19	Unused Pin.
FPGA_AD9516_CSB	1	N19	AD9516 Chip Select (Active Low).
FPGA_AD9516_SDIO	1	N20	AD9516 Serial Data Input.
FPGA_AD9516_RESET	1	N21	AD9516 Reset (Active High).
FPGA_AD9516_REF_SEL	1	N22	AD9516 Reference Select.
No Connect	1	L22	Unused Pin.
No Connect	1	L21	Unused Pin.
No Connect	1	L20	Unused Pin.
No Connect	1	M18	Unused Pin.
No Connect	1	M20	Unused Pin.
No Connect	1	K20	Unused Pin.
No Connect	1	U18	Unused Pin.
No Connect	1	R15	Unused Pin.
No Connect	1	R16	Unused Pin.
No Connect	1	P15	Unused Pin.
No Connect	1	P16	Unused Pin.
No Connect	1	R17	Unused Pin.
FPGA_TMPSENS_2A_MISO	1	R18	Temperature Sensor 2A Master-In-Slave-Out (MISO).
FPGA_AD9516_SDO	1	P22	AD9516 Serial Data Output.
No Connect	1	N15	Unused Pin.
No Connect	1	N16	Unused Pin.
FPGA_AD9516_LD	1	P18	AD9516 Lock Detect.
FPGA_AD9516_SCLK	1	N18	AD9516 Serial Clock.
FPGA_AD9516_STATUS	1	N17	AD9516 Status.
FPGA_AD9516_REFMON	1	M17	AD9516 Reference Monitor.
No Connect	1	M16	Unused Pin.
FPGA_TMPSENS_2B_MOSI	1	J22	Temperature Sensor 2B Master-Out-Slave-In (MOSI).
FPGA_TMPSENS_2B_CSN	1	K22	Temperature Sensor 2B Chip Select (Active Low).
No Connect	1	M15	Unused Pin.
No Connect	1	L16	Unused Pin.
No Connect	1	L18	Unused Pin.
FPGA_TMPSENS_2B_SCK	1	J21	Temperature Sensor 2B Serial Clock.
FPGA_TMPSENS_2B_MISO	1	J20	Temperature Sensor 2B Master-In-Slave-Out (MISO).
No Connect	1	H22	Unused Pin.
No Connect	1	L15	Unused Pin.
No Connect	1	K16	Unused Pin.
No Connect	1	H21	Unused Pin.
No Connect	1	H20	Unused Pin.
No Connect	1	K14	Unused Pin.
No Connect	1	K15	Unused Pin.
No Connect	1	G19	Unused Pin.
No Connect	1	G20	Unused Pin.
No Connect	1	J18	Unused Pin.
No Connect	1	H19	Unused Pin.
No Connect	1	H17	Unused Pin.
No Connect	1	H18	Unused Pin.
FPGA_DP_CTRL_GPIO[0]	1	J16	Data Path Control GPIO Bit 0.
No Connect	1	J15	Unused Pin.
FPGA_DP_CTRL_INTN	1	G18	Data Path Service Request (Active Low).
No Connect	1	G17	Unused Pin.

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Xilinx Spartan 3A XC3S1400A FPGA Pin Out			
Signal Name	**Bank #**	**Pin #**	**Description**
No Connect	1	H16	Unused Pin.
No Connect	1	H15	Unused Pin.
Bank 2			
FPGA_FTDI_RDN	2	U13	FTDI Read Enable (Active Low).
FPGA_TMPSENS_1C_CSN	2	Y17	Temperature Sensor 1C Chip Select (Active Low).
FPGA_ASAP2_RST_CNTCLK	2	AA17	AsAP #2 Reset Counter Clock.
FPGA_AMC6821_FAN2_SCK	2	AB9	AMC6821 Fan #2 I^2C Serial Clock.
FPGA_SLOTID[2]	2	T11	Slot ID Bit 2.
FPGA_REACH_TX	2	U12	Reach Technologies Display RS-232 Transmit Data.
FPGA_REACH_RX	2	V12	Reach Technologies Display RS-232 Receive Data.
FPGA_CLK100MHZ_N	2	AB12	100MHz Clock (Negative Differential).
FPGA_CLK100MHZ_P	2	AA12	100MHz Clock (Positive Differential).
No Connect	2	Y12	Unused Pin.
No Connect	2	W12	Unused Pin.
FPGA_RS232_RX	2	AB5	CP2102 RS-232 Receive Data.
FPGA_TMPSENS_1A_MISO	2	AB6	Temperature Sensor 1A Master-In-Slave-Out (MISO).
FPGA_RS232_CTS	2	Y6	CP2102 RS-232 Clear To Send Signal.
No Connect	2	W6	Unused Pin.
FPGA_RS232_RTS	2	AA6	CP2102 RS-232 Ready To Send Signal.
FPGA_SD_BUSY_LED	2	AB4	microSD Card Busy LED (Active Low).
FPGA_SD_RXD	2	AB3	microSD Card Receive Data.
FPGA_SD_CLK	2	AA3	microSD Card Serial Clock.
FPGA_SLOTID[1]	2	T10	Slot ID Bit 1.
FPGA_SD_TXD	2	AB2	microSD Card Transmit Data.
FPGA_AMC6821_FAN2_SMBALERTN	2	T9	AMC6821 Fan #2 SMB Alert (Active Low).
FPGA_SD_CARD_DETECT	2	AA4	microSD Card Chip Select (Active Low).
FPGA_AMC6821_FAN1_FAULTN	2	T7	AMC6821 Fan #1 Fault Flag (Active Low.)
FPGA_AMC6821_FAN1_THERMN	2	U7	AMC6821 Fan #1 Thermal Flag (Active Low.)
FPGA_SLOTID[0]	2	R11	Slot ID Bit 0.
FPGA_FTDI_TXEN	2	P12	FTDI Transmit Enable (Active Low).
FPGA_FTDI_RXFN	2	R12	FTDI Receive Data Enable (Active Low).
FPGA_FTDI_PWRENN	2	R13	FTDI Power Enable (Active Low).
No Connect	2	U11	Unused Pin.
FPGA_RS232_TX	2	Y5	CP2102 RS-232 Transmit Data.
No Connect	2	T16	Unused Pin.
FPGA_TMPSENS_1C_MISO	2	U16	Temperature Sensor 1C Master-In-Slave-Out (MISO).
FPGA_TMPSENS_1C_SCK	2	V17	Temperature Sensor 1C Serial Clock.
FPGA_AMC6821_FAN1_OVRN	2	T8	AMC6821 Fan #1 Over Temp Flag (Active Low.)
FPGA_AMC6821_FAN1_SMBALERTN	2	V7	AMC6821 Fan #1 SMB Alert (Active Low).
FPGA_AMC6821_FAN2_FAULTN	2	U8	AMC6821 Fan #2 Fault Flag (Active Low.)
FPGA_AMC6821_FAN1_SCK	2	W7	AMC6821 Fan #1 I^2C Serial Clock.
FPGA_AMC6821_FAN2_THERMN	2	V8	AMC6821 Fan #2 Thermal Flag (Active Low.)
FPGA_AMC6821_FAN1_SDA	2	Y7	AMC6821 Fan #1 I^2C Serial Data.
FPGA_TMPSENS_1A_SCK	2	AB7	Temperature Sensor 1A Serial Clock.
FPGA_AMC6821_FAN2_SDA	2	Y9	AMC6821 Fan #2 I^2C Serial Data.
CUST_TDO	2	U10	Custom JTAG TDO Signal for Configuration via MicroBlaze.
FPGA_TMPSENS_1A_CSN	2	AA8	Temperature Sensor 1A Chip Select (Active Low).
FPGA_TMPSENS_1A_MOSI	2	AB8	Temperature Sensor 1A Master-Out-Slave-In (MOSI).
CUST_TCK	2	Y10	Custom JTAG TCK Signal for Configuration via MicroBlaze.
JTAG_CCN	2	V10	Xilinx JTAG Cable Connected Signal (Active Low).

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Xilinx Spartan 3A XC3S1400A FPGA Pin Out			
Signal Name	**Bank #**	**Pin #**	**Description**
CUST_TDI	2	AA10	Custom JTAG TDI Signal for Configuration via MicroBlaze.
CUST_TMS	2	AB10	Custom JTAG TMS Signal for Configuration via MicroBlaze.
FPGA_FTDI_WRN	2	V14	FTDI Write Enable (Active Low).
FPGA_FTDI_DATA[3]	2	W16	FTDI Data Bit 3.
FPGA_FTDI_DATA[0]	2	V15	FTDI Data Bit 0.
FPGA_FTDI_DATA[1]	2	V16	FTDI Data Bit 1.
No Connect	2	Y13	Unused Pin.
No Connect	2	Y14	Unused Pin.
FPGA_FTDI_SI_WU	2	W13	FTDI Send Immediate / Wake Up Enable.
FPGA_FTDI_DATA[2]	2	W15	FTDI Data Bit 2.
S3A_SPI_WPN	2	AA14	Spartan-3A SPI Write Protect Signal (Active Low).
S3A_SPI_HOLDN	2	AB13	Spartan-3A SPI Hold Signal (Active Low).
FPGA_TMPSENS_1C_MOSI	2	W17	Temperature Sensor 1C Master-Out-Slave-In (MOSI).
FPGA_FTDI_DATA[4]	2	Y15	FTDI Data Bit 4.
FPGA_FTDI_DATA[6]	2	AB15	FTDI Data Bit 6.
FPGA_FTDI_DATA[7]	2	AB16	FTDI Data Bit 7.
S3A_SPI_DATA_TO_V5	2	AA15	Spartan-3A Serial Data Output to Virtex-5.
FPGA_FTDI_DATA[6]	2	Y16	FTDI Data Bit 6.
FPGA_ASAP2_RESET_COLD	2	AB17	AsAP #2 Reset Cold (Active High).
FPGA_ASAP2_SPI_CLK	2	AB18	AsAP #2 Serial Clock.
FPGA_ASAP2_MOSI	2	Y18	AsAP #2 Master-Out-Slave-In (MOSI).
FPGA_ASAP2_MISO	2	W18	AsAP #2 Master-In-Slave-Out (MISO).
FPGA_ASAP2_CFG_CLK	2	AA21	AsAP #2 Configuration Clock.
FPGA_ASAP2_CFG_VALID	2	AB21	AsAP #2 Configuration Valid.
FPGA_ASAP2_SPI_CSN	2	AA19	AsAP #2 Serial Chip Select (Active Low).
FPGA_ASAP2_SPI_LOAD	2	AB19	AsAP #2 Serial Load Enable (Active High).
FPGA_AMC6821_FAN2_OVRN	2	V9	AMC6821 Fan #1 Over Temp Flag (Active Low.)
S3A_CCLK	2	AA20	Spartan-3A Configuration Clock.
S3A_INIT_B	2	V13	Spartan-3A Configuration Initialization (Active Low).
S3A_M0	2	W5	Spartan-3A Configuration Mode Pin 0.
S3A_M1	2	V6	Spartan-3A Configuration Mode Pin 1.
S3A_M2	2	W4	Spartan-3A Configuration Mode Pin 2.
S3A_SPI_CSO	2	Y4	Spartan-3A SPI Chip Select (Active Low).
No Connect	2	AB11	Unused Pin.
S3A_SPI_MISO	2	AB20	Spartan-3A SPI Master-In-Slave-Out (MISO).
S3A_SPI_MOSI	2	AB14	Spartan-3A SPI Master-Out-Slave-In (MOSI).
No Connect	2	Y11	Unused Pin.
S3A_V0	2	Y8	Spartan-3A SPI Mode Pin 0.
S3A_V1	2	W8	Spartan-3A SPI Mode Pin 1.
S3A_V2	2	W9	Spartan-3A SPI Mode Pin 2.
No Connect	2	V11	Unused Pin.
No Connect	2	T13	Unused Pin.
No Connect	2	T15	Unused Pin.
No Connect	2	U15	Unused Pin.
No Connect	2	T14	Unused Pin.
FPGA_HWID[0]	2	R9	Hardware ID Bit 0.
FPGA_FTDI_RSTOUTN	2	R14	FTDI Reset Output (Active Low).
FPGA_HWID[1]	2	R10	Hardware ID Bit 1.
Bank 3			
FPGA_DDR_SDRAM_ADDR[0]	3	K5	DDR SDRAM Address.

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Xilinx Spartan 3A XC3S1400A FPGA Pin Out			
Signal Name	**Bank #**	**Pin #**	**Description**
FPGA_DDR_SDRAM_ADDR[1]	3	K2	DDR SDRAM Address.
FPGA_DDR_SDRAM_ADDR[2]	3	K3	DDR SDRAM Address.
FPGA_DDR_SDRAM_ADDR[3]	3	L3	DDR SDRAM Address.
FPGA_DDR_SDRAM_ADDR[4]	3	L5	DDR SDRAM Address.
FPGA_DDR_SDRAM_ADDR[5]	3	L1	DDR SDRAM Address.
FPGA_DDR_SDRAM_ADDR[6]	3	K1	DDR SDRAM Address.
FPGA_DDR_SDRAM_ADDR[7]	3	M2	DDR SDRAM Address.
FPGA_DDR_SDRAM_ADDR[8]	3	M1	DDR SDRAM Address.
FPGA_DDR_SDRAM_ADDR[9]	3	M4	DDR SDRAM Address.
FPGA_DDR_SDRAM_ADDR[10]	3	M3	DDR SDRAM Address.
FPGA_DDR_SDRAM_ADDR[11]	3	Y2	DDR SDRAM Address.
FPGA_DDR_SDRAM_ADDR[12]	3	Y1	DDR SDRAM Address.
FPGA_DDR_SDRAM_BA[0]	3	H2	DDR SDRAM Bank Address.
FPGA_DDR_SDRAM_BA[1]	3	K4	DDR SDRAM Bank Address.
FPGA_DDR_SDRAM_CASN	3	G3	DDR SDRAM Column Address Strobe (Active Low).
FPGA_DDR_SDRAM_CKE	3	H1	DDR SDRAM Clock Enable (Active Low).
+1.25V DDR VREF	3	R6	DDR SDRAM Reference Voltage.
FPGA_DDR_SDRAM_CLKFB	3	W3	DDR SDRAM Clock Feedback Input.
FPGA_DDR_SDRAM_CLK_N	3	AA2	DDR SDRAM Clock (Negative Differential).
FPGA_DDR_SDRAM_CLK_P	3	AA1	DDR SDRAM Clock (Positive Differential).
FPGA_DDR_SDRAM_CSN	3	H4	DDR SDRAM Chip Select (Active Low).
FPGA_DDR_SDRAM_DATA[0]	3	W1	DDR SDRAM Data.
FPGA_DDR_SDRAM_DATA[1]	3	W2	DDR SDRAM Data.
FPGA_DDR_SDRAM_CLKFB	3	V4	DDR SDRAM Clock Feedback Output.
FPGA_DDR_SDRAM_DATA[2]	3	U3	DDR SDRAM Data.
FPGA_DDR_SDRAM_DATA[3]	3	U4	DDR SDRAM Data.
FPGA_DDR_SDRAM_DATA[4]	3	V1	DDR SDRAM Data.
FPGA_DDR_SDRAM_DATA[5]	3	V3	DDR SDRAM Data.
FPGA_DDR_SDRAM_DATA[6]	3	U1	DDR SDRAM Data.
FPGA_DDR_SDRAM_DATA[7]	3	U2	DDR SDRAM Data.
FPGA_DDR_SDRAM_DATA[8]	3	R5	DDR SDRAM Data.
FPGA_DDR_SDRAM_DATA[9]	3	R4	DDR SDRAM Data.
FPGA_DDR_SDRAM_DATA[10]	3	R3	DDR SDRAM Data.
FPGA_DDR_SDRAM_DATA[11]	3	R2	DDR SDRAM Data.
FPGA_DDR_SDRAM_DATA[12]	3	P3	DDR SDRAM Data.
FPGA_DDR_SDRAM_DATA[13]	3	P5	DDR SDRAM Data.
FPGA_DDR_SDRAM_DATA[14]	3	P1	DDR SDRAM Data.
FPGA_DDR_SDRAM_DATA[15]	3	P2	DDR SDRAM Data.
FPGA_DDR_SDRAM_LDM	3	T4	DDR SDRAM Lower Data Mask.
FPGA_DDR_SDRAM_LDQS	3	U5	DDR SDRAM Lower Data Strobe.
FPGA_DDR_SDRAM_RASN	3	H3	DDR SDRAM Row Address Strobe (Active Low).
FPGA_DDR_SDRAM_UDM	3	R1	DDR SDRAM Upper Data Mask.
FPGA_DDR_SDRAM_UDQS	3	N4	DDR SDRAM Upper Data Strobe.
FPGA_DDR_SDRAM_WEN	3	G1	DDR SDRAM Write Enable (Active Low).
No Connect	3	R7	Unused Pin.
+1.25V DDR VREF	3	T6	DDR SDRAM Reference Voltage.
No Connect	3	T5	Unused Pin.
No Connect	3	R8	Unused Pin.
No Connect	3	P7	Unused Pin.
No Connect	3	T3	Unused Pin.

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Xilinx Spartan 3A XC3S1400A FPGA Pin Out			
Signal Name	**Bank #**	**Pin #**	**Description**
+1.25V DDR VREF	3	T1	DDR SDRAM Reference Voltage.
No Connect	3	P8	Unused Pin.
No Connect	3	N7	Unused Pin.
No Connect	3	N5	Unused Pin.
No Connect	3	N6	Unused Pin.
No Connect	3	M5	Unused Pin.
No Connect	3	N9	Unused Pin.
No Connect	3	N8	Unused Pin.
+1.25V DDR VREF	3	N1	DDR SDRAM Reference Voltage.
No Connect	3	N3	Unused Pin.
No Connect	3	M6	Unused Pin.
No Connect	3	M7	Unused Pin.
No Connect	3	M8	Unused Pin.
No Connect	3	L7	Unused Pin.
+1.25V DDR VREF	3	J1	DDR SDRAM Reference Voltage.
No Connect	3	J3	Unused Pin.
+1.25V DDR VREF	3	L8	DDR SDRAM Reference Voltage.
No Connect	3	K7	Unused Pin.
No Connect	3	K8	Unused Pin.
No Connect	3	F2	Unused Pin.
No Connect	3	J7	Unused Pin.
No Connect	3	J5	Unused Pin.
No Connect	3	H6	Unused Pin.
No Connect	3	K6	Unused Pin.
No Connect	3	G4	Unused Pin.
No Connect	3	H5	Unused Pin.
No Connect	3	F3	Unused Pin.
+1.25V DDR VREF	3	J8	DDR SDRAM Reference Voltage.
No Connect	3	G5	Unused Pin.
No Connect	3	G6	Unused Pin.
+1.25V DDR VREF	3	H7	DDR SDRAM Reference Voltage.
No Connect	3	H8	Unused Pin.
No Connect	3	D3	Unused Pin.
No Connect	3	C2	Unused Pin.
No Connect	3	B1	Unused Pin.
No Connect	3	D2	Unused Pin.
No Connect	3	C1	Unused Pin.
No Connect	3	E4	Unused Pin.
No Connect	3	E1	Unused Pin.
No Connect	3	D1	Unused Pin.
No Connect	3	F4	Unused Pin.
No Connect	3	E3	Unused Pin.
No Connect	3	F1	Unused Pin.

7 Electrical Specifications

7.1 Power Consumption

7.1.1 Total Power Consumption

Table 7.1: Total Power Supply Current Usage

Total Power Supply Current Usage		
ITEM	**+12V**	**TOTAL PWR**
Analog Power Supply Current Usage	1.322989	15.875872
Digital Power Supply Current Usage	4.933585	59.203015
TOTAL CURRENT (A)	6.256574	
TOTAL POWER (W)	75.078888	75.078888

7.1.2 Analog Power Consumption

Table 7.2: Analog Power Supply Current Usage

Analog Power Supply Current Usage					
ITEM	**+12V**	**+5.5V**	**+2.5V**	**-6V**	**TOTAL PWR**
THS4302 Fixed-Gain Op-Amp 14dB	0.130	0.284	0.000	0.000	1.560000
THS4509 Wide-Band Differential Op-Amp 8dB	0.043	0.095	0.000	0.000	0.520000
ADS5463 12-bit, 500MS/s ADC	0.333	0.725	0.000	0.000	3.990000
SN74LVC2G125 x12	0.0000260	0.0000567	0.000	0.000	0.000312
DAC5682Z 16-bit, 1GS/s DAC	0.288	0.300	0.720	0.000	3.450000
OPA695 Op-Amp	0.128	0.142	0.000	-0.125	1.530000
Vectron 10MHz TCXO Oscillator	0.003	0.006	0.000	0.000	0.033000
On Semiconductor - NB6L11MMNG	0.021	0.045	0.000	0.000	0.247500
Micrel - SY58017UMG	0.019	0.042	0.000	0.000	0.231000
Micrel - SY58017UMG	0.019	0.042	0.000	0.000	0.231000
Micrel - SY58017UMG	0.019	0.042	0.000	0.000	0.231000
Micrel - SY58011UMG	0.026	0.057	0.000	0.000	0.313500
Micrel - SY58608UMG	0.022	0.048	0.000	0.000	0.264000
Texas Instruments - ONET1191PRGTT	0.013	0.029	0.000	0.000	0.161700
On Semiconductor - MC10EP89DTG	0.030	0.065	0.000	0.000	0.356400
On Semiconductor - NB4N527S	0.015	0.032	0.000	0.000	0.174900
On Semiconductor - MC10EP89DTG	0.028	0.060	0.000	0.000	0.330000
Analog Devices AD9516	0.138	0.300	0.000	0.000	1.650000
Micrel - SY58601UMG - Trigger Out	0.013	0.027	0.000	0.000	0.150000
SN65LVDS1 (x2)	0.004	0.009	0.000	0.000	0.050000
UMC: UMX-244-B14	0.033	0.000	0.000	0.000	0.400000
TOTAL CURRENT (A)	1.322989	2.350159	0.720000	-0.125000	
TOTAL POWER (W)	15.875872	12.925872	1.800000	0.750000	15.8758720

7.1.3 Digital Power Consumption

Table 7.3: Digital Power Supply Current Usage

Digital Power Supply Current Usage		
ITEM	**+12V**	**Total Power**
XC5VSX50T-3FF1136C (Virtex 5 SX50T)	1.531	18.366600
DDR2 SDRAM SODIMM (MT16HTF25664H)	0.620	7.434000
QDR-II SRAM (K7R323684C-EC250)	0.214	2.565000
AsAP DSP IC (x2)	1.617	19.400000
XC3S1400A-4FG484 (Spartan 3A)	0.088	1.052000
M25P64-VMF6TP (SPI Flash 64 Mb)	0.006	0.066000
TPS3823-25DBVT (Reset uChip)	0.000006875	0.000083
TPS3823-25DBVT (Config Hold-Off uChip)	0.000006875	0.000083
CSX750FB (14.7456 MHz)	0.004	0.049500
MT46V32M16BN-6 (DDR SDRAM)	0.141	1.687500
SN74LVC1G08 (Single 2-Input AND Gate)	0.000002750	0.000033
SN74LVC1G32 (Single 2-Input OR Gate)	0.000002750	0.000033
CP2102 (USB-to-RS-232 Bridge IC)	0.022	0.264000
CP2102 (USB-to-RS-232 Bridge IC)	0.022	0.264000
MicroSD Card	0.083	0.990000
MicroSD Card	0.083	0.990000
ADR03 +2.5V Precision Ref for V5 SM	0.010	0.120000
AMC6821 (x2)	0.006	0.066000
XC9572XL-10VQ44	0.011	0.132000
CCLD-033-50-100.00 (x2)	0.035	0.422400
FTDI FT245BL (x2)	0.021	0.251320
User Interface Board	0.417	5.000000
Temperature Sensor (TMP125) (x6)	0.000110	0.001320
SN65LVDT2DBVR (TTL-to-LVDS)	0.002750	0.033000
TPS3808G25DRV (x2)	0.000012	0.000144
TL7733BCDR	0.004	0.048000
TOTAL CURRENT (A)	4.933585	
TOTAL POWER (W)	59.203015	59.203015

Table 7.4: Digital Power Supply Current Usage Detail

Digital Power Supply Current Usage Detail										
ITEM	**+0.9V**	**+1V**	**+1V AsAP**	**+1.2V**	**+1.25Vref**	**+1.3V**	**+1.8V**	**+2.5V**	**+3.3V**	**+5V**
XC5VSX50T-3FF1136C (Virtex 5 SX50T)	1.710	3.737	0	0	0	0	2.723	3.138	0.104	0
DDR2 SDRAM SODIMM (MT16HTF25664H)	1.260	0	0	0	0	0	3.500	0	0	0
QDR-II SRAM (K7R323684C-EC250)	0.450	0	0	0	0	0	1.200	0	0	0
AsAP DSP IC (x2)	0	0	4	0	0	8	0	2.000	0	0
XC3S1400A-4FG484 (Spartan 3A)	0	0	0	0.134	0	0	0	0.173	0.13900	0
M25P64-VMF6TP (SPI Flash 64 Mb)	0	0	0	0	0	0	0	0	0.0200	0
TPS3823-25DBVT (Reset uChip)	0	0	0	0	0	0	0	0	0.000025	0
TPS3823-25DBVT (Config Hold-Off uChip)	0	0	0	0	0	0	0	0	0.000025	0
CSX750FB (14.7456 MHz)	0	0	0	0	0	0	0	0	0.015000	0
MT46V32M16BN-6 (DDR SDRAM)	0	0	0	0	0.450	0	0	0.450	0	0
SN74LVC1G08 (Single 2-Input AND Gate)	0	0	0	0	0	0	0	0	0.000010	0
SN74LVC1G32 (Single 2-Input OR Gate)	0	0	0	0	0	0	0	0	0.000010	0
CP2102 (USB-to-RS-232 Bridge IC)	0	0	0	0	0	0	0	0	0.080000	0
CP2102 (USB-to-RS-232 Bridge IC)	0	0	0	0	0	0	0	0	0.080000	0
MicroSD Card	0	0	0	0	0	0	0	0	0.300000	0
MicroSD Card	0	0	0	0	0	0	0	0	0.300000	0
ADR03 +2.5V Precision Ref for V5 SM	0	0	0	0	0	0	0	0	0	0
AMC6821 (x2)	0	0	0	0	0	0	0	0	0.020000	0
XC9572XL-10VQ44	0	0	0	0	0	0	0	0	0.040000	0
CCLD-033-50-100.00 (x2)	0	0	0	0	0	0	0	0	0.128000	0
FTDI FT245BL (x2)	0	0	0	0	0	0	0	0	0.000400	0.05
User Interface Board	0	0	0	0	0	0	0	0	0	1.00
Temperature Sensor (TMP125) (x6)	0	0	0	0	0	0	0	0	0.000400	0
SN65LVDT2DBVR (TTL-to-LVDS)	0	0	0	0	0	0	0	0	0.010000	0
TPS3808G25DRV (x2)	0	0	0	0	0	0	0	0	0	0
TL7733BCDR	0	0	0	0	0	0	0	0	0	0
TOTAL CURRENT (A)	3.420	3.737	4	0.134	0.4500	8	7.423	5.76140	1.236870	1.05
TOTAL POWER (W)	3.078	3.737	4	0.161	0.5625	10.4	13.361	14.4035	4.081671	5.25

8 Analog Design Requirements

8.1 THS4302 Op-Amp Decoupling Requirements

Power supply decoupling is a critical aspect of any high-performance amplifier design process. Careful decoupling provides higher quality AC performance (most notably improved distortion performance). The following guidelines ensure the highest level of performance with the THS4302[7].

1. Place decoupling capacitors as close to the power supply inputs as possible, with the goal of minimizing the inductance of the path from ground to the power supply. Inductance in series with the bypass capacitors will degrade performance. Note that a narrow lead or trace has about 0.8nH of inductance for every millimeter of length. Each printed-circuit board (PCB) via also has between 0.3nH and 0.8nH depending on length and diameter. For these reasons, it is recommended to use a power supply trace about the width of the package for each power supply lead to the capacitors, and 3 or more vias to connect the capacitors to the ground plane.

2. Placement priority should put the smallest valued capacitors closest to the device.

3. Solid power planes can lead to PCB resonances when they are not properly terminated to the ground plane over the area and along the perimeter of the power plane by high frequency capacitors. Doing so ensures that there are no power plane resonances in the needed frequency range. Values used are in the range of 2pF to 50pF, depending on the frequencies to be supressed, with numerous vias for each. Using 0402 or smaller component sizes is recommended. An approximate expression for the resonant frequencies associated with a length of one of the power plane dimensions is given in Equation 8.1. Note that a power plane of arbitrary shape can have a number of resonant frequencies. A power plane without distributed capacitors and with active parts near the center of the plane usually has *n* even ($\geq$ 2) due to the half wave resonant nature of the plane.

$$f_{res} \approx \frac{n \cdot (44GHz/mm)}{l} \tag{8.1}$$

   In Equation 8.1, f_{res} is the approximate power plane resonant frequencies in GHz, l is the length of the power plane dimensions in millimeters, n is an integer (n $>$ 1) related to the mode of the oscillation. For guidance on capacitor spacing over the area on the ground plane, specify the lowest resonant frequency to be tolerated, then solve using the equation above, with n = 2. Use this length for the capacitor spacing. It is recommended that a power plane, if used, be either small enough, or decoupled as described, so that there are no resonances in the frequency range of interest. An alternative is to use a ferrite bead outside the op-amp, high-frequency bypass capacitors to decouple the amplifier, and mid- and high-frequency bypass capacitors, from the power plane. When a trace is used to deliver power, its approximate self-resonance is given by the equation above, substituting the trace length for power plane dimension.

4. Bypass capacitors, because they have a self-inductance, resonate with each other. To achieve optimum transfer characteristics through 2GHz, it is recommended that the bypass arrangement employed in the prototype board be used. The 30.1Ω resistor in series with the 0.1μF capacitor reduces the Q of the resonance of the lumped parallel elements including the 0.1μF and 47pF capacitors, and the power supply input of the amplifier. The ferrite bead isolates the low-frequency 22μF capacitor and power plane from the remainder of the bypass network.

5. By removing the 30.1Ω resistor and ferrite bead, the frequency response characteristic above 400MHz may be modified. However, bandwidth, distortion, and transient response remain optimal.

6. Recommended values for power supply decoupling include a bulk capacitor (22μF), a ferrite bead with a high self-resonant frequency, a mid-range decoupling capacitor (0.1μF) in series with a 30.1Ω resistor, and a high-frequency decoupling capacitor (47pF).

9 Layout Notes

9.1 Mechanical

1. The tallest component allowed on the topside is 1.100“.
2. The tallest component allowed on the bottomside is 0.200“.

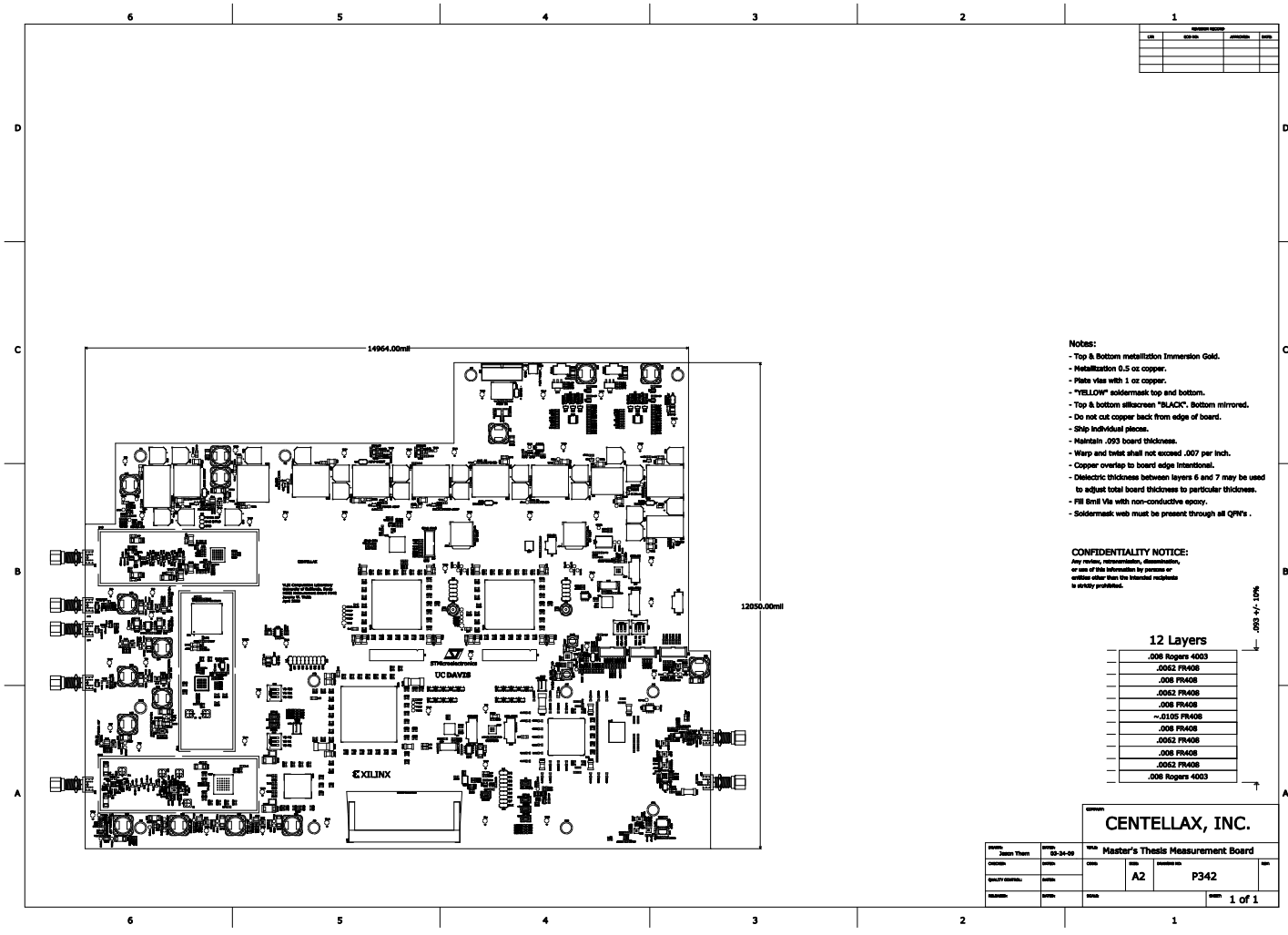

Figure 9.1: Measurement Board Assembly Top Diagram.

9.2 Board Construction: 12 Layer FR408/Rogers 4003 Core construction

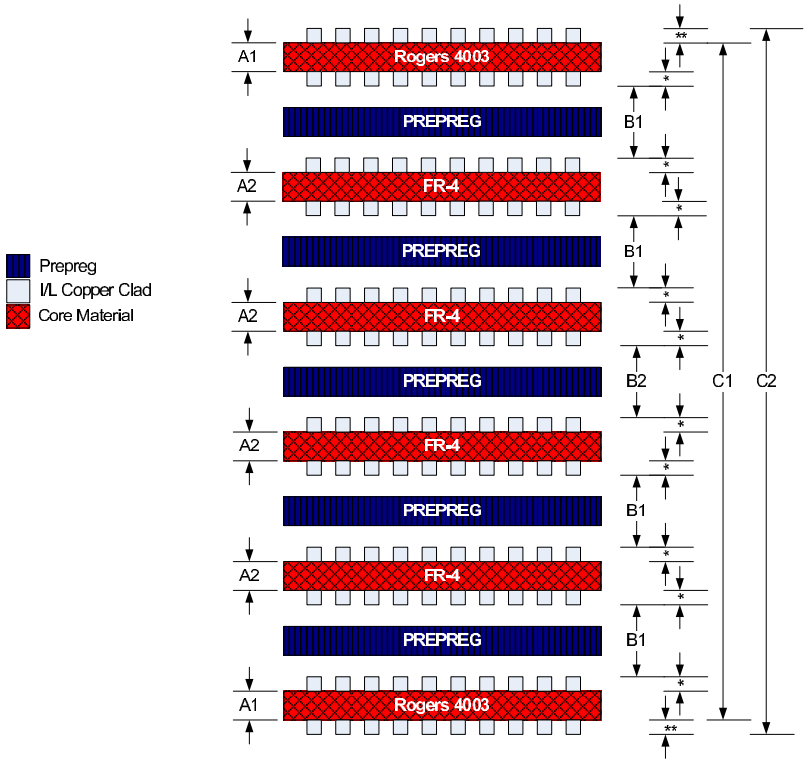

Figure 9.2: 12 Layer FR408/Rogers 4003 Core construction.

12 layer FR408/Rogers 4003 Core construction						
Construction Type	**A1 (inches)**	**A2 (inches)**	**B1 (inches)**	**B2 (inches)**	**C1 (inches)**	**C2 (inches)**
FR408/Rogers Mix	.008 ± .001	.008 ± .001	.0062 ± .0007	.0105 ± .0007	.08472-.09868	.08612-.10008

Table 9.1: 12 layer FR408/Rogers 4003 Core construction

* Copper thickness unless otherwise specified on inner layers: $\frac{1}{2}$ oz. Cu (0.0007“).

** Copper thickness unless otherwise specified on outer layers: $\frac{1}{2}$ oz. Cu (0.0007“ before plating).

A1 Rogers 4003 Core thickness

A2 FR408 Core thickness

B1 Pressed thickness of prepreg - 2x FR408 Prepreg 1080

B2 Pressed thickness of prepreg - 1x FR408 Prepreg 1080 and 1x FR408 Prepreg 7628

C1 Overall finished board thickness substrate-to-substrate

C2 Overall finished board thickness plated metal to plated metal. In addition, some surface coatings (i.e., HAL) can add up to 0.002“ of solder per side. Soldermask (also not specified) typically adds about 0.001” per side but can add up to 0.004“ per side in extreme examples.

9.3 Board Stackup and Transmission Lines

9.3.1 Board Stackup: 12 layer FR408/Rogers 4003 Stackup

The stackup for this 12-layer board is divided into two sections:

1. Analog
2. Digital

The stackup for the Analog section is shown in Table 9.2.

Table 9.2: 12 layer FR408/Rogers 4003 Analog Stackup

12 layer FR408/Rogers 4003 Analog Stackup		
Layer Name	**Signal or Plane**	**Description**
TOP	Signal	Routing
SIDE2	Plane	Ground
SIDE3	Signal	Routing
SIDE4	Signal	Routing
SIDE5	Plane	Ground
SIDE6	Signal	Power
SIDE7	Signal	Power
SIDE8	Plane	Ground
SIDE9	Signal	Power
SIDE10	Signal	Power
SIDE11	Plane	Ground
BOTTOM	Signal	Routing

The stackup for the Digital Section is shown in Table 9.3.

Table 9.3: 12 layer FR408/Rogers 4003 Digital Stackup

12 layer FR408/Rogers 4003 Digital Stackup		
Layer Name	**Signal or Plane**	**Description**
TOP	Signal	Routing, Ground and BGA Breakout
SIDE2	Plane	Ground
SIDE3	Signal	Routing - Offset Stripline
SIDE4	Signal	Routing - Offset Stripline
SIDE5	Plane	Ground
SIDE6	Signal	Power - +3.3V, +1.8V, and +5V
SIDE7	Signal	Power - +2.5V, +1.2V, and +1V
SIDE8	Plane	Ground
SIDE9	Signal	Routing - Offset Stripline
SIDE10	Plane	Routing - Offset Stripline
SIDE11	Plane	Ground
BOTTOM	Signal	Routing, Ground and BGA Breakout

9.3.2 Transmission Line Information

9.3.2.1 Microstrip Transmission Line Infomation

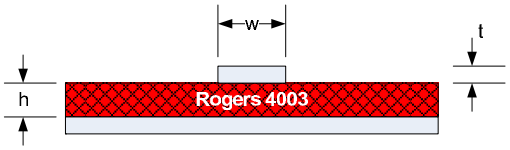

Figure 9.3: Single-Ended Microstrip

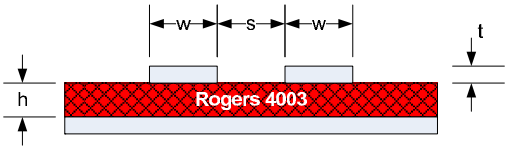

Figure 9.4: Differential Microstrip

Transmission Line	w (Inches)	h (Inches)	s (Inches)	t (oz)[Inches]	Z_o (Ohms)	ϵ_r
Single-Ended (Solder Mask)	0.015	0.008 $\pm$ 0.001	N/A	$\frac{1}{2}$[0.0007]	52 Ω	3.38
Single-Ended (No Solder Mask)	0.016	0.008 $\pm$ 0.001	N/A	$\frac{1}{2}$[0.0007]	52 Ω	3.38
Differential (Solder Mask)	0.010	0.008 $\pm$ 0.001	0.006	$\frac{1}{2}$[0.0007]	103 Ω	3.38

Table 9.4: Microstrip Transmission Line Information

9.3.2.2 Stripline Transmission Line Infomation

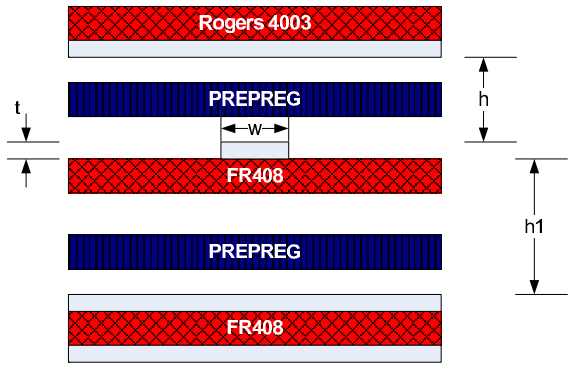

Figure 9.5: Single-Ended Stripline

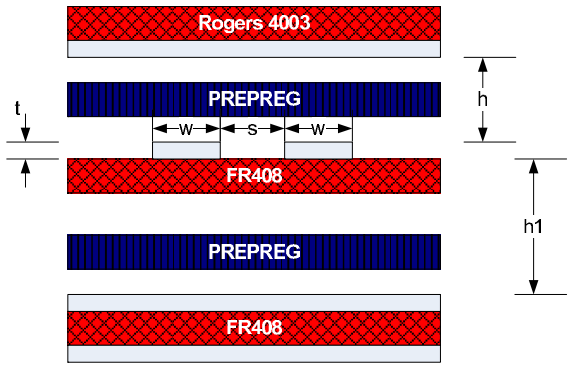

Figure 9.6: Differential Stripline

Transmission Line	h1 (Inches)	h (Inches)	w (Inches)	s (Inches)	t (oz)[Inches]	Z_o (Ohms)	ϵ_r
Single-Ended	0.0149 $\pm$ 0.0017	0.0062 $\pm$ 0.0007	0.007	N/A	$\frac{1}{2}$[0.0007]	49 Ω	3.90
Differential	0.0149 $\pm$ 0.0017	0.0062 $\pm$ 0.0007	0.004	0.004	$\frac{1}{2}$[0.0007]	107 Ω	3.90

Table 9.5: Stripline Transmission Line Information

9.3.2.3 Transmission Line Delay Infomation

For the Measurement Board's stackup the following metrics should be used:

- The estimated delay per inch for top/bottom microstrip is: $\sim$(130-140) ps/in.
- The estimated delay per inch for inner layer stripline is: $\sim$(160-170) ps/in.

9.4 Placement and Routing Constraints

9.4.1 DDR SDRAM Routing Constraints

1. DQ/DM to DQS/DQS# ± 25ps
2. Address/Control to CK/CK# ± 50ps
3. DQS/DQS# to CK/CK# ± 100ps
4. Feedback clock length = DQS + DRAM clock

Put the first three groups all in the same routing constraint group. The length matching constraint can be set to ± 70mils which comes out to ± 10 or 15 ps.

9.4.2 DDR2 SDRAM Routing Constraints

1. DQ/DM to DQS/DQS# ± 25ps
2. Address/Control to CK/CK# ± 50ps
3. DQS/DQS# to CK/CK# ± 100ps
4. Feedback clock length = DQS + DRAM clock

Put the first three groups all in the same routing constraint group. The length matching constraint can be set to ± 70mils which comes out to ± 10 or 15 ps.

9.4.3 QDR-II SRAM Routing Constraints

The source synchronous nature of the Read and Write path interfaces requires matched board trace lengths for the interface clock, data, and control signals.

For example, the trace lengths of the QDR II memory device input signals (QDR_K, QDR_K_n, QDR_W_n, QDR_R_n, QDR_SA, QDR_BW_n, and QDR_D) must be well matched to present the control, address, and data lines to the memory device with adequate setup and hold margins. The implementation of the physical interface ensures these signals are center aligned to the QDR_K and QDR_K_n clock edges when leaving the FPGA device outputs. The board traces must ensure that this relationship continues to the memory device inputs.

Similarly, the QDR II memory device output signals (QDR_Q, QDR_CQ) must have well-matched trace lengths for the signals to all arrive edge aligned at the inputs to the Virtex-5 device. This trace length matching is critical to the implementation of the direct-clocking Read data capture methodology. Any reasonable board design tool can match these traces within an acceptable tolerance with little effort.

9.4.4 ADS5463 Routing Constraints

1. Place a 6-by-6 array of thermal vias in the thermal pad area. These holes should be 13 mils in diameter. The small size prevents wicking of the solder through the holes.
2. It is recommended to place a small number of 25-mil-diameter holes under the package, but outside the thermal pad area to provide an additional heat path.
3. Connect all holes (both those inside and outside the thermal pad area) to an internal copper plane (such as a ground plane).
4. Do not use the typical web or spoke via-connection pattern when connecting the thermal vias to the ground plane. Flood the via, rather than using a spoke pattern. See Figure 9.7. [1]

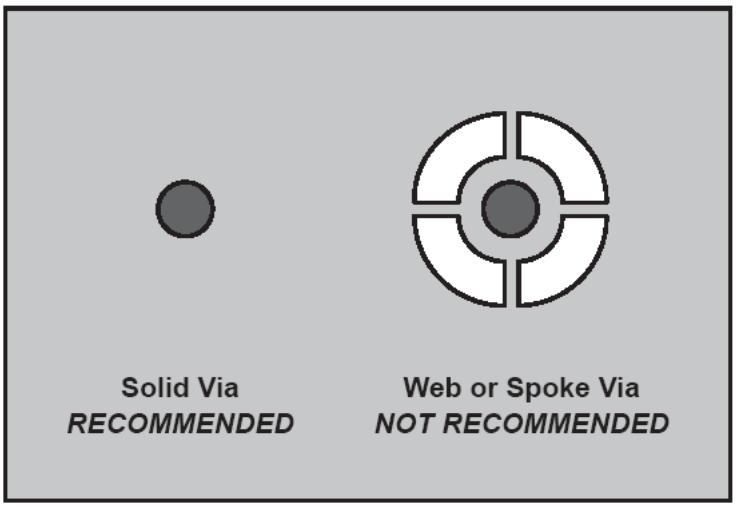

Figure 9.7: Via Connection.

9.4.5 DAC5682Z Routing Constraints

9.4.5.1 DAC5682z output, CLK, and power

Make all DAC5682 IOUT traces the same length ($\pm$ 2 mils).

The CLKIN and CLKINC inputs should be properly terminated at both ends. When using the DAC5682, a 100 Ω termination should be placed across the two CLKIN traces to terminate the source at the load. Two series capacitors should be used to AC couple the CLKIN signal before going into the self-biased CLKIN inputs of the DAC5682. All three components should be 0402 footprint and the resistor placed as close as possible to the CLKIN input pins.

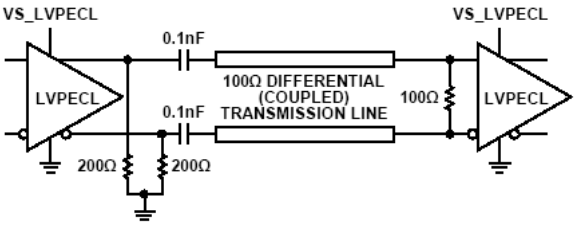

Figure 9.8: DAC5682Z High-Speed Clock Input.

When using the DAC5682, a 100 Ω termination should be placed across the two DCLK traces to terminate the source from a LVDS source. Two series capacitors should be used to AC couple the CLK signal before going into the self-biased CLK inputs of the DAC5682. The caps need to be placed after the 100 Ohm series resistor to allow for proper termination of these LVDS level signals. All three components should be 0402 footprint with the termination resistor placed before the series caps to allow for proper termination of the LVDS source. The three parts should be placed as close as possible to the DAC input pins.

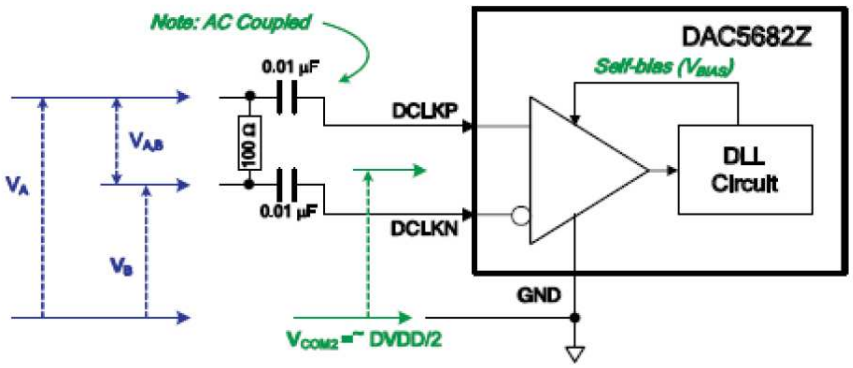

Figure 9.9: DAC5682Z Digital Clock Input.

The DAC5682 +1.8V source should be from a clean source. This should not be shared with the noisy +1.8V source, such as a high speed FPGA or ASIC. Make sure every power pin on the DAC including the VFUSE pin has a decoupling cap placed as close as possible to the pin.

Add a bulk decoupling cap (10 μF) to each of the power supplies feeding the DAC5682 and place near the device.

The user needs to be extremely careful if a switching regulator is used to generate the 1.8V rail (or 3.3V for that matter) - this usually leads to spurs at the switching regulator frequency, probably from bleeding in the clock path. We recommend linear regulation, from a 3.3V supply for example, to supply 1.8V.

Provide additional isolation of +1.8V with a ferrite bead to pins 44, 50 and 63 of the DAC5682 if possible. Make sure the decoupling caps for these pins are placed as close as possible to the pins and the connection made to the power plane are made with thick traces and several vias going to internal power planes. Place the caps on the component side if possible. Pins 50 and 63 are the 1.8V supplies to the DAC cores. These provide power for the binary to thermometer code logic, and the output current switch drivers (DAC DVDD). These circuits are all full rate, running at the final DAC sample rate. Pin 44 is the 1.8V bias for the fuse circuits. The fuse circuits store the adjustments made during factory test (VFUSE).

Provide additional isolation of +1.8V with a ferrite bead to pin1 (CLKVDD). Make sure the decoupling cap for this pin is placed as close as possible to the pin and the connection made to the power and GND plane is made with thick trace and several vias. Place this cap on the component side if possible. This is the 1.8V supply to the clock receiver, PLL and clock buffer circuits. When the PLL is used, it is best to keep pin 1 separate from everything else, for clock mixing and SNR reasons.

Provide additional isolation of +1.8V with a ferrite bead to pins 10 and 39 if possible. These are the 1.8V supplies to the digital processing block (interpolation, coarse mixer, FIFO, etc) as well as the input LVDS receivers and DLL circuit (DIG DVDD). The logic section is an 8 way, skewed clock, poly-phase implementation. There supply current transients are therefore DACCLK/2, DACCLK/4 and DACCLK/8 impulses. For clock mixing reasons, the digital section (pins 10 and 39) should be separated from the clock and DAC 1.8V sections due to the CMOS logic switching.

In a situation where the PLL is not being used, we would suggest that just 2 separate filtered 1.8V supplies could be used. One for pins 10 and 39 (DIG DVDD), and the other for the remaining pins 50, 63, 1 and 44 (CLKVDD, DAC DVDD and VFUSE).

Use the power pad info from the DAC5682 power pad drawing for generating the board stencil for the area under the DAC5682. It is very critical that this power pad makes a good electrical contact to the board power plane as most of the device GND connection is made through this path.

9.4.5.2 LVDS DAC Interface

All LVDS inputs including the DACSYNC should be routed as 100 Ω differential pairs going to the DAC. These signals should have the same trace length as the DCLK signals, which also should be routed as 100 Ω differential. Attempt to make the difference between trace lengths of each leg of the individual pairs (P & N) no more than 3 mils. Attempt to make the difference between trace lengths of pairs no more than 5 mils. Since these are LVDS signals, the overall length is not as critical as keeping all of these traces roughly the same length.

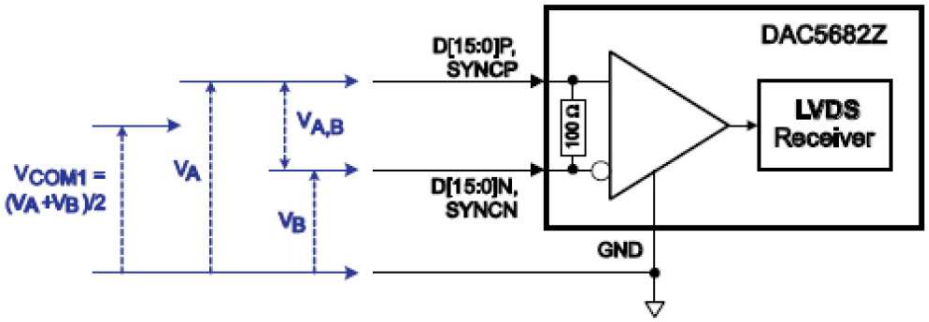

Figure 9.10: DAC5682Z LVDS Inputs.

9.4.5.3 General PCB Layout Guidelines

By using a single solid GND plane, the routing of signals on the top and bottom layers will keep the impedance constant as long as there are no breaks in the GND plane below the signal. Same holds for inner layer differential traces as long as there are no breaks in the GND planes above and below the signal.

Try to keep High level signals ($>$ 0dBm) away from any low level signals ($<$ 0 dBm) as much as possible.

Use pads inside decoupling vias to minimize the trace length between the component and power/GND planes. Fill the vias with non-conductive epoxy to prevent the solder paste from flowing into these holes during assembly.

Care must be used when installing the DAC5682 and DAC5688 power pads to the pcb. Use the DAC5682 power pad.pdf and DAC5688 Data Sheet for instructions regarding generating the proper stencil to be used with the DAC5682 power pad.

Route high speed differential lines on internal layers for better noise suppression. These signals must have unbroken GND planes above and below them to maintain the proper impedance.

Create small power planes between IC power pins and decoupling caps instead of traces when there are several caps and power input pins in close proximity. Use as many vias as possible to connect this plane to the internal power plane.

Use the smallest package decoupling capacitors possible (402 footprint) to provide the lowest inductance possible.

Lay power layers adjacent to ground layers. Connect the ground layers with numerous vias.

9.4.6 THS4509 Routing Constraints

It is recommended to follow the layout of the external components near the amplifier, ground plane construction, and power routing of the EVM as closely as possible [8]. General guidelines are:

1. Signal routing should be direct and as short as possible into and out of the opamp circuit.
2. The feedback path should be short and direct avoiding vias.
3. Ground or power planes should be removed from directly under the amplifier's input and output pins.
4. An output resistor is recommended on each output, as near to the output pin as possible.
5. Two 10μF and two 0.1μF power-supply decoupling capacitors should be placed as near to the power-supply pins as possible.
6. Two 0.1μF capacitors should be placed between the CM input pins and ground. This limits noise coupled into the pins. One each should be placed to ground near pin 4 and pin 9.
7. It is recommended to split the ground pane on layer 2 (L2) as shown below and to use a solid ground on layer 3 (L3). A single-point connection should be used between each split section on L2 and L3.
8. A single-point connection to ground on L2 is recommended for the input termination resistors R1 and R2. This should be applied to the input gain resistors if termination is not used.
9. The THS4509 recommended PCB footprint is shown in Figure 9.11.

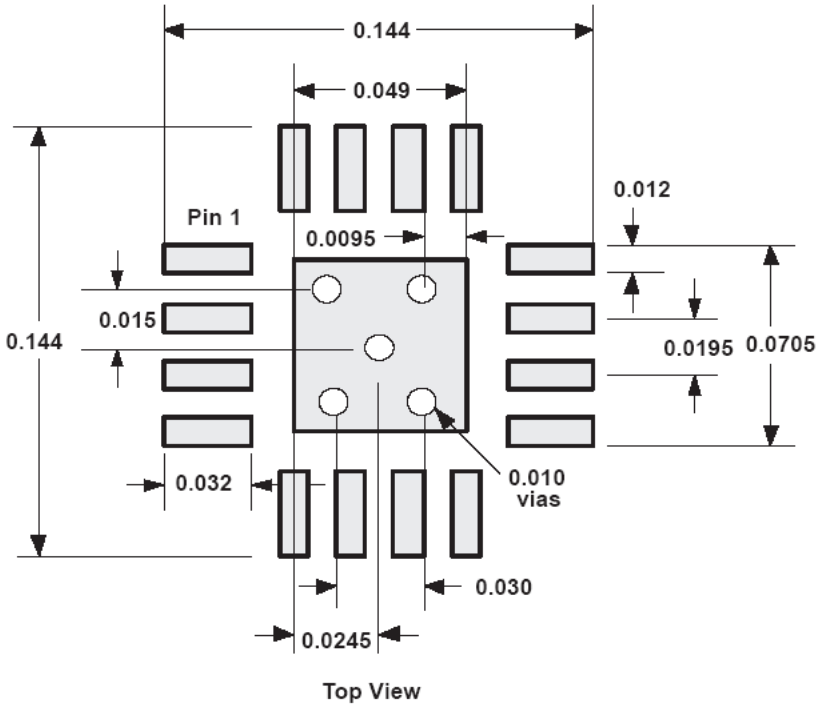

Figure 9.11: QFN Etch and Via Pattern.

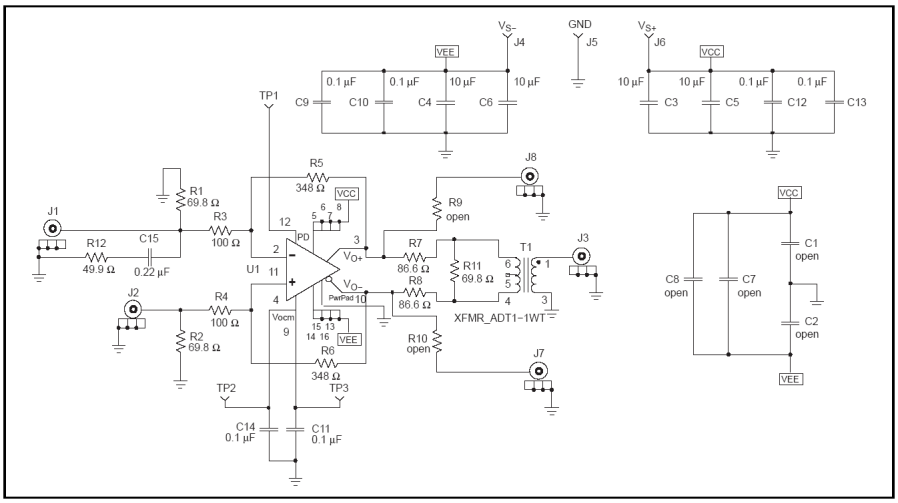

Figure 9.12: THS4509 EVM Schematic.

9.4.7 THS4302 Routing Constraints

Achieving optimum performance with a high-frequency amplifier like the THS4302 requires careful attention to board layout parasitics and external component types [7].

Recommendations that optimize performance include:

1. **Minimize parasitic capacitance to any AC Ground for all of the signal I/O pins.** However, if using a transmission line at the I/O, then place the matching resistor as close to the part as possible. Except for when transmission lines are used, parasitic capacitance on the output and the noninverting input pins can react with the load and source impedances to cause unintentional band limiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground planes and power planes should be unbroken elsewhere on the board, and terminated as described in Section 8.1.

2. **Minimize the distance ($<$ 0.25") from the power supply pins to high frequency 0.1μF decoupling capacitors.** At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Note that each millimeter of a line, that is narrow relative to its length, has $\sim$0.8nH of inductance. The power supply connections should always be decoupled with the recommended capacitors. If not properly decoupled, distortion performance is degraded. Large (6.8μF to 22μF) decoupling capacitors, effective at lower frequency, should also be used on the main supply lines, preferably decoupled from the amplifier and mid- and high-frequency capacitors by a ferrite bead. See Section 8.1. The larger caps may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board. A very low inductance path should be used to connect the inverting pin of the amplifier to ground. A minimum of 5 vias as close to the part as possible is recommended.

3. **Careful selection and placement of external components preserves the high frequency performance of the THS4302.** Resistors should be a low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Keep PC board trace length as short as possible.

4. **Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines.** For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_{ISO} from the plot of recommended R_{ISO} vs. Capacitive Load. Low parasitic capacitve loads ($<$4pF) may not need an R_{ISO} because THS4302 amplifiers are nominally compensated to operate with a 2pF parasitic load. Higher parasitic capacitive loads without an R_{ISO} are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance

transmission line using microstrip or stripline techniques. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the THS4302 is used as well as terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device: this total effective impedance should be set to match the trace impedance. If the 6dB attenuation of a doubly terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treet the trace as a capacitive load in this case, and set the series resistor value as shown in the plot of R_{ISO} vs Capacitive Load. This does not preserve signal integrity as well as a doubly terminated line. If the input impedance of the destination device is low, there is some signal attenuation due to the voltage divider formed by the series output into the terminating impedance. A 50Ω environment is normally not necessary on board as long as the lead lengths are short, and in fact, a highter impedance environment improves distortion as shown in the distortion versus load plots.

Although there are many ways to properly heatsink the PowerPAD package, the following steps illustrate the recommended approach.

1. Prepare the PCB with a top side etch pattern as shown in Figure 9.13. There should be etch for the leads as well as etch for the thermal pad.

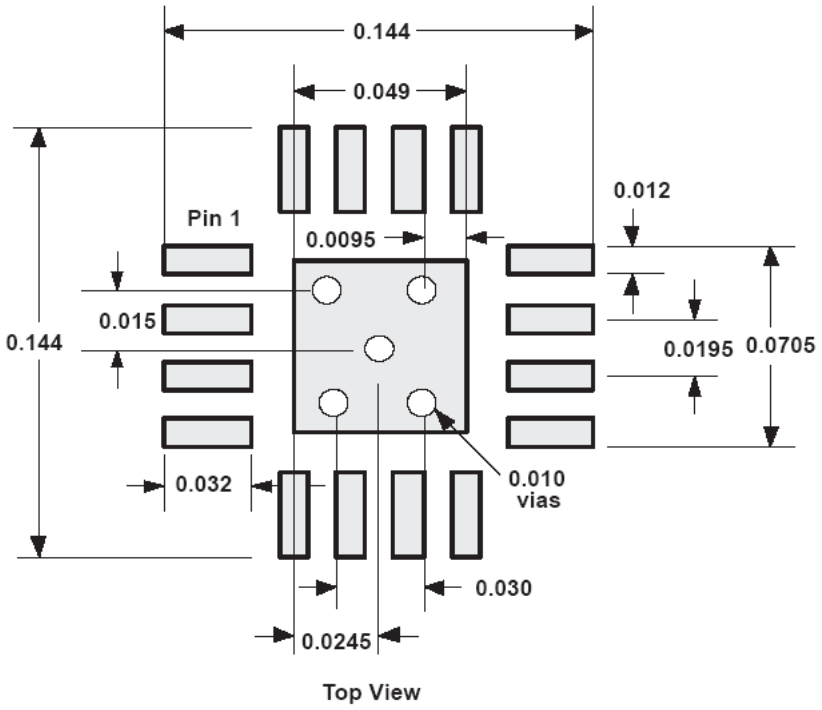

Figure 9.13: PowerPAD PCB Etch and Via Pattern.

2. Place five holes in the area of the thermal pad. The holes should be 13 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.

3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. They help dissipate the heat generated by the IC. These additional vias may be larger than the 13 mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered, so that wicking is not a problem.

4. Connect all holes to the internal ground plane.

5. When connecting these holes to the ground plane, **do not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for showing the heat transfer during soldering operations. This resistance makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the IC PowerPAD package should make their connection to the internal ground plane, with a complete connection around the entire circumference of the plated-through hole. See Figure 9.7.

6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.

7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.

8. With these preparatory steps in place, the IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

9.4.8 OPA695 Routing Constraints

1. **Minimize parasitic capacitance to any AC Ground for all of the signal I/O pins.** Parasitic capacitance on the output and the noninverting input pins can cause instability; on the non-inverting input, it can react with the source impedance to cause unintentional band limiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground planes and power planes should be unbroken elsewhere on the board.

2. **Minimize the distance ($<$ 0.25") from the power supply pins to high frequency 0.1μF decoupling capacitors.** At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power supply connections should always be decoupled with these capacitors. An optional supply-decoupling capacitor across the two power supplies (for bipolar operation) will improve 2nd-harmonic distortion performance. Larger (2.2μF to 6.8μF) decoupling capacitors, effective at a lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

3. **Careful selection and placement of external components will preserve the high frequency performance of the OPA695.** Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Keep PC board trace length as short as possible.

4. **Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines.** For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of *Recommended R_S vs. Capacitive Load*. Low parasitic capacitve loads ($<$5pF) may not need an R_S since the OPA695 is nominally compensated to operate with a 2pF parasitic load. If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques. With a characteristic board trace impedance defined (based on board material and trace dimensions), a matching series resistor into the trace from the output of the OPA695 is used. A terminating shunt resistor at the input of the destination device is used as well. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. If the 6dB attenuation of a doubly terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treet the trace as a capacitive load in this case, and set the series resistor value as shown in the plot of *R_S vs Capacitive Load*. This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance [9].

9.4.9 AD9516 and VCO Routing Constraints

1. Place the 200Ω shunt resistors and series 100pF close to the AD9516 IC.
2. Place the LVPECL bias network for the FPGA_ASAP_CLK_[P|N] and FPGA_DSP_CLK_[P|N] as close as possible to the FPGA.

9.4.10 10MHz Reference Circuit Routing Constraints

Routing stuff goes here.

9.4.11 Anti-Alias Filter Routing Constraints

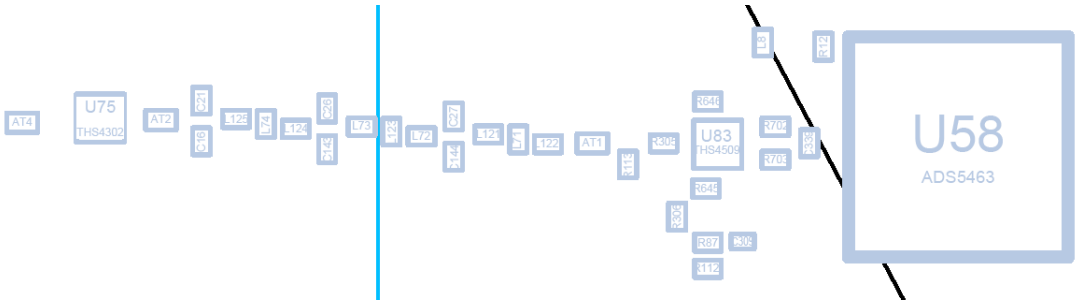

Figure 9.14: Anti-Alias Filter Recommended Placement.

9.4.12 Anti-Image Filter Routing Constraints

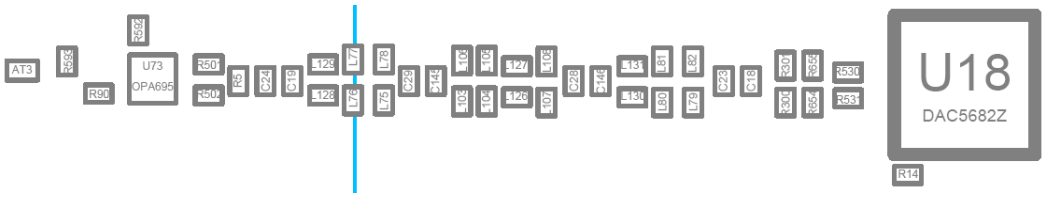

Figure 9.15: Anti-Image Filter Recommended Placement.

9.4.13 AsAP Routing Constraints

- Match lengths of the following nets within 500 mils:
  - FPGA_ASAP1_DATA_IN[15:0]
  - FPGA_ASAP1_CLK_IN
  - FPGA_ASAP1_REQ_IN
  - FPGA_ASAP1_VLD_IN
- Match lengths of the following nets within 500 mils:
  - FPGA_ASAP1_DATA_OUT[15:0]
  - FPGA_ASAP1_CLK_OUT
  - FPGA_ASAP1_REQ_OUT
  - FPGA_ASAP1_VLD_OUT
- Match lengths of the following nets within 500 mils:
  - FPGA_ASAP2_DATA_IN[15:0]
  - FPGA_ASAP2_CLK_IN
  - FPGA_ASAP2_REQ_IN
  - FPGA_ASAP2_VLD_IN
- Match lengths of the following nets within 500 mils:
  - FPGA_ASAP2_DATA_OUT[15:0]
  - FPGA_ASAP2_CLK_OUT
  - FPGA_ASAP2_REQ_OUT
  - FPGA_ASAP2_VLD_OUT

9.5 Net Types

The Net Types used on this PC board are shown in Table **??**. The net assignments to those Net Types are shown in Table 9.7.

For example, the trace lengths of the QDR II memory device input signals (QDR_K, QDR_K_n, QDR_W_n, QDR_R_n, QDR_SA, QDR_BW_n, and QDR_D) must be well matched to present

Table 9.6: PC Board Net Types

Net Type Name	Inner Outer	Trace Width	Trace Separation	Trace Impedance	Notes
POWER_15MIL		15 mils	N/A	N/A	
POWER_25MIL		25 mils	N/A	N/A	
POWER_50MIL		50 mils	N/A	N/A	
DEFAULT	INNER/OUTER	8 mils	N/A	N/A	1. Default analog trace width.
FPGA	INNER/OUTER	4 mils	N/A	N/A	1. Default FPGA trace width.
FPGA_DIFF	INNER	4 mils	4 mils	100 Ω	1. No area fill on adjacent layer.
	OUTER	10 mils	6 mils	100 Ω	
QDRII_SRAM_SE	INNER	7 mils	N/A	50 Ω	1. Match lengths (See Section 9.4.3). 2. No area fill on adjacent layer.
	OUTER	15 mils	N/A	50 Ω	1. Match lengths (See Section 9.4.3).
QDRII_SRAM_DIFF	INNER	4 mils	4 mils	100 Ω	1. Match lengths (See Section 9.4.3). 2. No area fill on adjacent layer.
	OUTER	10 mils	6 mils	100 Ω	1. Match lengths (See Section 9.4.3).
DDR2_SDRAM_SE	INNER	7 mils	N/A	50 Ω	1. Match lengths (See Section 9.4.2). 2. No area fill on adjacent layer.
	OUTER	15 mils	N/A	50 Ω	1. Match lengths (See Section 9.4.2).
DDR2_SDRAM_DIFF	INNER	4 mils	4 mils	100 Ω	1. Match lengths (See Section 9.4.2). 2. No area fill on adjacent layer.
	OUTER	10 mils	6 mils	100 Ω	1. Match lengths (See Section 9.4.2).
DDR_SDRAM_SE	INNER	7 mils	N/A	50 Ω	1. Match lengths (See Section 9.4.1). 2. No area fill on adjacent layer.
	OUTER	15 mils	N/A	50 Ω	1. Match lengths (See Section 9.4.1).
DDR_SDRAM_DIFF	INNER	4 mils	4 mils	100 Ω	1. Match lengths (See Section 9.4.1). 2. No area fill on adjacent layer.
	OUTER	10 mils	6 mils	100 Ω	1. Match lengths (See Section 9.4.1).
DIGITAL_SE	INNER	7 mils	N/A	50 Ω	1. Match lengths (See Section 9.4.13). 2. No area fill on adjacent layer.
	OUTER	15 mils	N/A	50 Ω	1. Match lengths (See Section 9.4.13).
ADC_DIFF	INNER	4 mils	4 mils	100 Ω	1. Match lengths (DML1). 2. No area fill on adjacent layer.
	OUTER	10 mils	6 mils	100 Ω	1. Match lengths (DML1).

Continued on Next Page...

Net Type Name	Inner Outer	Trace Width	Trace Separation	Trace Impedance	Notes
DAC_DIFF	INNER	4 mils	4 mils	100 Ω	1. Match lengths (DML2). 2. No area fill on adjacent layer.
	OUTER	10 mils	6 mils	100 Ω	1. Match lengths (DML2).
CLOCK_SE	INNER	7 mils	N/A	50 Ω	1. No area fill on adjacent layer.
	OUTER	15 mils	N/A	50 Ω	
CLOCK_DIFF	INNER	4 mils	4 mils	100 Ω	1. No area fill on adjacent layer.
	OUTER	10 mils	6 mils	100 Ω	
ANALOG_SE	INNER	7 mils	N/A	50 Ω	1. No area fill on adjacent layer.
	OUTER	15 mils	N/A	50 Ω	
ANALOG_DIFF	INNER	4 mils	4 mils	100 Ω	1. No area fill on adjacent layer.
	OUTER	10 mils	6 mils	100 Ω	
NO_TRACE		N/A	N/A	N/A	1. No traces allowed.

Table 9.7: Nets assigned to Net Types

Net Name	Net Type (Inner)	Net Type (Outer)
AD9516_1GHZ_VCO_OUT	CLOCK_SE	CLOCK_SE
AD9516_10MHZ_REF_N	CLOCK_DIFF	CLOCK_DIFF
AD9516_10MHZ_REF_P	CLOCK_DIFF	CLOCK_DIFF
AD9516_BYPASS	POWER_15MIL	POWER_15MIL
ADC_IN_N	NO_TRACE	ANALOG_DIFF
ADC_IN_P	NO_TRACE	ANALOG_DIFF
ADC_VREF	POWER_15MIL	POWER_15MIL
AIF_ADC_CLKIN_N	CLOCK_DIFF	CLOCK_DIFF
AIF_ADC_CLKIN_P	CLOCK_DIFF	CLOCK_DIFF
AIF_ADC_CLK_N	CLOCK_DIFF	CLOCK_DIFF
AIF_ADC_CLK_P	CLOCK_DIFF	CLOCK_DIFF
AMC6821_FAN1_A0	DEFAULT	DEFAULT
AMC6821_FAN1_A1	DEFAULT	DEFAULT
AMC6821_FAN1_FAULTN	DEFAULT	DEFAULT
AMC6821_FAN1_OVRN	DEFAULT	DEFAULT
AMC6821_FAN1_THERMN	DEFAULT	DEFAULT
AMC6821_FAN2_A0	DEFAULT	DEFAULT
AMC6821_FAN2_A1	DEFAULT	DEFAULT
AMC6821_FAN2_FAULTN	DEFAULT	DEFAULT
AMC6821_FAN2_OVRN	DEFAULT	DEFAULT
AMC6821_FAN2_THERMN	DEFAULT	DEFAULT
ANLG_INHIBIT	POWER_15MIL	POWER_15MIL
ASAP1_ANLG1	DIGITAL_SE	DIGITAL_SE
ASAP1_ANLG2	DIGITAL_SE	DIGITAL_SE

Continued on Next Page...

Net Name	Net Type (Inner)	Net Type (Outer)
ASAP1_ANLG3	DIGITAL_SE	DIGITAL_SE
ASAP1_ANLG4	DIGITAL_SE	DIGITAL_SE
ASAP1_CFG_CLK	DIGITAL_SE	DIGITAL_SE
ASAP1_CFG_VALID	DIGITAL_SE	DIGITAL_SE
ASAP1_EXT_CLK_IN	DIGITAL_SE	DIGITAL_SE
ASAP1_RESET_COLD	DIGITAL_SE	DIGITAL_SE
ASAP1_RST_CNTCLK	DIGITAL_SE	DIGITAL_SE
ASAP1_SPI_CLK	DIGITAL_SE	DIGITAL_SE
ASAP1_SPI_CSN	DIGITAL_SE	DIGITAL_SE
ASAP1_SPI_LOAD	DIGITAL_SE	DIGITAL_SE
ASAP1_SPI_MISO	DIGITAL_SE	DIGITAL_SE
ASAP1_SPI_MOSI	DIGITAL_SE	DIGITAL_SE
ASAP1_TEST0	DIGITAL_SE	DIGITAL_SE
ASAP1_TEST1	DIGITAL_SE	DIGITAL_SE
ASAP1_TEST2	DIGITAL_SE	DIGITAL_SE
ASAP1_TEST3	DIGITAL_SE	DIGITAL_SE
ASAP1_TEST4	DIGITAL_SE	DIGITAL_SE
ASAP1_TEST5	DIGITAL_SE	DIGITAL_SE
ASAP1_TEST6	DIGITAL_SE	DIGITAL_SE
ASAP1_TEST7	DIGITAL_SE	DIGITAL_SE
ASAP1_TEST8	DIGITAL_SE	DIGITAL_SE
ASAP1_TEST_OUT0	DIGITAL_SE	DIGITAL_SE
ASAP1_TEST_OUT1	DIGITAL_SE	DIGITAL_SE
ASAP1_TEST_OUT2	DIGITAL_SE	DIGITAL_SE
ASAP1_TEST_OUT3	DIGITAL_SE	DIGITAL_SE
ASAP1_TEST_OUT4	DIGITAL_SE	DIGITAL_SE
ASAP1_TEST_OUT5	DIGITAL_SE	DIGITAL_SE
ASAP1_TEST_OUT6	DIGITAL_SE	DIGITAL_SE
ASAP1_TEST_OUT7	DIGITAL_SE	DIGITAL_SE
ASAP1_TEST_OUT8	DIGITAL_SE	DIGITAL_SE
ASAP2_ANLG1	DIGITAL_SE	DIGITAL_SE
ASAP2_ANLG2	DIGITAL_SE	DIGITAL_SE
ASAP2_ANLG3	DIGITAL_SE	DIGITAL_SE
ASAP2_ANLG4	DIGITAL_SE	DIGITAL_SE
ASAP2_CFG_CLK	DIGITAL_SE	DIGITAL_SE
ASAP2_CFG_VALID	DIGITAL_SE	DIGITAL_SE
ASAP2_EXT_CLK_IN	DIGITAL_SE	DIGITAL_SE
ASAP2_RESET_COLD	DIGITAL_SE	DIGITAL_SE
ASAP2_RST_CNTCLK	DIGITAL_SE	DIGITAL_SE
ASAP2_SPI_CLK	DIGITAL_SE	DIGITAL_SE
ASAP2_SPI_CSN	DIGITAL_SE	DIGITAL_SE
ASAP2_SPI_LOAD	DIGITAL_SE	DIGITAL_SE
ASAP2_SPI_MISO	DIGITAL_SE	DIGITAL_SE
ASAP2_SPI_MOSI	DIGITAL_SE	DIGITAL_SE
ASAP2_TEST0	DIGITAL_SE	DIGITAL_SE
ASAP2_TEST1	DIGITAL_SE	DIGITAL_SE
ASAP2_TEST2	DIGITAL_SE	DIGITAL_SE
ASAP2_TEST3	DIGITAL_SE	DIGITAL_SE
ASAP2_TEST4	DIGITAL_SE	DIGITAL_SE
ASAP2_TEST5	DIGITAL_SE	DIGITAL_SE
ASAP2_TEST6	DIGITAL_SE	DIGITAL_SE
		Continued on Next Page...

Net Name	Net Type (Inner)	Net Type (Outer)
ASAP2_TEST7	DIGITAL_SE	DIGITAL_SE
ASAP2_TEST8	DIGITAL_SE	DIGITAL_SE
ASAP2_TEST_OUT0	DIGITAL_SE	DIGITAL_SE
ASAP2_TEST_OUT1	DIGITAL_SE	DIGITAL_SE
ASAP2_TEST_OUT2	DIGITAL_SE	DIGITAL_SE
ASAP2_TEST_OUT3	DIGITAL_SE	DIGITAL_SE
ASAP2_TEST_OUT4	DIGITAL_SE	DIGITAL_SE
ASAP2_TEST_OUT5	DIGITAL_SE	DIGITAL_SE
ASAP2_TEST_OUT6	DIGITAL_SE	DIGITAL_SE
ASAP2_TEST_OUT7	DIGITAL_SE	DIGITAL_SE
ASAP2_TEST_OUT8	DIGITAL_SE	DIGITAL_SE
ASAP_INHIBIT	POWER_15MIL	POWER_15MIL
ASAP_TRACK_CTRL1	POWER_15MIL	POWER_15MIL
ASAP_TRACK_CTRL_OUT1	POWER_15MIL	POWER_15MIL
ASAP_TRACK_CTRL_OUT2	POWER_15MIL	POWER_15MIL
AUX_IN	NO_TRACE	ANALOG_SE
CLK10MHZ_CPLD	CLOCK_SE	CLOCK_SE
CLK10MHZ_CPLD_OUT	CLOCK_SE	CLOCK_SE
CLK10MHZ_EXT_BUF_N	CLOCK_DIFF	CLOCK_DIFF
CLK10MHZ_EXT_BUF_P	CLOCK_DIFF	CLOCK_DIFF
CLK10MHZ_INT_BUF_N	CLOCK_DIFF	CLOCK_DIFF
CLK10MHZ_INT_BUF_P	CLOCK_DIFF	CLOCK_DIFF
CLK10MHZ_REFOUT_N	CLOCK_DIFF	CLOCK_DIFF
CLK10MHZ_REFOUT_P	CLOCK_DIFF	CLOCK_DIFF
CLK10MHZ_REF_AD9516_N	CLOCK_DIFF	CLOCK_DIFF
CLK10MHZ_REF_AD9516_P	CLOCK_DIFF	CLOCK_DIFF
CLK10MHZ_REF_INT_LVDS_N	CLOCK_DIFF	CLOCK_DIFF
CLK10MHZ_REF_INT_LVDS_P	CLOCK_DIFF	CLOCK_DIFF
CLK10MHZ_REF_N	CLOCK_DIFF	CLOCK_DIFF
CLK10MHZ_REF_P	CLOCK_DIFF	CLOCK_DIFF
CLK10MHZ_REF_OSC	CLOCK_SE	CLOCK_SE
CLK10MHZ_REF_OUT	CLOCK_SE	CLOCK_SE
CPLD_BOARD_RSTN	FPGA	FPGA
CPLD_BUTTON	FPGA	FPGA
CPLD_CLK10MHZ_LVDS_N	CLOCK_DIFF	CLOCK_DIFF
CPLD_CLK10MHZ_LVDS_P	CLOCK_DIFF	CLOCK_DIFF
CPLD_LED	FPGA	FPGA
CPLD_TCK	FPGA	FPGA
CPLD_TDI	FPGA	FPGA
CPLD_TDO	FPGA	FPGA
CPLD_TMS	FPGA	FPGA
CUST_CCLK	CLOCK_SE	CLOCK_SE
CUST_CFG_DONE	FPGA	FPGA
CUST_INIT_B	FPGA	FPGA
CUST_PROG_B	FPGA	FPGA
CUST_TCK	FPGA	FPGA
CUST_TDI	FPGA	FPGA
CUST_TDO	FPGA	FPGA
CUST_TMS	FPGA	FPGA
DAC5682_EXTLO	ANALOG_SE	ANALOG_SE
DAC5682_UNUSED_N	NO_TRACE	ANALOG_DIFF
		Continued on Next Page...

Net Name	Net Type (Inner)	Net Type (Outer)
DAC5682_UNUSED_P	NO_TRACE	ANALOG_DIFF
DAC_SS_N	NO_TRACE	ANALOG_DIFF
DAC_SS_P	NO_TRACE	ANALOG_DIFF
DDR_SDRAM_ADDR0	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_ADDR1	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_ADDR2	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_ADDR3	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_ADDR4	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_ADDR5	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_ADDR6	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_ADDR7	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_ADDR8	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_ADDR9	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_ADDR10	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_ADDR11	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_ADDR12	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_BA0	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_BA1	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_CASN	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_CKE	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_CLK_N	DDR_SDRAM_DIFF	DDR_SDRAM_DIF
DDR_SDRAM_CLK_P	DDR_SDRAM_DIFF	DDR_SDRAM_DIF
DDR_SDRAM_CSN	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_DATA0	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_DATA1	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_DATA2	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_DATA3	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_DATA4	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_DATA5	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_DATA6	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_DATA7	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_DATA8	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_DATA9	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_DATA10	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_DATA11	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_DATA12	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_DATA13	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_DATA14	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_DATA15	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_LDM	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_LDQS	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_RASN	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_UDM	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_UDQS	DDR_SDRAM_SE	DDR_SDRAM_SE
DDR_SDRAM_WEN	DDR_SDRAM_SE	DDR_SDRAM_SE
DIG2_INHIBIT	POWER_15MIL	POWER_15MIL
DIG_INHIBIT	POWER_15MIL	POWER_15MIL
EXT_CLK10MHZ_REF	NO_TRACE	CLOCK_SE
EXT_CLK10MHZ_REFOUT	NO_TRACE	CLOCK_SE
FAN1_TACH	POWER_15MIL	POWER_15MIL
FAN2_TACH	POWER_15MIL	POWER_15MIL

Continued on Next Page...

Net Name	Net Type (Inner)	Net Type (Outer)
FIFO_USB_N	ANALOG_DIFF	ANALOG_DIFF
FIFO_USB_P	ANALOG_DIFF	ANALOG_DIFF
FOX_10MHZ_REF	NO_TRACE	CLOCK_SE
FPGA_AD9516_CSB	FPGA	FPGA
FPGA_AD9516_LD	FPGA	FPGA
FPGA_AD9516_PD	FPGA	FPGA
FPGA_AD9516_REFMON	FPGA	FPGA
FPGA_AD9516_REF_SEL	FPGA	FPGA
FPGA_AD9516_RESET	FPGA	FPGA
FPGA_AD9516_SCLK	FPGA	FPGA
FPGA_AD9516_SDIO	FPGA	FPGA
FPGA_AD9516_SDO	FPGA	FPGA
FPGA_AD9516_STATUS	FPGA	FPGA
FPGA_AD9516_SYNC	FPGA	FPGA
FPGA_ADC_DATA_N0	ADC_DIFF	ADC_DIFF
FPGA_ADC_DATA_N1	ADC_DIFF	ADC_DIFF
FPGA_ADC_DATA_N2	ADC_DIFF	ADC_DIFF
FPGA_ADC_DATA_N3	ADC_DIFF	ADC_DIFF
FPGA_ADC_DATA_N4	ADC_DIFF	ADC_DIFF
FPGA_ADC_DATA_N5	ADC_DIFF	ADC_DIFF
FPGA_ADC_DATA_N6	ADC_DIFF	ADC_DIFF
FPGA_ADC_DATA_N7	ADC_DIFF	ADC_DIFF
FPGA_ADC_DATA_N8	ADC_DIFF	ADC_DIFF
FPGA_ADC_DATA_N9	ADC_DIFF	ADC_DIFF
FPGA_ADC_DATA_N10	ADC_DIFF	ADC_DIFF
FPGA_ADC_DATA_N11	ADC_DIFF	ADC_DIFF
FPGA_ADC_DATA_N12	ADC_DIFF	ADC_DIFF
FPGA_ADC_DATA_N13	ADC_DIFF	ADC_DIFF
FPGA_ADC_DATA_N14	ADC_DIFF	ADC_DIFF
FPGA_ADC_DATA_N15	ADC_DIFF	ADC_DIFF
FPGA_ADC_DATA_P0	ADC_DIFF	ADC_DIFF
FPGA_ADC_DATA_P1	ADC_DIFF	ADC_DIFF
FPGA_ADC_DATA_P2	ADC_DIFF	ADC_DIFF
FPGA_ADC_DATA_P3	ADC_DIFF	ADC_DIFF
FPGA_ADC_DATA_P4	ADC_DIFF	ADC_DIFF
FPGA_ADC_DATA_P5	ADC_DIFF	ADC_DIFF
FPGA_ADC_DATA_P6	ADC_DIFF	ADC_DIFF
FPGA_ADC_DATA_P7	ADC_DIFF	ADC_DIFF
FPGA_ADC_DATA_P8	ADC_DIFF	ADC_DIFF
FPGA_ADC_DATA_P9	ADC_DIFF	ADC_DIFF
FPGA_ADC_DATA_P10	ADC_DIFF	ADC_DIFF
FPGA_ADC_DATA_P11	ADC_DIFF	ADC_DIFF
FPGA_ADC_DATA_P12	ADC_DIFF	ADC_DIFF
FPGA_ADC_DATA_P13	ADC_DIFF	ADC_DIFF
FPGA_ADC_DATA_P14	ADC_DIFF	ADC_DIFF
FPGA_ADC_DATA_P15	ADC_DIFF	ADC_DIFF
FPGA_ADC_DATA_RDY_N	ADC_DIFF	ADC_DIFF
FPGA_ADC_DATA_RDY_P	ADC_DIFF	ADC_DIFF
FPGA_ADC_OVR_N	ADC_DIFF	ADC_DIFF
FPGA_ADC_OVR_P	ADC_DIFF	ADC_DIFF
FPGA_AMC6821_FAN1_FAULTN	FPGA	FPGA

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Net Name	Net Type (Inner)	Net Type (Outer)
FPGA_AMC6821_FAN1_OVRN	FPGA	FPGA
FPGA_AMC6821_FAN1_SCK	FPGA	FPGA
FPGA_AMC6821_FAN1_SDA	FPGA	FPGA
FPGA_AMC6821_FAN1_SMBALERTN	FPGA	FPGA
FPGA_AMC6821_FAN1_THERMN	FPGA	FPGA
FPGA_AMC6821_FAN2_FAULTN	FPGA	FPGA
FPGA_AMC6821_FAN2_OVRN	FPGA	FPGA
FPGA_AMC6821_FAN2_SCK	FPGA	FPGA
FPGA_AMC6821_FAN2_SDA	FPGA	FPGA
FPGA_AMC6821_FAN2_SMBALERTN	FPGA	FPGA
FPGA_AMC6821_FAN2_THERMN	FPGA	FPGA
FPGA_ASAP1_CFG_CLK	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_CFG_VALID	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_CLK_IN	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_CLK_OUT	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_DATA_IN0	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_DATA_IN1	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_DATA_IN2	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_DATA_IN3	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_DATA_IN4	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_DATA_IN5	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_DATA_IN6	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_DATA_IN7	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_DATA_IN8	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_DATA_IN9	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_DATA_IN10	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_DATA_IN11	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_DATA_IN12	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_DATA_IN13	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_DATA_IN14	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_DATA_IN15	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_DATA_OUT0	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_DATA_OUT1	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_DATA_OUT2	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_DATA_OUT3	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_DATA_OUT4	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_DATA_OUT5	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_DATA_OUT6	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_DATA_OUT7	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_DATA_OUT8	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_DATA_OUT9	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_DATA_OUT10	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_DATA_OUT11	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_DATA_OUT12	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_DATA_OUT13	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_DATA_OUT14	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_DATA_OUT15	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_MISO	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_MOSI	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_REQ_IN	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_REQ_OUT	DIGITAL_SE	DIGITAL_SE
		Continued on Next Page...

Net Name	Net Type (Inner)	Net Type (Outer)
FPGA_ASAP1_RESET_COLD	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_RST_CNTCLK	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_SPI_CLK	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_SPI_CSN	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_SPI_LOAD	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_VLD_IN	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP1_VLD_OUT	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_CFG_CLK	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_CFG_VALID	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_CLK_IN	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_CLK_OUT	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_DATA_IN0	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_DATA_IN1	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_DATA_IN2	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_DATA_IN3	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_DATA_IN4	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_DATA_IN5	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_DATA_IN6	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_DATA_IN7	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_DATA_IN8	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_DATA_IN9	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_DATA_IN10	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_DATA_IN11	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_DATA_IN12	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_DATA_IN13	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_DATA_IN14	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_DATA_IN15	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_DATA_OUT0	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_DATA_OUT1	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_DATA_OUT2	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_DATA_OUT3	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_DATA_OUT4	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_DATA_OUT5	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_DATA_OUT6	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_DATA_OUT7	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_DATA_OUT8	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_DATA_OUT9	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_DATA_OUT10	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_DATA_OUT11	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_DATA_OUT12	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_DATA_OUT13	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_DATA_OUT14	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_DATA_OUT15	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_MISO	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_MOSI	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_REQ_IN	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_REQ_OUT	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_RESET_COLD	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_RST_CNTCLK	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_SPI_CLK	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_SPI_CSN	DIGITAL_SE	DIGITAL_SE
		Continued on Next Page...

Net Name	Net Type (Inner)	Net Type (Outer)
FPGA_ASAP2_SPI_LOAD	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_VLD_IN	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP2_VLD_OUT	DIGITAL_SE	DIGITAL_SE
FPGA_ASAP_CLKIN_N	CLOCK_DIFF	CLOCK_DIFF
FPGA_ASAP_CLKIN_P	CLOCK_DIFF	CLOCK_DIFF
FPGA_ASAP_CLK_N	CLOCK_DIFF	CLOCK_DIFF
FPGA_ASAP_CLK_P	CLOCK_DIFF	CLOCK_DIFF
FPGA_AUX_IN_N	FPGA_DIFF	FPGA_DIFF
FPGA_AUX_IN_P	FPGA_DIFF	FPGA_DIFF
FPGA_BANK3_VRN	POWER_15MIL	POWER_15MIL
FPGA_BANK3_VRP	POWER_15MIL	POWER_15MIL
FPGA_BANK11_VRN	POWER_15MIL	POWER_15MIL
FPGA_BANK11_VRP	POWER_15MIL	POWER_15MIL
FPGA_BANK12_VRN	POWER_15MIL	POWER_15MIL
FPGA_BANK12_VRP	POWER_15MIL	POWER_15MIL
FPGA_BANK15_VRN	POWER_15MIL	POWER_15MIL
FPGA_BANK15_VRP	POWER_15MIL	POWER_15MIL
FPGA_BANK19_VRN	POWER_15MIL	POWER_15MIL
FPGA_BANK19_VRP	POWER_15MIL	POWER_15MIL
FPGA_BANK20_VRN	POWER_15MIL	POWER_15MIL
FPGA_BANK20_VRP	POWER_15MIL	POWER_15MIL
FPGA_BANK21_VRN	POWER_15MIL	POWER_15MIL
FPGA_BANK21_VRP	POWER_15MIL	POWER_15MIL
FPGA_BOARD_RSTN	FPGA	FPGA
FPGA_CCLK	CLOCK_SE	CLOCK_SE
FPGA_CLK10MHZ_REF_CTRL0	FPGA	FPGA
FPGA_CLK10MHZ_REF_CTRL1	FPGA	FPGA
FPGA_CLK10MHZ_REF_CTRL2	FPGA	FPGA
FPGA_CLK10MHZ_REF_CTRL3	FPGA	FPGA
FPGA_CLK100MHZ_N	CLOCK_DIFF	CLOCK_DIFF
FPGA_CLK100MHZ_P	CLOCK_DIFF	CLOCK_DIFF
FPGA_CONFIG_DONE	FPGA	FPGA
FPGA_CS_B	FPGA	FPGA
FPGA_DAC5682_RSTB	FPGA	FPGA
FPGA_DAC5682_SCLK	FPGA	FPGA
FPGA_DAC5682_SDENB	FPGA	FPGA
FPGA_DAC5682_SDIO	FPGA	FPGA
FPGA_DAC5682_SDO	FPGA	FPGA
FPGA_DAC_CLK_N	CLOCK_DIFF	CLOCK_DIFF
FPGA_DAC_CLK_P	CLOCK_DIFF	CLOCK_DIFF
FPGA_DAC_DATA_N0	DAC_DIFF	DAC_DIFF
FPGA_DAC_DATA_N1	DAC_DIFF	DAC_DIFF
FPGA_DAC_DATA_N2	DAC_DIFF	DAC_DIFF
FPGA_DAC_DATA_N3	DAC_DIFF	DAC_DIFF
FPGA_DAC_DATA_N4	DAC_DIFF	DAC_DIFF
FPGA_DAC_DATA_N5	DAC_DIFF	DAC_DIFF
FPGA_DAC_DATA_N6	DAC_DIFF	DAC_DIFF
FPGA_DAC_DATA_N7	DAC_DIFF	DAC_DIFF
FPGA_DAC_DATA_N8	DAC_DIFF	DAC_DIFF
FPGA_DAC_DATA_N9	DAC_DIFF	DAC_DIFF
FPGA_DAC_DATA_N10	DAC_DIFF	DAC_DIFF

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Net Name	Net Type (Inner)	Net Type (Outer)
FPGA_DAC_DATA_N11	DAC_DIFF	DAC_DIFF
FPGA_DAC_DATA_N12	DAC_DIFF	DAC_DIFF
FPGA_DAC_DATA_N13	DAC_DIFF	DAC_DIFF
FPGA_DAC_DATA_N14	DAC_DIFF	DAC_DIFF
FPGA_DAC_DATA_N15	DAC_DIFF	DAC_DIFF
FPGA_DAC_DATA_P0	DAC_DIFF	DAC_DIFF
FPGA_DAC_DATA_P1	DAC_DIFF	DAC_DIFF
FPGA_DAC_DATA_P2	DAC_DIFF	DAC_DIFF
FPGA_DAC_DATA_P3	DAC_DIFF	DAC_DIFF
FPGA_DAC_DATA_P4	DAC_DIFF	DAC_DIFF
FPGA_DAC_DATA_P5	DAC_DIFF	DAC_DIFF
FPGA_DAC_DATA_P6	DAC_DIFF	DAC_DIFF
FPGA_DAC_DATA_P7	DAC_DIFF	DAC_DIFF
FPGA_DAC_DATA_P8	DAC_DIFF	DAC_DIFF
FPGA_DAC_DATA_P9	DAC_DIFF	DAC_DIFF
FPGA_DAC_DATA_P10	DAC_DIFF	DAC_DIFF
FPGA_DAC_DATA_P11	DAC_DIFF	DAC_DIFF
FPGA_DAC_DATA_P12	DAC_DIFF	DAC_DIFF
FPGA_DAC_DATA_P13	DAC_DIFF	DAC_DIFF
FPGA_DAC_DATA_P14	DAC_DIFF	DAC_DIFF
FPGA_DAC_DATA_P15	DAC_DIFF	DAC_DIFF
FPGA_DAC_SYNC_N	DAC_DIFF	DAC_DIFF
FPGA_DAC_SYNC_P	DAC_DIFF	DAC_DIFF
FPGA_DDR2_SDRAM_A0	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_A1	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_A2	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_A3	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_A4	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_A5	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_A6	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_A7	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_A8	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_A9	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_A10	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_A11	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_A12	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_A13	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_A14	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_A15	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_BA0	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_BA1	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_BA2	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_CASN	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_CKE0	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_CKE1	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_CK_N0	DDR2_SDRAM_DIFF	DDR2_SDRAM_DIFF
FPGA_DDR2_SDRAM_CK_N1	DDR2_SDRAM_DIFF	DDR2_SDRAM_DIFF
FPGA_DDR2_SDRAM_CK_P0	DDR2_SDRAM_DIFF	DDR2_SDRAM_DIFF
FPGA_DDR2_SDRAM_CK_P1	DDR2_SDRAM_DIFF	DDR2_SDRAM_DIFF
FPGA_DDR2_SDRAM_DM0	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DM1	DDR2_SDRAM_SE	DDR2_SDRAM_SE

Continued on Next Page...

Net Name	Net Type (Inner)	Net Type (Outer)
FPGA_DDR2_SDRAM_DM2	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DM3	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DM4	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DM5	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DM6	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DM7	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ0	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ1	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ2	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ3	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ4	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ5	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ6	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ7	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ8	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ9	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ10	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ11	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ12	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ13	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ14	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ15	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ16	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ17	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ18	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ19	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ20	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ21	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ22	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ23	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ24	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ25	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ26	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ27	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ28	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ29	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ30	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ31	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ32	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ33	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ34	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ35	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ36	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ37	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ38	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ39	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ40	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ41	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ42	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ43	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ44	DDR2_SDRAM_SE	DDR2_SDRAM_SE
		Continued on Next Page...

Net Name	Net Type (Inner)	Net Type (Outer)
FPGA_DDR2_SDRAM_DQ45	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ46	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ47	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ48	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ49	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ50	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ51	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ52	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ53	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ54	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ55	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ56	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ57	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ58	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ59	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ60	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ61	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ62	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQ63	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_DQS0	DDR2_SDRAM_DIFF	DDR2_SDRAM_DIFF
FPGA_DDR2_SDRAM_DQS1	DDR2_SDRAM_DIFF	DDR2_SDRAM_DIFF
FPGA_DDR2_SDRAM_DQS2	DDR2_SDRAM_DIFF	DDR2_SDRAM_DIFF
FPGA_DDR2_SDRAM_DQS3	DDR2_SDRAM_DIFF	DDR2_SDRAM_DIFF
FPGA_DDR2_SDRAM_DQS4	DDR2_SDRAM_DIFF	DDR2_SDRAM_DIFF
FPGA_DDR2_SDRAM_DQS5	DDR2_SDRAM_DIFF	DDR2_SDRAM_DIFF
FPGA_DDR2_SDRAM_DQS6	DDR2_SDRAM_DIFF	DDR2_SDRAM_DIFF
FPGA_DDR2_SDRAM_DQS7	DDR2_SDRAM_DIFF	DDR2_SDRAM_DIFF
FPGA_DDR2_SDRAM_DQSN_NC0	DDR2_SDRAM_DIFF	DDR2_SDRAM_DIFF
FPGA_DDR2_SDRAM_DQSN_NC1	DDR2_SDRAM_DIFF	DDR2_SDRAM_DIFF
FPGA_DDR2_SDRAM_DQSN_NC2	DDR2_SDRAM_DIFF	DDR2_SDRAM_DIFF
FPGA_DDR2_SDRAM_DQSN_NC3	DDR2_SDRAM_DIFF	DDR2_SDRAM_DIFF
FPGA_DDR2_SDRAM_DQSN_NC4	DDR2_SDRAM_DIFF	DDR2_SDRAM_DIFF
FPGA_DDR2_SDRAM_DQSN_NC5	DDR2_SDRAM_DIFF	DDR2_SDRAM_DIFF
FPGA_DDR2_SDRAM_DQSN_NC6	DDR2_SDRAM_DIFF	DDR2_SDRAM_DIFF
FPGA_DDR2_SDRAM_DQSN_NC7	DDR2_SDRAM_DIFF	DDR2_SDRAM_DIFF
FPGA_DDR2_SDRAM_ODT0	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_ODT1	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_RASN	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_SCL	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_SDA	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_SN0	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_SN1	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR2_SDRAM_WEN	DDR2_SDRAM_SE	DDR2_SDRAM_SE
FPGA_DDR_SDRAM_ADDR0	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_ADDR1	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_ADDR2	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_ADDR3	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_ADDR4	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_ADDR5	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_ADDR6	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_ADDR7	DDR_SDRAM_SE	DDR_SDRAM_SE
		Continued on Next Page...

Net Name	Net Type (Inner)	Net Type (Outer)
FPGA_DDR_SDRAM_ADDR8	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_ADDR9	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_ADDR10	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_ADDR11	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_ADDR12	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_BA0	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_BA1	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_CASN	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_CKE	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_CLKFB	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_CLK_N	DDR_SDRAM_DIFF	DDR_SDRAM_DIFF
FPGA_DDR_SDRAM_CLK_P	DDR_SDRAM_DIFF	DDR_SDRAM_DIFF
FPGA_DDR_SDRAM_CSN	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_DATA0	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_DATA1	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_DATA2	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_DATA3	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_DATA4	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_DATA5	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_DATA6	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_DATA7	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_DATA8	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_DATA9	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_DATA10	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_DATA11	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_DATA12	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_DATA13	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_DATA14	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_DATA15	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_LDM	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_LDQS	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_RASN	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_UDM	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_UDQS	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DDR_SDRAM_WEN	DDR_SDRAM_SE	DDR_SDRAM_SE
FPGA_DP_CTRL_CSN	FPGA	FPGA
FPGA_DP_CTRL_GPIO0	FPGA	FPGA
FPGA_DP_CTRL_GPIO1	FPGA	FPGA
FPGA_DP_CTRL_GPIO2	FPGA	FPGA
FPGA_DP_CTRL_GPIO3	FPGA	FPGA
FPGA_DP_CTRL_GPIO4	FPGA	FPGA
FPGA_DP_CTRL_INTN	FPGA	FPGA
FPGA_DP_CTRL_MISO	FPGA	FPGA
FPGA_DP_CTRL_MOSI	FPGA	FPGA
FPGA_DP_CTRL_RSTN	FPGA	FPGA
FPGA_DP_CTRL_SCK	FPGA	FPGA
FPGA_DSP_CLKIN_N	CLOCK_DIFF	CLOCK_DIFF
FPGA_DSP_CLKIN_P	CLOCK_DIFF	CLOCK_DIFF
FPGA_DSP_CLK_N	CLOCK_DIFF	CLOCK_DIFF
FPGA_DSP_CLK_P	CLOCK_DIFF	CLOCK_DIFF
FPGA_EXT_CLK10MHZ_LOS	FPGA	FPGA
		Continued on Next Page...

Net Name	Net Type (Inner)	Net Type (Outer)
FPGA_EXT_CLK10MHZ_REF_N	CLOCK_DIFF	CLOCK_DIFF
FPGA_EXT_CLK10MHZ_REF_P	CLOCK_DIFF	CLOCK_DIFF
FPGA_FTDI_DATA0	FPGA	FPGA
FPGA_FTDI_DATA1	FPGA	FPGA
FPGA_FTDI_DATA2	FPGA	FPGA
FPGA_FTDI_DATA3	FPGA	FPGA
FPGA_FTDI_DATA4	FPGA	FPGA
FPGA_FTDI_DATA5	FPGA	FPGA
FPGA_FTDI_DATA6	FPGA	FPGA
FPGA_FTDI_DATA7	FPGA	FPGA
FPGA_FTDI_PWRENN	FPGA	FPGA
FPGA_FTDI_RDN	FPGA	FPGA
FPGA_FTDI_RSTOUTN	FPGA	FPGA
FPGA_FTDI_RXFN	FPGA	FPGA
FPGA_FTDI_SI_WU	FPGA	FPGA
FPGA_FTDI_TXEN	FPGA	FPGA
FPGA_FTDI_WRN	FPGA	FPGA
FPGA_HWID0	FPGA	FPGA
FPGA_HWID1	FPGA	FPGA
FPGA_INIT_B	FPGA	FPGA
FPGA_INT_CLK10MHZ_REF_N	CLOCK_DIFF	CLOCK_DIFF
FPGA_INT_CLK10MHZ_REF_P	CLOCK_DIFF	CLOCK_DIFF
FPGA_IODELAY_CLK_N	CLOCK_DIFF	CLOCK_DIFF
FPGA_IODELAY_CLK_P	CLOCK_DIFF	CLOCK_DIFF
FPGA_LA_CLK	FPGA	FPGA
FPGA_LA_DATA0	FPGA	FPGA
FPGA_LA_DATA1	FPGA	FPGA
FPGA_LA_DATA2	FPGA	FPGA
FPGA_LA_DATA3	FPGA	FPGA
FPGA_LA_DATA4	FPGA	FPGA
FPGA_LA_DATA5	FPGA	FPGA
FPGA_LA_DATA6	FPGA	FPGA
FPGA_LA_DATA7	FPGA	FPGA
FPGA_LEDS0	FPGA	FPGA
FPGA_LEDS1	FPGA	FPGA
FPGA_LEDS2	FPGA	FPGA
FPGA_LEDS3	FPGA	FPGA
FPGA_LOCAL_RSTN	FPGA	FPGA
FPGA_PROG_B	FPGA	FPGA
FPGA_PUSHBUTTON0	FPGA	FPGA
FPGA_PUSHBUTTON1	FPGA	FPGA
FPGA_PUSHBUTTON2	FPGA	FPGA
FPGA_RDWR_B	FPGA	FPGA
FPGA_REACH_RX	FPGA	FPGA
FPGA_REACH_TX	FPGA	FPGA
FPGA_RS232_CTS	FPGA	FPGA
FPGA_RS232_RTS	FPGA	FPGA
FPGA_RS232_RX	FPGA	FPGA
FPGA_RS232_TX	FPGA	FPGA
FPGA_S3A_BOARD_RSTN	FPGA	FPGA
FPGA_SDRAM_CLK_N	CLOCK_DIFF	CLOCK_DIFF
		Continued on Next Page...

Net Name	Net Type (Inner)	Net Type (Outer)
FPGA_SDRAM_CLK_P	CLOCK_DIFF	CLOCK_DIFF
FPGA_SD_BUSY_LED	FPGA	FPGA
FPGA_SD_CARD_DETECT	FPGA	FPGA
FPGA_SD_CLK	FPGA	FPGA
FPGA_SD_RXD	FPGA	FPGA
FPGA_SD_TXD	FPGA	FPGA
FPGA_SLOTID0	FPGA	FPGA
FPGA_SLOTID1	FPGA	FPGA
FPGA_SLOTID2	FPGA	FPGA
FPGA_SRAM_ADDR0	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_ADDR1	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_ADDR2	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_ADDR3	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_ADDR4	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_ADDR5	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_ADDR6	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_ADDR7	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_ADDR8	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_ADDR9	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_ADDR10	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_ADDR11	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_ADDR12	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_ADDR13	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_ADDR14	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_ADDR15	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_ADDR16	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_ADDR17	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_BWN0	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_BWN1	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_BWN2	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_BWN3	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_CLK_N	CLOCK_DIFF	CLOCK_DIFF
FPGA_SRAM_CLK_P	CLOCK_DIFF	CLOCK_DIFF
FPGA_SRAM_CQ_CLK_N	QDRII_SRAM_DIFF	QDRII_SRAM_DIFF
FPGA_SRAM_CQ_CLK_P	QDRII_SRAM_DIFF	QDRII_SRAM_DIFF
FPGA_SRAM_C_CLK_N	QDRII_SRAM_DIFF	QDRII_SRAM_DIFF
FPGA_SRAM_C_CLK_P	QDRII_SRAM_DIFF	QDRII_SRAM_DIFF
FPGA_SRAM_K_CLK_N	QDRII_SRAM_DIFF	QDRII_SRAM_DIFF
FPGA_SRAM_K_CLK_P	QDRII_SRAM_DIFF	QDRII_SRAM_DIFF
FPGA_SRAM_RDATA0	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDATA1	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDATA2	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDATA3	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDATA4	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDATA5	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDATA6	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDATA7	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDATA8	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDATA9	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDATA10	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDATA11	QDRII_SRAM_SE	QDRII_SRAM_SE

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Net Name	Net Type (Inner)	Net Type (Outer)
FPGA_SRAM_RDATA12	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDATA13	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDATA14	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDATA15	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDATA16	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDATA17	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDATA18	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDATA19	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDATA20	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDATA21	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDATA22	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDATA23	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDATA24	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDATA25	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDATA26	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDATA27	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDATA28	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDATA29	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDATA30	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDATA31	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDATA32	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDATA33	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDATA34	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDATA35	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_RDN	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA0	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA1	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA2	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA3	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA4	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA5	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA6	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA7	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA8	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA9	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA10	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA11	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA12	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA13	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA14	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA15	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA16	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA17	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA18	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA19	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA20	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA21	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA22	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA23	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA24	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA25	QDRII_SRAM_SE	QDRII_SRAM_SE

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Net Name	Net Type (Inner)	Net Type (Outer)
FPGA_SRAM_WDATA26	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA27	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA28	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA29	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA30	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA31	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA32	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA33	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA34	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WDATA35	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_SRAM_WRN	QDRII_SRAM_SE	QDRII_SRAM_SE
FPGA_TMPSENS_1A_CSN	FPGA	FPGA
FPGA_TMPSENS_1A_MISO	FPGA	FPGA
FPGA_TMPSENS_1A_MOSI	FPGA	FPGA
FPGA_TMPSENS_1A_SCK	FPGA	FPGA
FPGA_TMPSENS_1B_CSN	FPGA	FPGA
FPGA_TMPSENS_1B_MISO	FPGA	FPGA
FPGA_TMPSENS_1B_MOSI	FPGA	FPGA
FPGA_TMPSENS_1B_SCK	FPGA	FPGA
FPGA_TMPSENS_1C_CSN	FPGA	FPGA
FPGA_TMPSENS_1C_MISO	FPGA	FPGA
FPGA_TMPSENS_1C_MOSI	FPGA	FPGA
FPGA_TMPSENS_1C_SCK	FPGA	FPGA
FPGA_TMPSENS_2A_CSN	FPGA	FPGA
FPGA_TMPSENS_2A_MISO	FPGA	FPGA
FPGA_TMPSENS_2A_MOSI	FPGA	FPGA
FPGA_TMPSENS_2A_SCK	FPGA	FPGA
FPGA_TMPSENS_2B_CSN	FPGA	FPGA
FPGA_TMPSENS_2B_MISO	FPGA	FPGA
FPGA_TMPSENS_2B_MOSI	FPGA	FPGA
FPGA_TMPSENS_2B_SCK	FPGA	FPGA
FPGA_TMPSENS_2C_CSN	FPGA	FPGA
FPGA_TMPSENS_2C_MISO	FPGA	FPGA
FPGA_TMPSENS_2C_MOSI	FPGA	FPGA
FPGA_TMPSENS_2C_SCK	FPGA	FPGA
FPGA_TRIG_IN_N	FPGA_DIFF	FPGA_DIFF
FPGA_TRIG_IN_P	FPGA_DIFF	FPGA_DIFF
FPGA_TRIG_OUT_N	FPGA_DIFF	FPGA_DIFF
FPGA_TRIG_OUT_P	FPGA_DIFF	FPGA_DIFF
FPGA_UI_CSN	FPGA	FPGA
FPGA_UI_INTN	FPGA	FPGA
FPGA_UI_MISO	FPGA	FPGA
FPGA_UI_MOSI	FPGA	FPGA
FPGA_UI_PROG0	FPGA	FPGA
FPGA_UI_PROG1	FPGA	FPGA
FPGA_UI_PROG2	FPGA	FPGA
FPGA_UI_RDY	FPGA	FPGA
FPGA_UI_RSTN	FPGA	FPGA
FPGA_UI_SCK	FPGA	FPGA
FPGA_V5_BOARD_RSTN	FPGA	FPGA
FPGA_V5_CLK100MHZ_N	FPGA_DIFF	FPGA_DIFF
		Continued on Next Page...

Net Name	Net Type (Inner)	Net Type (Outer)
FPGA_V5_CLK100MHZ_P	FPGA_DIFF	FPGA_DIFF
FPGA_V5_FTDI_DATA0	FPGA	FPGA
FPGA_V5_FTDI_DATA1	FPGA	FPGA
FPGA_V5_FTDI_DATA2	FPGA	FPGA
FPGA_V5_FTDI_DATA3	FPGA	FPGA
FPGA_V5_FTDI_DATA4	FPGA	FPGA
FPGA_V5_FTDI_DATA5	FPGA	FPGA
FPGA_V5_FTDI_DATA6	FPGA	FPGA
FPGA_V5_FTDI_DATA7	FPGA	FPGA
FPGA_V5_FTDI_PWRENN	FPGA	FPGA
FPGA_V5_FTDI_RDN	FPGA	FPGA
FPGA_V5_FTDI_RSTOUTN	FPGA	FPGA
FPGA_V5_FTDI_RXFN	FPGA	FPGA
FPGA_V5_FTDI_SI_WU	FPGA	FPGA
FPGA_V5_FTDI_TXEN	FPGA	FPGA
FPGA_V5_FTDI_WRN	FPGA	FPGA
FPGA_V5_LA_CLK	FPGA	FPGA
FPGA_V5_LA_DATA0	FPGA	FPGA
FPGA_V5_LA_DATA1	FPGA	FPGA
FPGA_V5_LA_DATA2	FPGA	FPGA
FPGA_V5_LA_DATA3	FPGA	FPGA
FPGA_V5_LA_DATA4	FPGA	FPGA
FPGA_V5_LA_DATA5	FPGA	FPGA
FPGA_V5_LA_DATA6	FPGA	FPGA
FPGA_V5_LA_DATA7	FPGA	FPGA
FPGA_V5_LEDS0	FPGA	FPGA
FPGA_V5_LEDS1	FPGA	FPGA
FPGA_V5_LEDS2	FPGA	FPGA
FPGA_V5_LEDS3	FPGA	FPGA
FPGA_V5_PUSHBUTTON0	FPGA	FPGA
FPGA_V5_PUSHBUTTON1	FPGA	FPGA
FPGA_V5_RS232_CTS	FPGA	FPGA
FPGA_V5_RS232_RTS	FPGA	FPGA
FPGA_V5_RS232_RX	FPGA	FPGA
FPGA_V5_RS232_TX	FPGA	FPGA
FPGA_V5_SD_BUSY_LED	FPGA	FPGA
FPGA_V5_SD_CARD_DETECT	FPGA	FPGA
FPGA_V5_SD_CLK	FPGA	FPGA
FPGA_V5_SD_RXD	FPGA	FPGA
FPGA_V5_SD_TXD	FPGA	FPGA
FP_AUX_IN	ANALOG	ANALOG
FP_TRIG_IN	ANALOG	ANALOG
FTDI_EECS	FPGA	FPGA
FTDI_EESCK	FPGA	FPGA
FTDI_EESDIO	FPGA	FPGA
FTDI_POWER	POWER_25MIL	POWER_25MIL
FTDI_RESETN	FPGA	FPGA
FTDI_USBDM	ANALOG_DIFF	ANALOG_DIFF
FTDI_USBDP	ANALOG_DIFF	ANALOG_DIFF
FTDI_XTAL_IN	CLOCK_SE	CLOCK_SE
FTDI_XTAL_OUT	CLOCK_SE	CLOCK_SE

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Net Name	Net Type (Inner)	Net Type (Outer)
GND	POWER_25MIL	POWER_25MIL
GNDA_FPGA	POWER_15MIL	POWER_15MIL
GND_MAIN	POWER_50MIL	POWER_50MIL
IF_AAF_IN	NO_TRACE	ANALOG_SE
IF_AAF_OUT	NO_TRACE	ANALOG_SE
IF_IN	NO_TRACE	ANALOG_SE
IF_LNA_IN	NO_TRACE	ANALOG_SE
IF_LNA_OUT	NO_TRACE	ANALOG_SE
IF_PREAMP_CM	ANALOG_SE	ANALOG_SE
IF_PREAMP_IN	NO_TRACE	ANALOG_SE
IF_PREAMP_OUT_N	NO_TRACE	ANALOG_DIFF
IF_PREAMP_OUT_P	NO_TRACE	ANALOG_DIFF
JTAG_CCN	FPGA	FPGA
N2V5A_AIF	POWER_25MIL	POWER_25MIL
N2V5A_IFLNA	POWER_25MIL	POWER_25MIL
N5V2AF_AIF	POWER_25MIL	POWER_25MIL
N5V2AF_AIF_IN	POWER_25MIL	POWER_25MIL
N5V2A_AIF	POWER_25MIL	POWER_25MIL
N5V2A_SS	POWER_25MIL	POWER_25MIL
N5V2A_SS_AMPF	POWER_25MIL	POWER_25MIL
N6VA	POWER_25MIL	POWER_25MIL
N6VAF_AIF	POWER_25MIL	POWER_25MIL
N6VAF_AIF_IN	POWER_25MIL	POWER_25MIL
N6VAF_SS	POWER_25MIL	POWER_25MIL
N6VAF_SS_IN	POWER_25MIL	POWER_25MIL
N6VA_OUT	POWER_25MIL	POWER_25MIL
P0V9D_MEM_VREF	POWER_15MIL	POWER_15MIL
P0V9D_SDRAM_VREF	POWER_15MIL	POWER_15MIL
P0V9D_SDRAM_VTT	POWER_15MIL	POWER_15MIL
P0V9D_SRAM_VREF	POWER_15MIL	POWER_15MIL
P0V9D_SRAM_VTT	POWER_15MIL	POWER_15MIL
P0V9D_VREF	POWER_15MIL	POWER_15MIL
P0V9D_VTT	POWER_15MIL	POWER_15MIL
P1V0D	POWER_25MIL	POWER_25MIL
P1V0D_ASAP	POWER_25MIL	POWER_25MIL
P1V0D_V5	POWER_25MIL	POWER_25MIL
P1V2D	POWER_25MIL	POWER_25MIL
P1V2D_S3A	POWER_15MIL	POWER_15MIL
P1V3D_ASAP	POWER_25MIL	POWER_25MIL
P1V8A_SS	POWER_25MIL	POWER_25MIL
P1V8A_SSF	POWER_25MIL	POWER_25MIL
P1V8D	POWER_25MIL	POWER_25MIL
P1V8D_SDRAM	POWER_25MIL	POWER_25MIL
P1V8D_SRAM	POWER_25MIL	POWER_25MIL
P1V8D_V5	POWER_25MIL	POWER_25MIL
P1V25D_DDR_VREF	POWER_15MIL	POWER_15MIL
P1V25D_DDR_VTT	POWER_15MIL	POWER_15MIL
P2V5A	POWER_25MIL	POWER_25MIL
P2V5A_AIF	POWER_25MIL	POWER_25MIL
P2V5A_IFLNA	POWER_25MIL	POWER_25MIL
P2V5A_TRIG	POWER_25MIL	POWER_25MIL

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Net Name	Net Type (Inner)	Net Type (Outer)
P2V5D	POWER_25MIL	POWER_25MIL
P2V5D_10MHZREF	POWER_25MIL	POWER_25MIL
P2V5D_S3A	POWER_25MIL	POWER_25MIL
P2V5D_V5	POWER_25MIL	POWER_25MIL
P2V5F_AUX_IN	POWER_15MIL	POWER_15MIL
P2V5F_TRIG_IN	POWER_15MIL	POWER_15MIL
P2V5F_TRIG_OUT	POWER_15MIL	POWER_15MIL
P2V5REF	POWER_15MIL	POWER_15MIL
P2V5REF_FPGA	POWER_15MIL	POWER_15MIL
P3V3A_10MHZREF	POWER_25MIL	POWER_25MIL
P3V3A_AD9516	POWER_25MIL	POWER_25MIL
P3V3A_ADC	POWER_25MIL	POWER_25MIL
P3V3A_AIF	POWER_25MIL	POWER_25MIL
P3V3A_CLK	POWER_25MIL	POWER_25MIL
P3V3A_CLKDIV	POWER_25MIL	POWER_25MIL
P3V3A_CLKDIVREF	POWER_25MIL	POWER_25MIL
P3V3A_SS	POWER_25MIL	POWER_25MIL
P3V3A_SSF	POWER_25MIL	POWER_25MIL
P3V3D	POWER_25MIL	POWER_25MIL
P3V3D_ADC	POWER_25MIL	POWER_25MIL
P3V3D_AIF	POWER_25MIL	POWER_25MIL
P3V3D_CP2102	POWER_25MIL	POWER_25MIL
P3V3D_CPLD	POWER_25MIL	POWER_25MIL
P3V3D_FAN1	POWER_25MIL	POWER_25MIL
P3V3D_FAN2	POWER_25MIL	POWER_25MIL
P3V3D_REACH	POWER_25MIL	POWER_25MIL
P3V3D_RST	POWER_25MIL	POWER_25MIL
P3V3D_S3A	POWER_25MIL	POWER_25MIL
P3V3D_SD	POWER_25MIL	POWER_25MIL
P3V3D_SDRAM	POWER_25MIL	POWER_25MIL
P3V3D_TPS74201	POWER_25MIL	POWER_25MIL
P3V3D_TRACK_CTRL	POWER_15MIL	POWER_15MIL
P3V3D_TRACK_CTRL_OUT	POWER_15MIL	POWER_15MIL
P3V3D_USB	POWER_25MIL	POWER_25MIL
P3V3D_V5	POWER_15MIL	POWER_15MIL
P3V3D_V5_CP2102	POWER_15MIL	POWER_15MIL
P3V3D_V5_SD	POWER_25MIL	POWER_25MIL
P3V3D_V5_USB	POWER_25MIL	POWER_25MIL
P5V2A	POWER_25MIL	POWER_25MIL
P5V2A_ADC	POWER_25MIL	POWER_25MIL
P5V2A_PREAMP	POWER_25MIL	POWER_25MIL
P5V2A_SS_AMPF	POWER_25MIL	POWER_25MIL
P5V2A_SS_FILT	POWER_25MIL	POWER_25MIL
P5V2A_VCO	POWER_25MIL	POWER_25MIL
P5V5A	POWER_25MIL	POWER_25MIL
P5V5AF	POWER_25MIL	POWER_25MIL
P5V5AF_AIF	POWER_25MIL	POWER_25MIL
P5V5AF_CLK	POWER_25MIL	POWER_25MIL
P5V5AF_CLKDIV	POWER_25MIL	POWER_25MIL
P5V5AF_SS	POWER_25MIL	POWER_25MIL
P5V5AF_THS4302	POWER_25MIL	POWER_25MIL

Continued on Next Page...

Net Name	Net Type (Inner)	Net Type (Outer)
P5V5AF_TRIG	POWER_25MIL	POWER_25MIL
P5V5DF_AIF	POWER_25MIL	POWER_25MIL
P5VA_USB	POWER_25MIL	POWER_25MIL
P5VA_V5_USB	POWER_25MIL	POWER_25MIL
P5VD	POWER_25MIL	POWER_25MIL
P5VD_UI	POWER_25MIL	POWER_25MIL
P5VD_USB	POWER_25MIL	POWER_25MIL
P5VD_V5_USB	POWER_25MIL	POWER_25MIL
P8VAF_VCO	POWER_25MIL	POWER_25MIL
P8VA_CLKDIV	POWER_25MIL	POWER_25MIL
P12VA_TRACK_CTRL1	POWER_15MIL	POWER_15MIL
P12VA_TRACK_CTRL2	POWER_15MIL	POWER_15MIL
P12VD_TRACK_CTRL1	POWER_15MIL	POWER_15MIL
P12VFA	POWER_25MIL	POWER_25MIL
P12VFD	POWER_25MIL	POWER_25MIL
P12VFD_FAN	POWER_25MIL	POWER_25MIL
P12VFD_REACH	POWER_25MIL	POWER_25MIL
P12VF_FAN1	POWER_25MIL	POWER_25MIL
P12VF_FAN2	POWER_25MIL	POWER_25MIL
P12VF_IN	POWER_50MIL	POWER_50MIL
P12V_IN	POWER_50MIL	POWER_50MIL
P12V_MAIN	POWER_50MIL	POWER_50MIL
PTH08T220_SOUT1	CLOCK_SE	CLOCK_SE
PTH08T220_SOUT2	CLOCK_SE	CLOCK_SE
PTH08T220_SOUT3	CLOCK_SE	CLOCK_SE
PTH08T220_SOUT4	CLOCK_SE	CLOCK_SE
PTH08T220_SOUT5	CLOCK_SE	CLOCK_SE
PTH08T220_SOUT6	CLOCK_SE	CLOCK_SE
PTH08T220_SOUT7	CLOCK_SE	CLOCK_SE
PTH08T220_SYNC1	CLOCK_SE	CLOCK_SE
PTH08T220_SYNC2	CLOCK_SE	CLOCK_SE
PTH08T220_SYNC3	CLOCK_SE	CLOCK_SE
PTH08T220_SYNC4	CLOCK_SE	CLOCK_SE
PTH08T220_SYNC5	CLOCK_SE	CLOCK_SE
PTH08T220_SYNC6	CLOCK_SE	CLOCK_SE
PTH08T220_SYNC7	CLOCK_SE	CLOCK_SE
PTH08T260_SOUT8	CLOCK_SE	CLOCK_SE
PTH08T260_SOUT9	CLOCK_SE	CLOCK_SE
PTH08T260_SYNC8	CLOCK_SE	CLOCK_SE
PTH08T260_SYNC9	CLOCK_SE	CLOCK_SE
REACH_RX	FPGA	FPGA
REACH_TX	FPGA	FPGA
S3A_CCLK	CLOCK_SE	CLOCK_SE
S3A_CONFIG_DONE	FPGA	FPGA
S3A_INIT_B	FPGA	FPGA
S3A_M0	FPGA	FPGA
S3A_M1	FPGA	FPGA
S3A_M2	FPGA	FPGA
S3A_PROG_B	FPGA	FPGA
S3A_SPI_CSO	FPGA	FPGA
S3A_SPI_DATA_TO_V5	FPGA	FPGA
		Continued on Next Page...

Net Name	Net Type (Inner)	Net Type (Outer)
S3A_SPI_HOLDN	FPGA	FPGA
S3A_SPI_MISO	FPGA	FPGA
S3A_SPI_MOSI	FPGA	FPGA
S3A_SPI_WPN	FPGA	FPGA
S3A_V0	FPGA	FPGA
S3A_V1	FPGA	FPGA
S3A_V2	FPGA	FPGA
SRAM_DLL_OFFN	FPGA	FPGA
SS_AIF_IN_N	NO_TRACE	ANALOG_DIFF
SS_AIF_IN_P	NO_TRACE	ANALOG_DIFF
SS_AIF_OUT_N	NO_TRACE	ANALOG_DIFF
SS_AIF_OUT_P	NO_TRACE	ANALOG_DIFF
SS_AMP_OUT	NO_TRACE	ANALOG_SE
SS_DAC_CLKIN_N	CLOCK_DIFF	CLOCK_DIFF
SS_DAC_CLKIN_P	CLOCK_DIFF	CLOCK_DIFF
SS_DAC_CLK_N	CLOCK_DIFF	CLOCK_DIFF
SS_DAC_CLK_P	CLOCK_DIFF	CLOCK_DIFF
SS_OUT	NO_TRACE	ANALOG_SE
TCK	FPGA	FPGA
TCK_SRAM	FPGA	FPGA
TDI_SRAM	FPGA	FPGA
TDI_TO_S3A	FPGA	FPGA
TDI_TO_V5	FPGA	FPGA
TDO_SRAM	FPGA	FPGA
TDO_TO_JTAG	FPGA	FPGA
TEST_CLK_N	CLOCK_DIFF	CLOCK_DIFF
TEST_CLK_P	CLOCK_DIFF	CLOCK_DIFF
TMS	FPGA	FPGA
TMS_SRAM	FPGA	FPGA
TOUTN	NO_TRACE	ANALOG_SE
TOUTP	NO_TRACE	ANALOG_SE
TRIG_IN	NO_TRACE	ANALOG_SE
TRIG_OUT	NO_TRACE	ANALOG_SE
UI_CSN	FPGA	FPGA
UI_INTN	FPGA	FPGA
UI_MISO	FPGA	FPGA
UI_MOSI	FPGA	FPGA
UI_PROG0	FPGA	FPGA
UI_PROG1	FPGA	FPGA
UI_PROG2	FPGA	FPGA
UI_RDY	FPGA	FPGA
UI_RSTN	FPGA	FPGA
UI_SCK	FPGA	FPGA
USB_D_N	ANALOG_DIFF	ANALOG_DIFF
USB_D_P	ANALOG_DIFF	ANALOG_DIFF
USB_VBUS	POWER_25MIL	POWER_25MIL
V5_CCLK	CLOCK_SE	CLOCK_SE
V5_CONFIG_DONE	FPGA	FPGA
V5_FIFO_USB_N	ANALOG_DIFF	ANALOG_DIFF
V5_FIFO_USB_P	ANALOG_DIFF	ANALOG_DIFF
V5_FS0	FPGA	FPGA
		Continued on Next Page...

Net Name	Net Type (Inner)	Net Type (Outer)
V5_FS1	FPGA	FPGA
V5_FS2	FPGA	FPGA
V5_FTDI_EECS	FPGA	FPGA
V5_FTDI_EESCK	FPGA	FPGA
V5_FTDI_EESDIO	FPGA	FPGA
V5_FTDI_POWER	POWER_25MIL	POWER_25MIL
V5_FTDI_RESETN	FPGA	FPGA
V5_FTDI_USBDM	ANALOG_DIFF	ANALOG_DIFF
V5_FTDI_USBDP	ANALOG_DIFF	ANALOG_DIFF
V5_FTDI_XTAL_IN	CLOCK_SE	CLOCK_SE
V5_FTDI_XTAL_OUT	CLOCK_SE	CLOCK_SE
V5_HSWAPEN	FPGA	FPGA
V5_INIT_B	FPGA	FPGA
V5_M0	FPGA	FPGA
V5_M1	FPGA	FPGA
V5_M2	FPGA	FPGA
V5_PROG_B	FPGA	FPGA
V5_USB_D_N	ANALOG_DIFF	ANALOG_DIFF
V5_USB_D_P	ANALOG_DIFF	ANALOG_DIFF
V5_USB_VBUS	POWER_25MIL	POWER_25MIL
VDDH_ASAP1	POWER_25MIL	POWER_25MIL
VDDH_ASAP2	POWER_25MIL	POWER_25MIL
VDDIO_ASAP1	POWER_25MIL	POWER_25MIL
VDDIO_ASAP2	POWER_25MIL	POWER_25MIL
VDDL_ASAP1	POWER_25MIL	POWER_25MIL
VDDL_ASAP2	POWER_25MIL	POWER_25MIL
VDDON_ASAP1	POWER_25MIL	POWER_25MIL
VDDON_ASAP2	POWER_25MIL	POWER_25MIL
VDDOSC_ASAP1	POWER_25MIL	POWER_25MIL
VDDOSC_ASAP2	POWER_25MIL	POWER_25MIL
VECTRON_10MHZ_REF	NO_TRACE	CLOCK_SE
VP_VN_SM	FPGA	FPGA

10 SODIMM Interposer Board

The layout footprint for the DDR2 SDRAM SODIMM Socket (U42) used on the Measurement Board was incorrectly drawn. The two rows of pins on the SODIMM socket were too close together. Due to the incorrect dimensions of the SODIMM layout footprint, the SODIMM socket could not be assembled onto the Measurement board. To fix this problem a interposer board was designed with the incorrect footprint on the bottom layer and the correct footprint on the top layer. The assembly top diagram is shown in Figure 10.1.

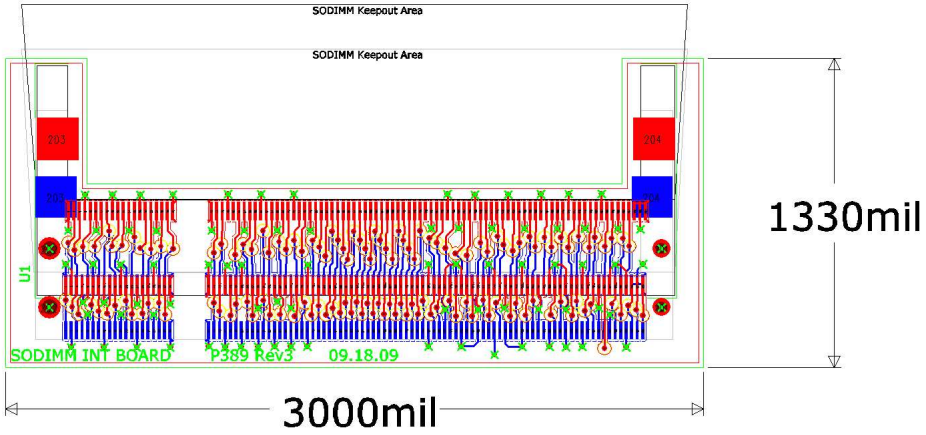

Figure 10.1: SODIMM Interposer Board Assembly Top Diagram.

The SODIMM interposer board is mounted to the Measurement board in a similar fashion to a QFN package. Solder paste is applied to the incorrect footprint on the Measurement board. There are two drill holes on the Measurement board and SODIMM interposer board that are used to properly align the pads. Once the boards are aligned, heat is applied to the area of U42 until the solder has melted, and then the heat is removed. At this point, the board is X-rayed to ensure the SODIMM board is properly aligned and affixed to the Measurement board. The SODIMM socket is then soldered to the SODIMM interposer board.

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