Scalable Hardware-Based Power Management for Many-Core Systems

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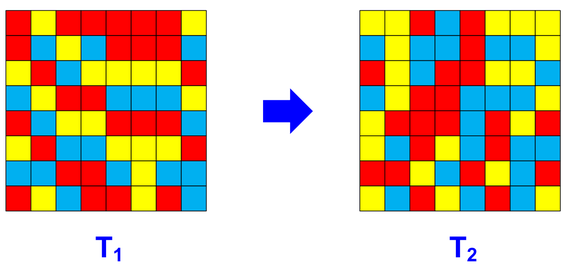
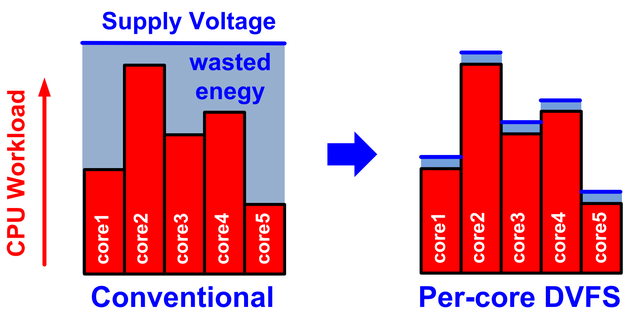
1. Motivation



Workload Variations

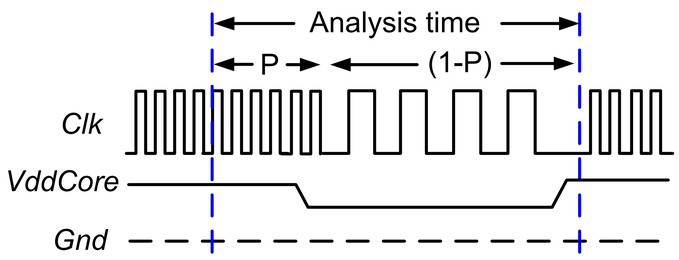
- Workload varies on different cores
- Workload changes over time



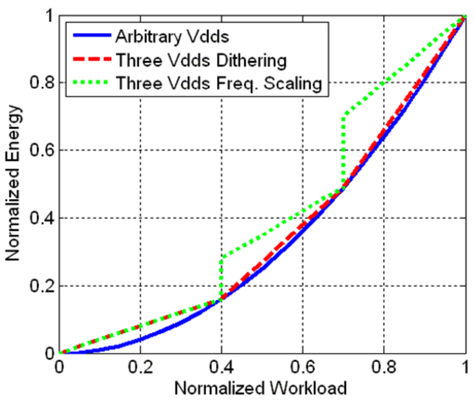
Dynamic Voltage/Frequency Scaling

- Scale voltage and frequency according to per-core workload to save power and energy

2. Voltage Dithering



$$Freq_{core} = P \times Freq_{High} + (1 - P) \times Freq_{Low}$$



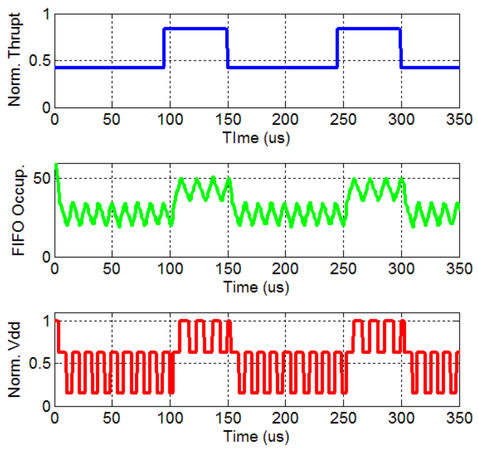
- ***Voltage dithering*** switches between the voltage and frequency pairs above and below the desired frequency.
- The energy efficiency of voltage dithering with three voltage domains is close to the ideal DVFS system with infinite voltage domains

3. Proposed Algorithm

1. FIFO Occupancy

- FIFO -> **full**, core -> **speed up**
- FIFO -> **empty**, core -> **slow down**
- For ***N*** Vdds, split FIFO into ***(2N-2)*** levels

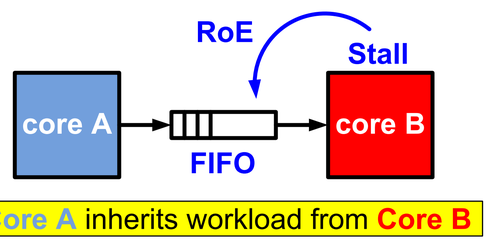
$$V_{occu} = \begin{cases} V_1, & \text{if } O_{curr} = L_1 \\ V_{pre+1}, & \text{if } O_{curr} > O_{pre+1} \\ V_{pre}, & \text{if } O_{pre-1} \le O_{curr} \le O_{pre+1} \\ V_{pre-1}, & \text{if } O_{curr} < O_{pre-1} \\ V_N, & \text{if } O_{curr} = L_{(2N-2)} \end{cases}$$



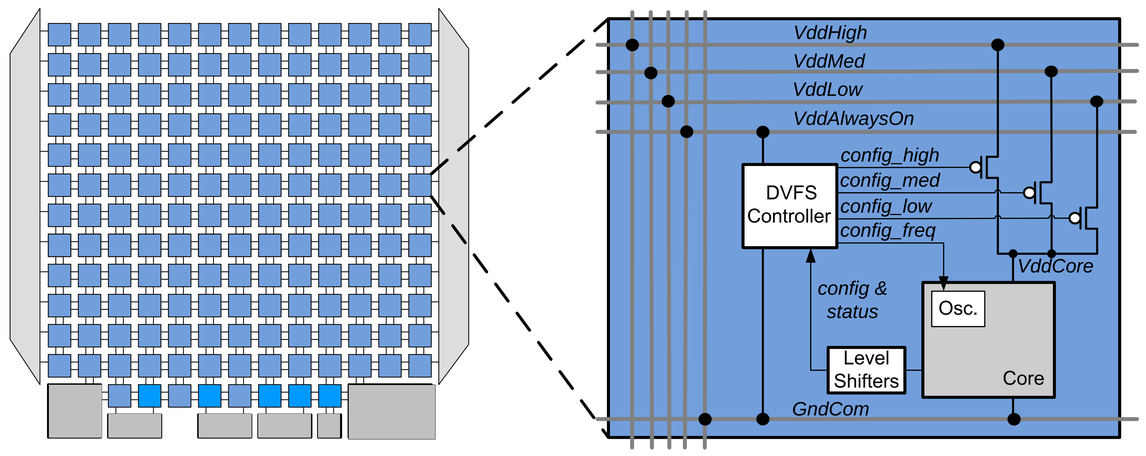
2. FIFO Stall Information

- Workload inheritance
- If inheritance is **true**, stall counter counts **up**
- If inheritance is **false**, stall counter counts **down**
- For ***N*** Vdds, ***(N-1)*** voltage switching thresholds for the stall counter

$$V_{stall} = \begin{cases} V_1, & \text{if } C_{Stall} \le T_1 \\ V_i, & \text{if } T_{i-1} < C_{Stall} \le T_i \\ V_N, & \text{if } C_{Stall} > T_{N-1} \end{cases}$$



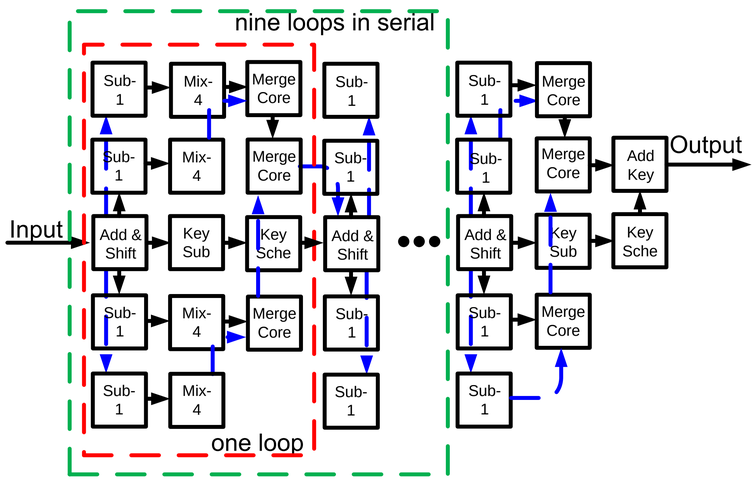
4. Experimental Many-Core System

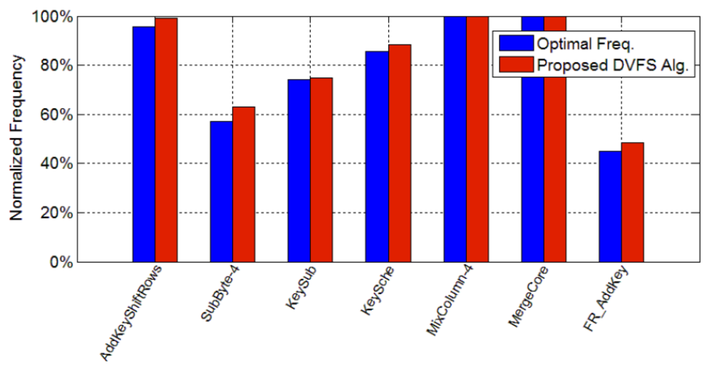


AsAP2 Single Tile (164 total)	
Area	0.17 mm²
Transistors	325,000
CMOS Tech.	65 nm low-leakage
Max. frequency	1.2GHz @ 1.3 V
Instru. Memory	128 x 32-bit
Data Memory	128 x 16-bit

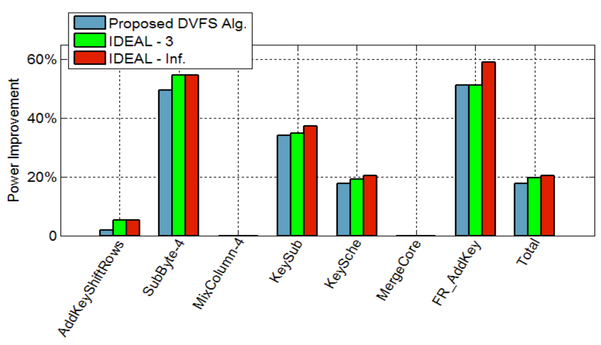
- In-order single-issue 6-stage pipeline
- Reconfigurable 2D-mesh network
- Per-core DVFS based on both FIFO occupancy and FIFO stall information
- Three global voltage and frequency levels

5. Benchmark: 137-core AES Engine





- Frequency selected by the proposed DVFS matches the optimal working frequency for each individual core



- Proposed DVFS algorithm saves 18% power, which is only 3% less than theoretical limits

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