Processor Shapes and Topologies for Dense On-Chip Networks

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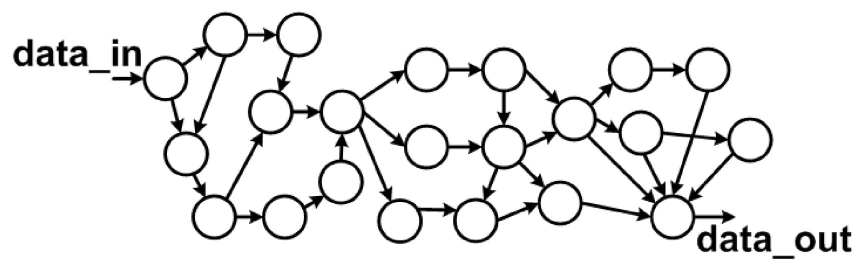
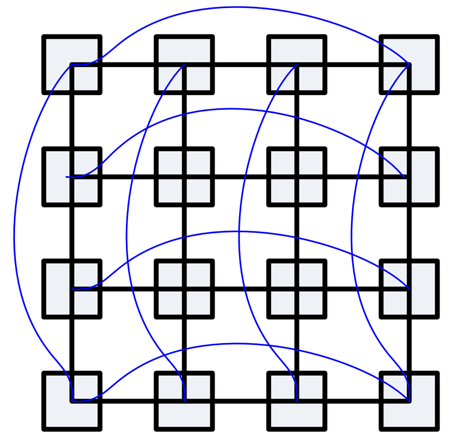
1. Overview

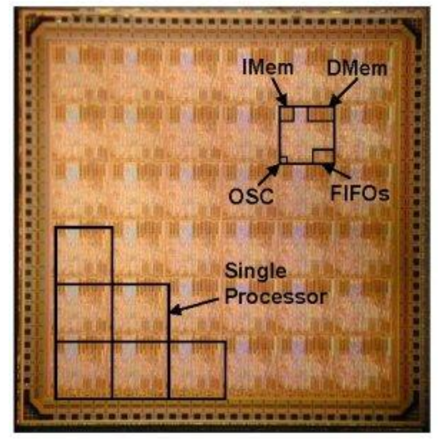
- **Many-core processor topology:** The available inter-processor interconnect affects the total application throughput, energy (power), chip area, and latency
- **Key motivation:** Commonly-used 2D mesh many-core processor arrays can have local congestion and long latencies for global traffic
- **Research target:** Topologies that increase application performance, reduce communication energy, avoid global wires, and ease physical implementation



Application (H.264)



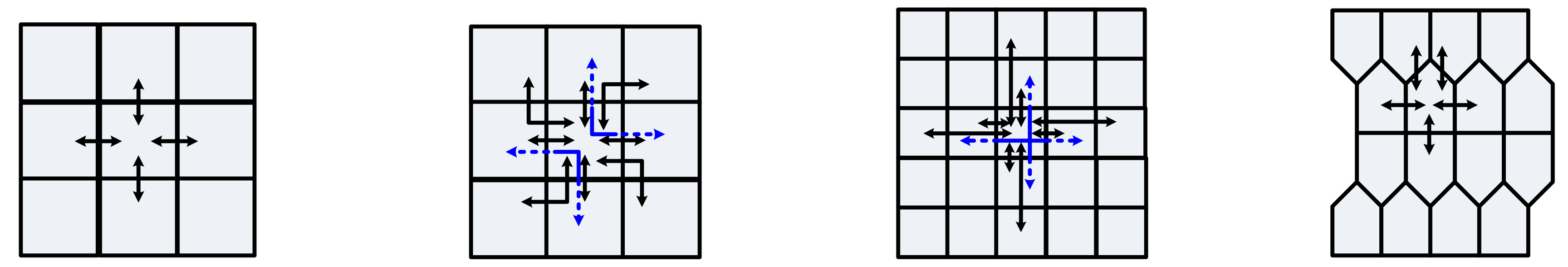
Topology



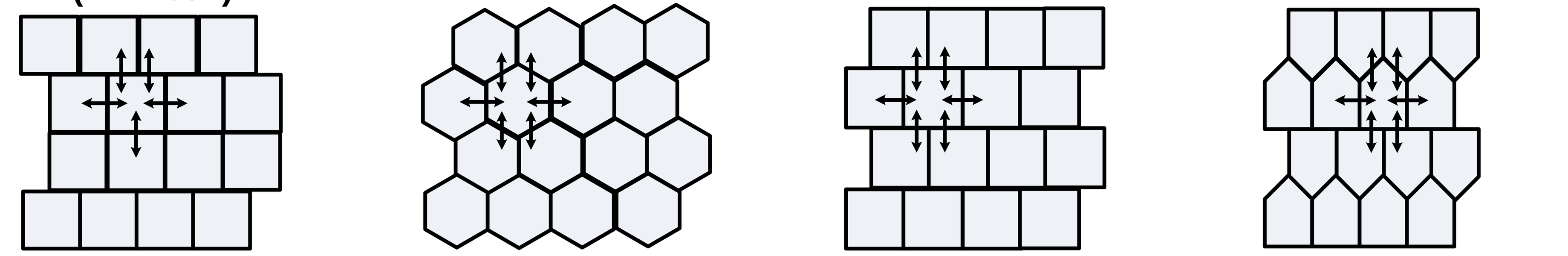
Many-core processor array

2. Proposed Topologies and Shapes

- **Key idea:** Novel interconnection topologies and processor tile shapes to increase the number of local inter-processor connections
- **Common 2D mesh and the seven proposed topologies**
  - Dense On-Chip Networks (NoCs) without long global wires
  - Two 5-neighbor, three 6-neighbor and two 8-neighbor topologies
  - Hexagonal-shaped and "House-shaped" processor tiles



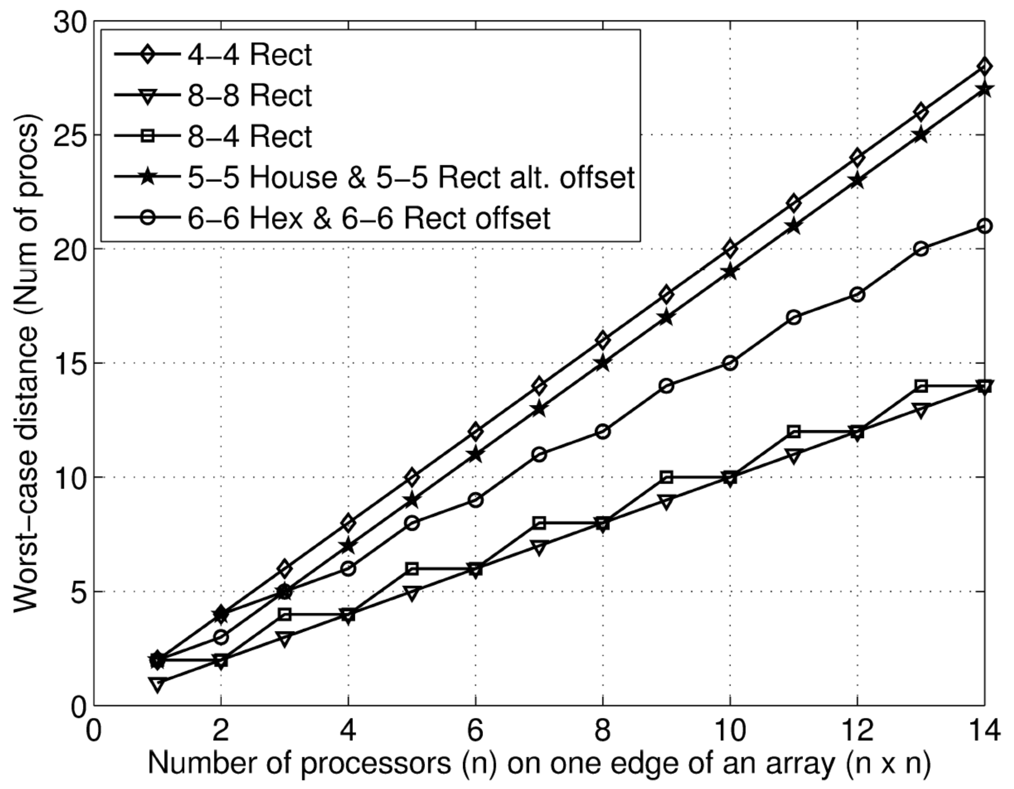
(a) 4-4 Rect (2D mesh) (b) 8-8 Rect (c) 8-4 Rect (d) 5-5 House



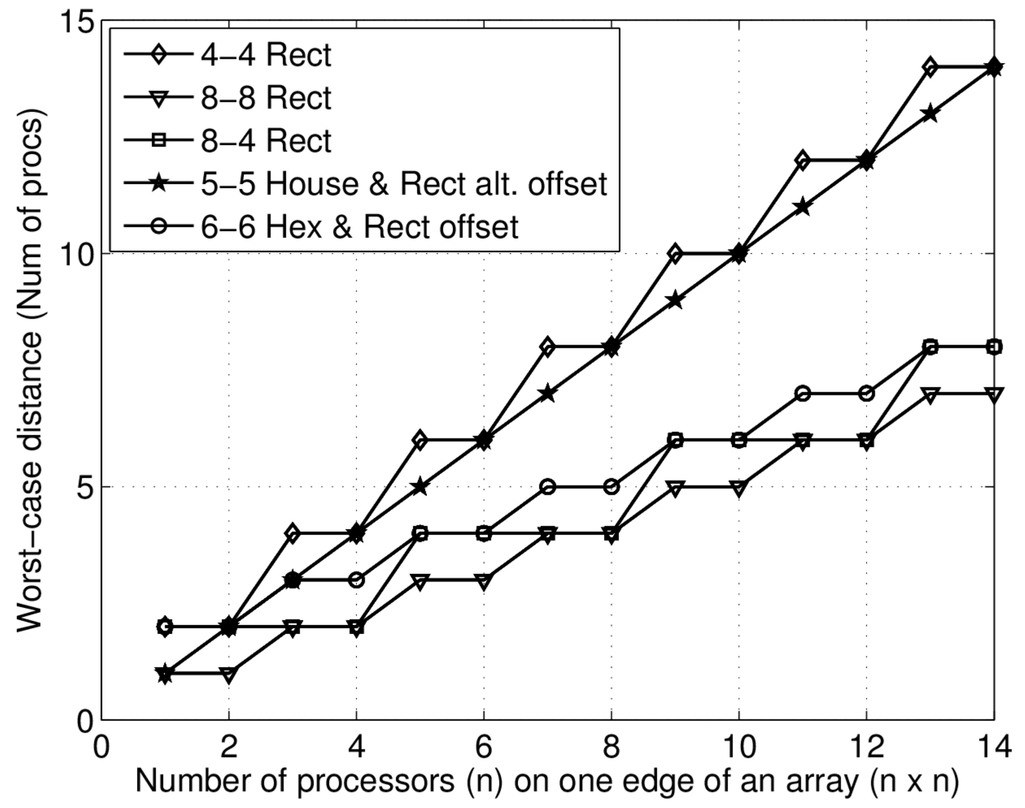
(e) 5-5 Rect alt. offset (f) 6-6 Hex (g) 6-6 Rect offset (h) 6-6 House alt. offset

3. Communication Latencies

- **Worst-case communication distance** for four basic communication patterns
  - One-to-one, one-to-all, all-to-all and all-to-one



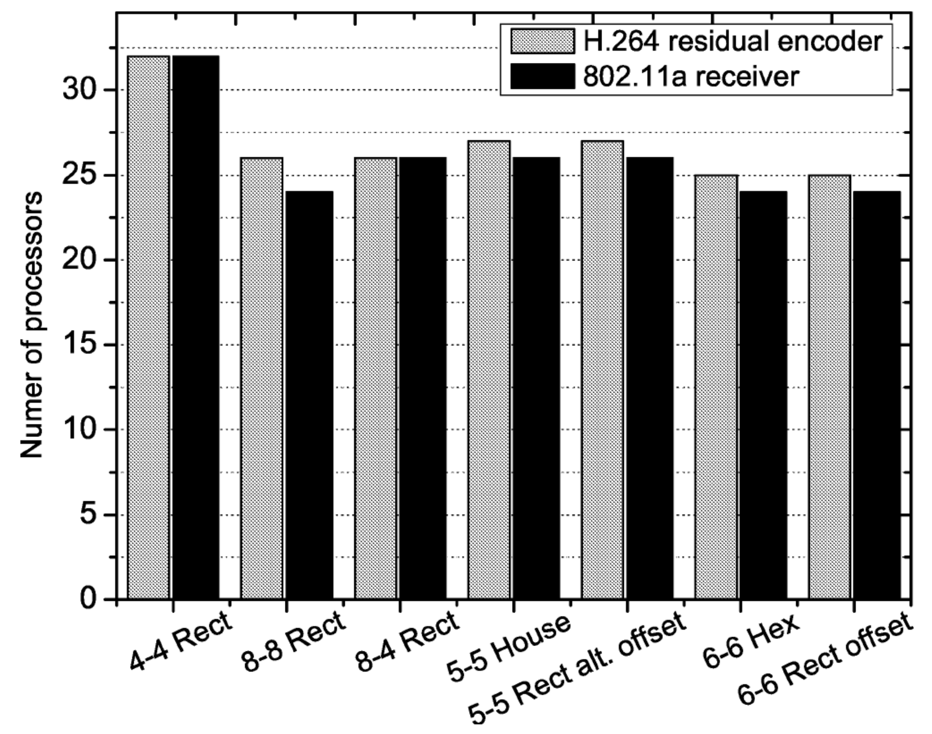
One-to-one, one-to-all and all-to-all



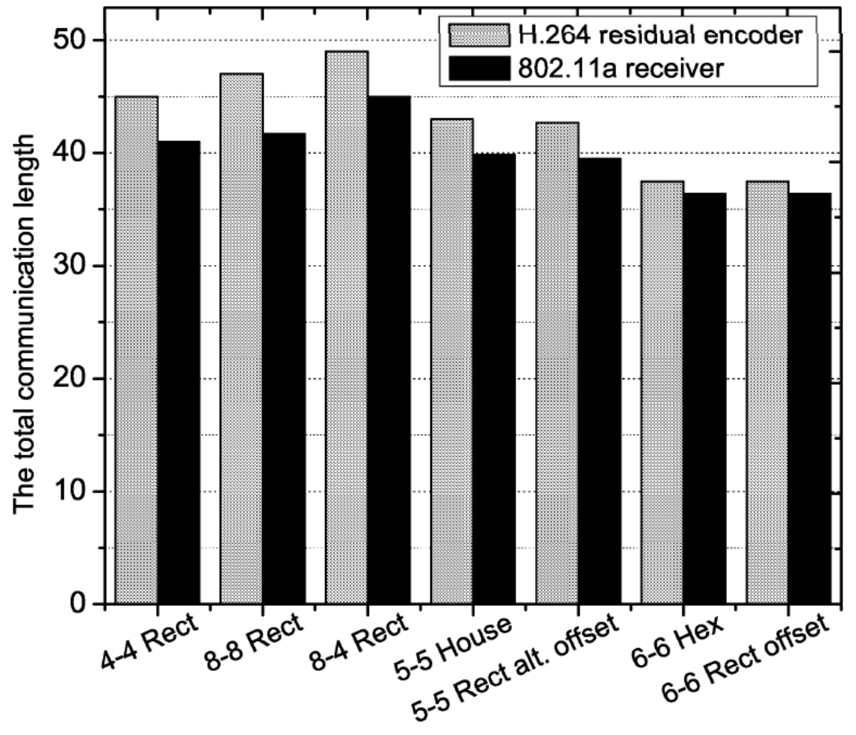
All-to-one

4. Application Mapping

- **Two complete real-time complex applications**
  - H.264 HDTV residual encoder and 802.11a Wi-Fi receiver
- **6-neighbor topologies vs. 4-neighbor 2D mesh**
  - 21% lower application area
  - 19% shorter total communication link length

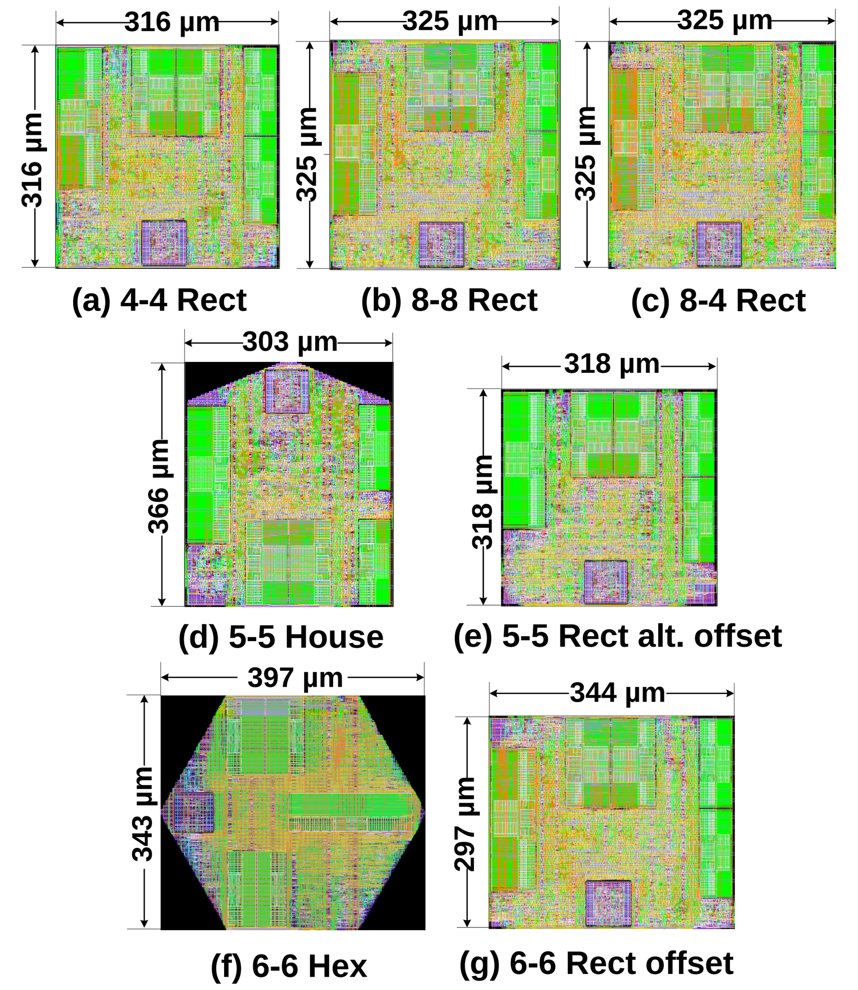


Number of processors



Total communication length

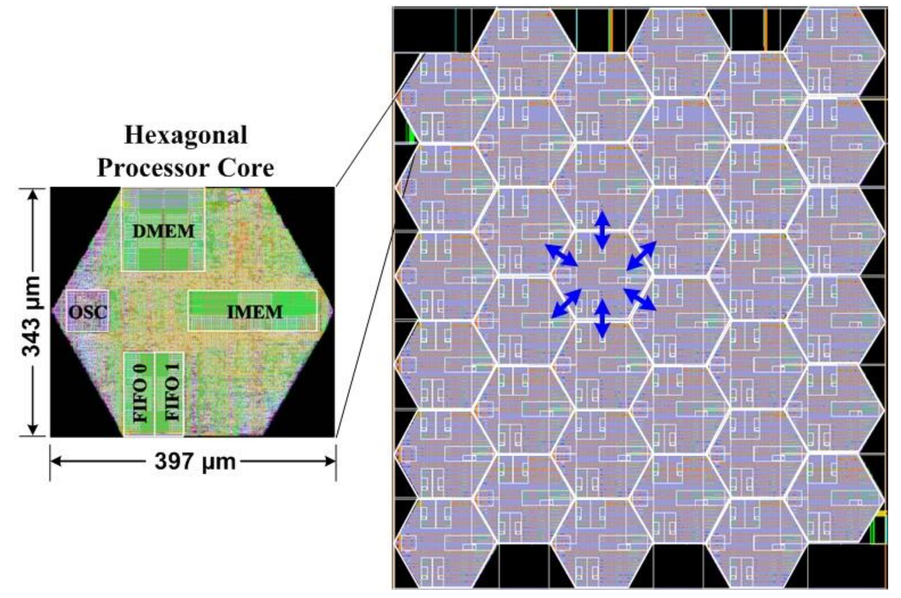
5. Physical Implementation



(a) 4-4 Rect (b) 8-8 Rect (c) 8-4 Rect (d) 5-5 House (e) 5-5 Rect alt. offset (f) 6-6 Hex (g) 6-6 Rect offset

Processor tiles for all topologies

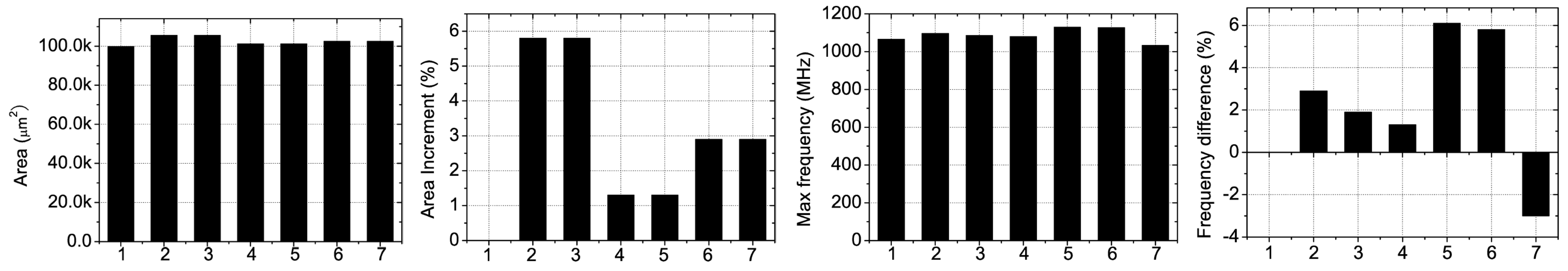
- 16-bit DSP tile tailored for all topologies
- 65 nm standard-cell CMOS
- DRC and LVS clean
- Design iterations to find minimum area
- Easy array design by abutting proc. tiles



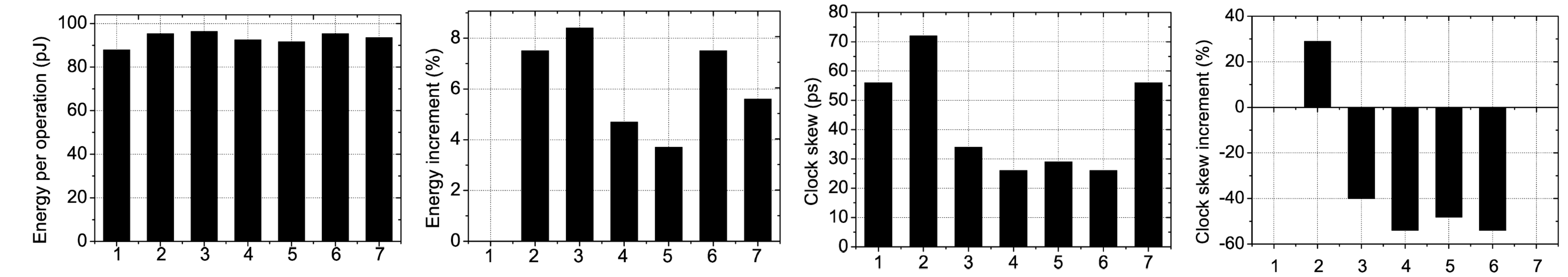
Hexagonal-shaped processor tile and 6x6 chip multiprocessor

6. Chip Implementation Results

- **Non-2D-mesh designs** have:
  - Larger area per tile (+1.3% to +5.9%) partially caused by higher fan-in and fan-out I/O port logic
  - Higher energy per operation (+3.7% to +8.4%)
  - Non-rectangular tiles have lower clock skew (–40% to –54%)
- Results would improve with optimization of items such as SRAM and tile I/O port placements



(a) Area (b) Incremental area (c) Freq. (d) Incremental freq.



(e) Energy per op. (f) Incremental energy per op. (g) Clock skew (h) Incremental clock skew

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