A Complete Real-Time 802.11a Baseband Receiver Implemented on an Array of Programmable Processors

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Outline

- Architecture of a 802.11a Digital Baseband Receiver
- The Target Many-core Computational Platform
- Implementation of the Receiver
- Results and Analysis
- Conclusion

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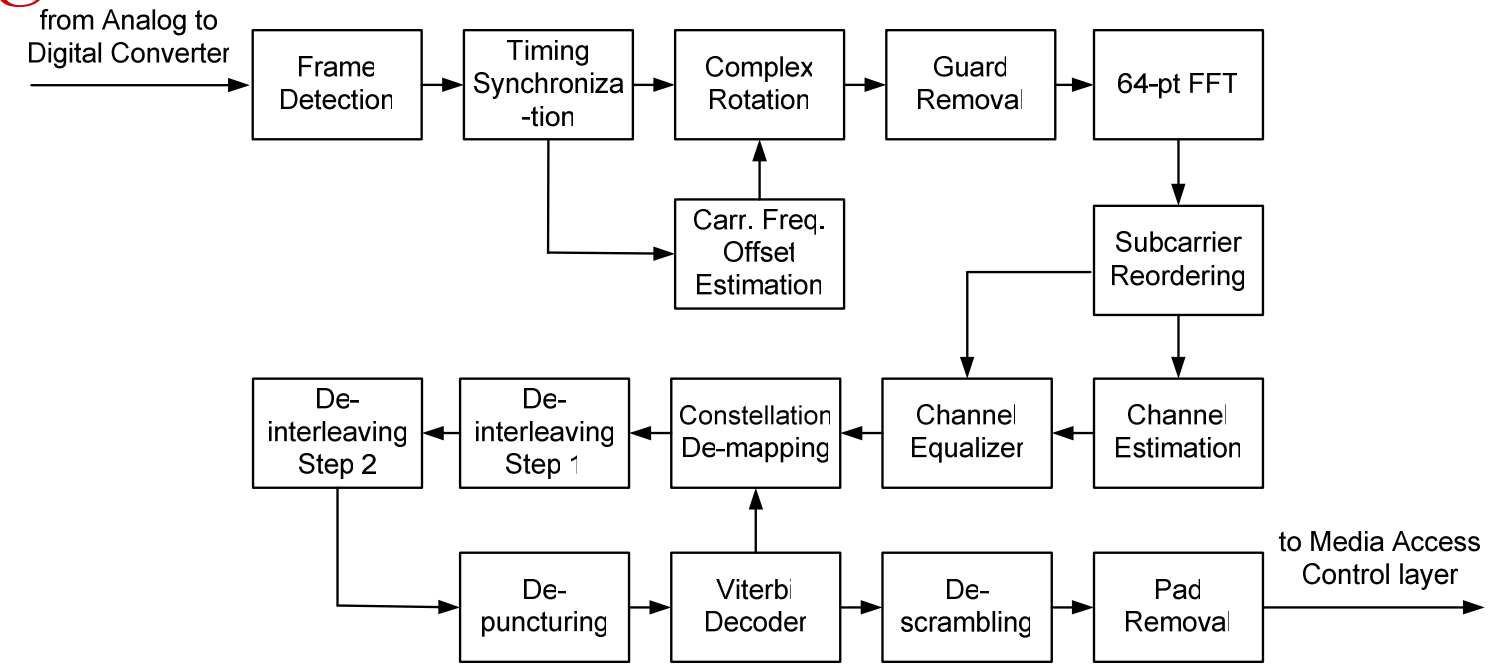
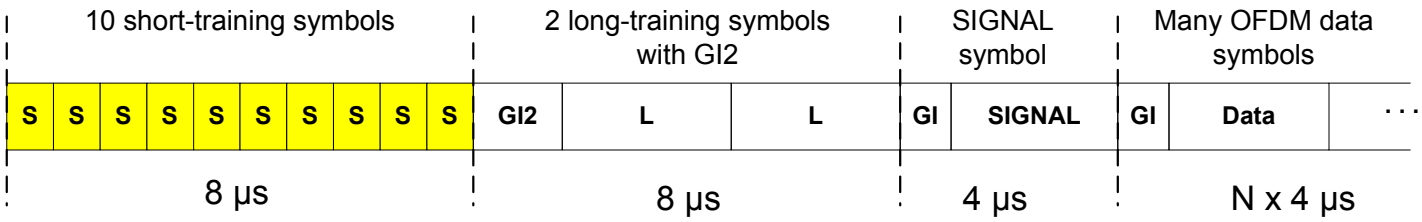
Architecture of a Complete 802.11a Digital Baseband Receiver



- Three important features required for a practical receiver:
  - Frame detection and timing synchronization
  - Carrier frequency offset (CFO) estimation and correction
  - Channel estimation and equalization

Frame Detection and Timing Synchronization



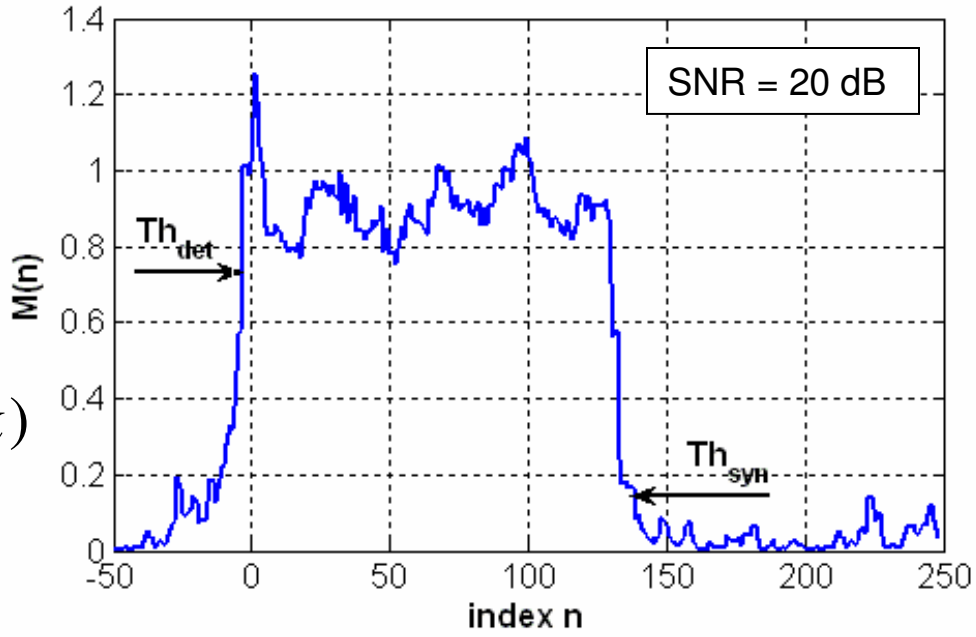
- Timing metric (*):

$$M(n) = \frac{|P(n)|^2}{Q(n)^2}$$

where:

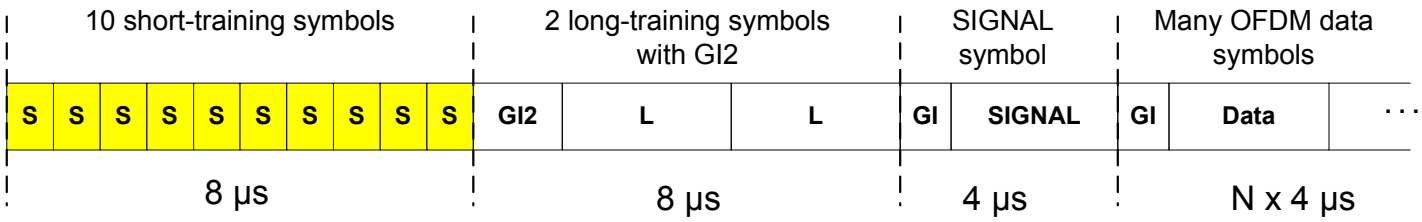
$$P(n) = \sum_{k=0}^{15} r(n+k+16).r^*(n+k)$$

$$Q(n) = \sum_{k=0}^{15} |r(n+k)|^2$$



(*)T.M. Schmidl and D.C. Cox, "Robust frequency and timing synchronization for OFDM," *IEEE Transactions on Communications*, pp. 1613-1621, Dec. 1997

Frame Detection and Timing Synchronization



- Frame detection:

$$M(n) > Th_{\det}$$

or:

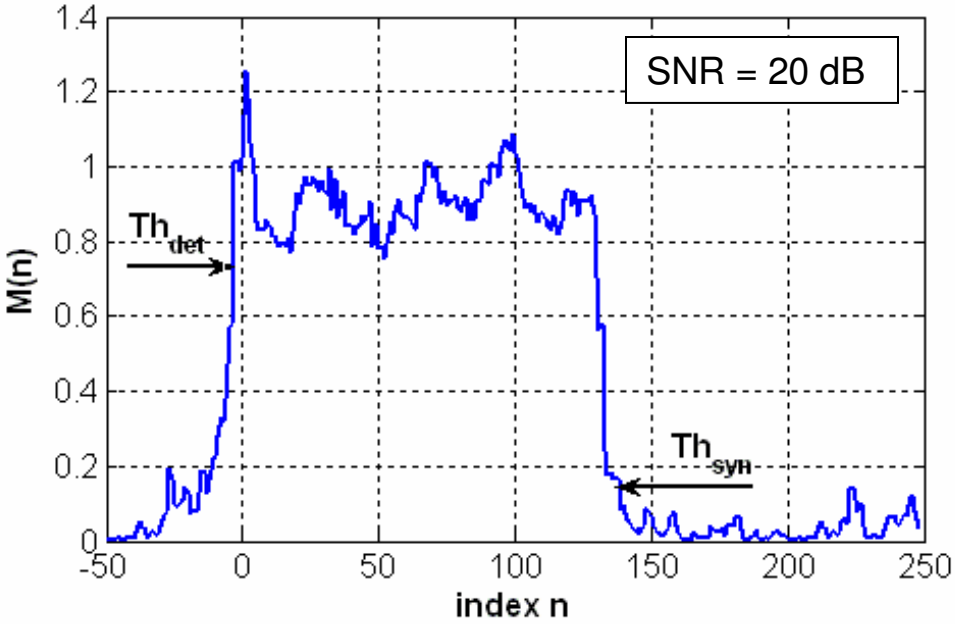
$$|P(n)|^2 > Th_{\det} \cdot Q(n)^2$$

- Timing synchronization:

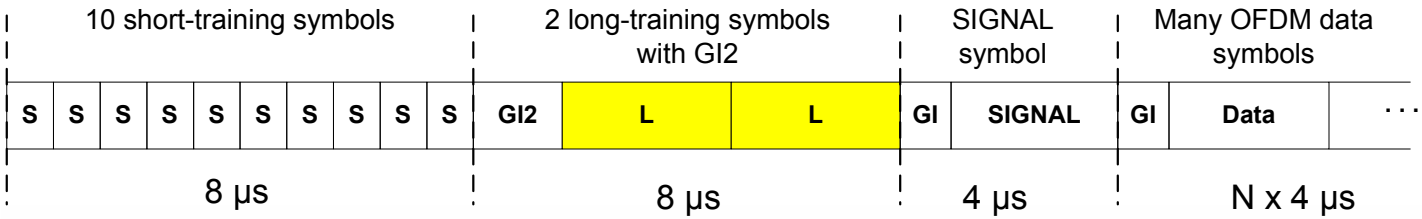
$$M(n) < Th_{syn}$$

or:

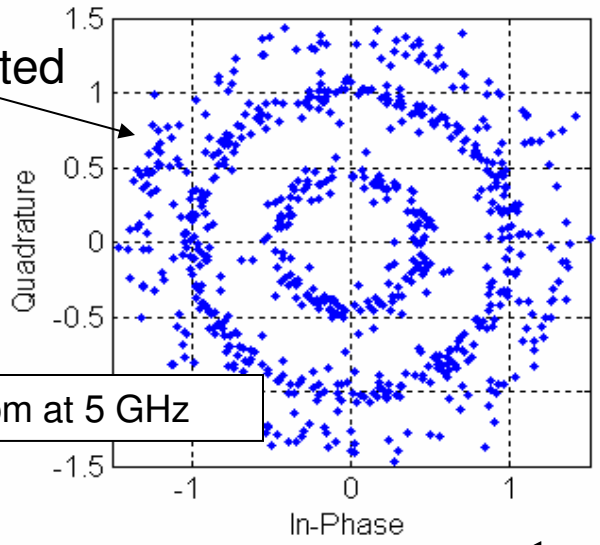
$$|P(n)|^2 < Th_{syn} \cdot Q(n)^2$$



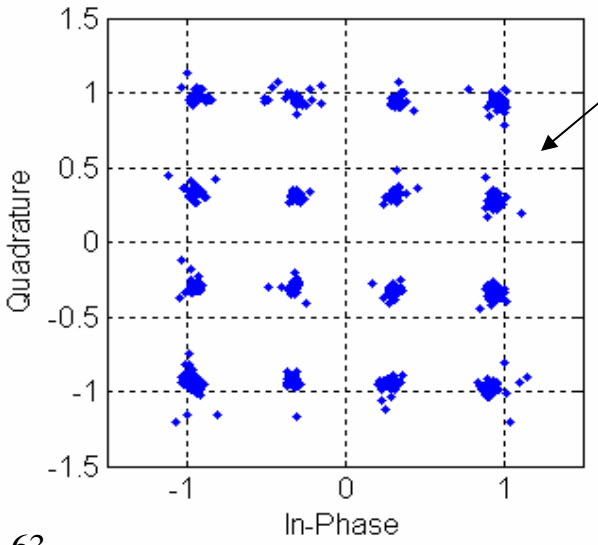
CFO Estimation and Compensation



Before Compensated



CFO = 10 ppm at 5 GHz

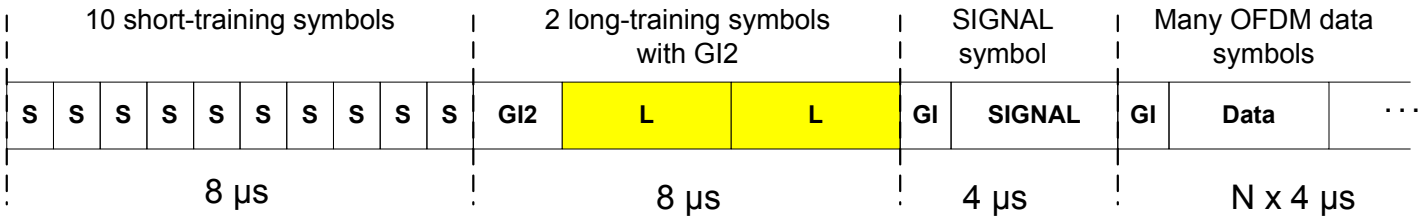


After compensated

- Offset angle (*): $$\alpha = \frac{1}{64} \angle \sum_{k=0}^{63} L_2(k).L_1^*(k)$$
- CFO compensation: using CORDIC Rotation algorithm

(*) E. Sourour et al., “Frequency offset estimation and correction in the IEEE 802.11a WLAN,” *IEEE Vehicular Technology Conference*, pp. 4923-4927, Sep. 2004.

Channel Estimation and Equalization



- Channel coefficients: $$H(k) = \frac{1}{2} \cdot \frac{\widetilde{L}_1(k) + \widetilde{L}_2(k)}{\hat{L}(k)}$$

- Channel equalization: $$\widehat{S}_m(k) = \frac{\widetilde{S}_m(k)}{H(k)}$$

$$= \widetilde{S}_m(k) \cdot C(k)$$

where: $$C(k) = \frac{1}{H(k)} = \frac{2\hat{L}(k)}{\widetilde{L}_1(k) + \widetilde{L}_2(k)}$$

P. Hung et al., “Fast division algorithm with a small lookup table,” IEEE Asilomar CSSC, pp. 1465-1468, Oct. 1999.

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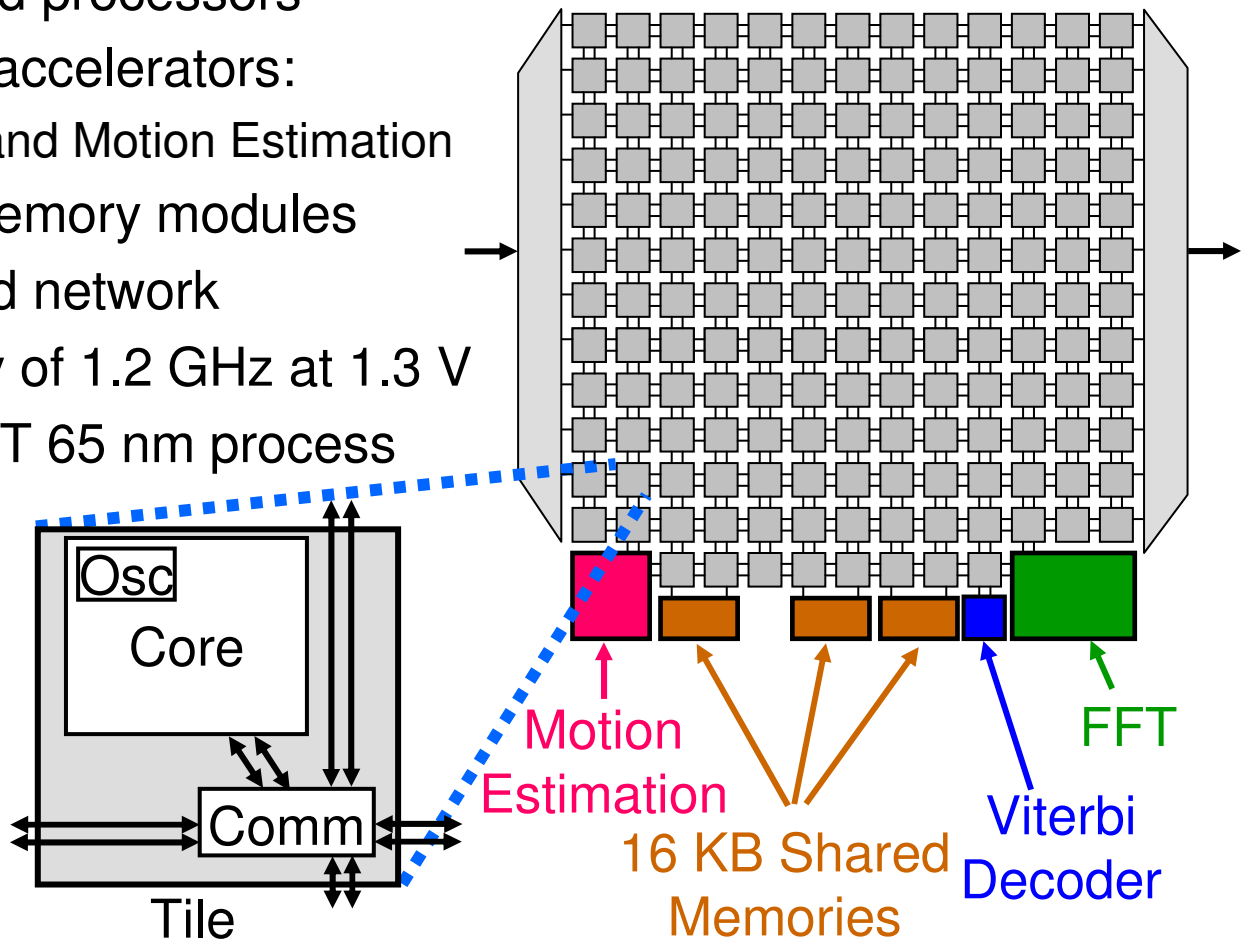
The Target Computational Platform

- Key features (*):
  - 164 fine-grained processors
  - 3 configurable accelerators:
    - FFT, Viterbi and Motion Estimation
  - 3 big shared memory modules
  - Circuit-switched network
  - Max. frequency of 1.2 GHz at 1.3 V
  - Fabricated in ST 65 nm process



(*) D. Truong, et at., " A 167-processor 65 nm Computational Platform with Per-Processor Dynamic Supply Voltage and Dynamic Clock Frequency Scaling}," *VLSI Circuits Symposium*, Jun. 2008.

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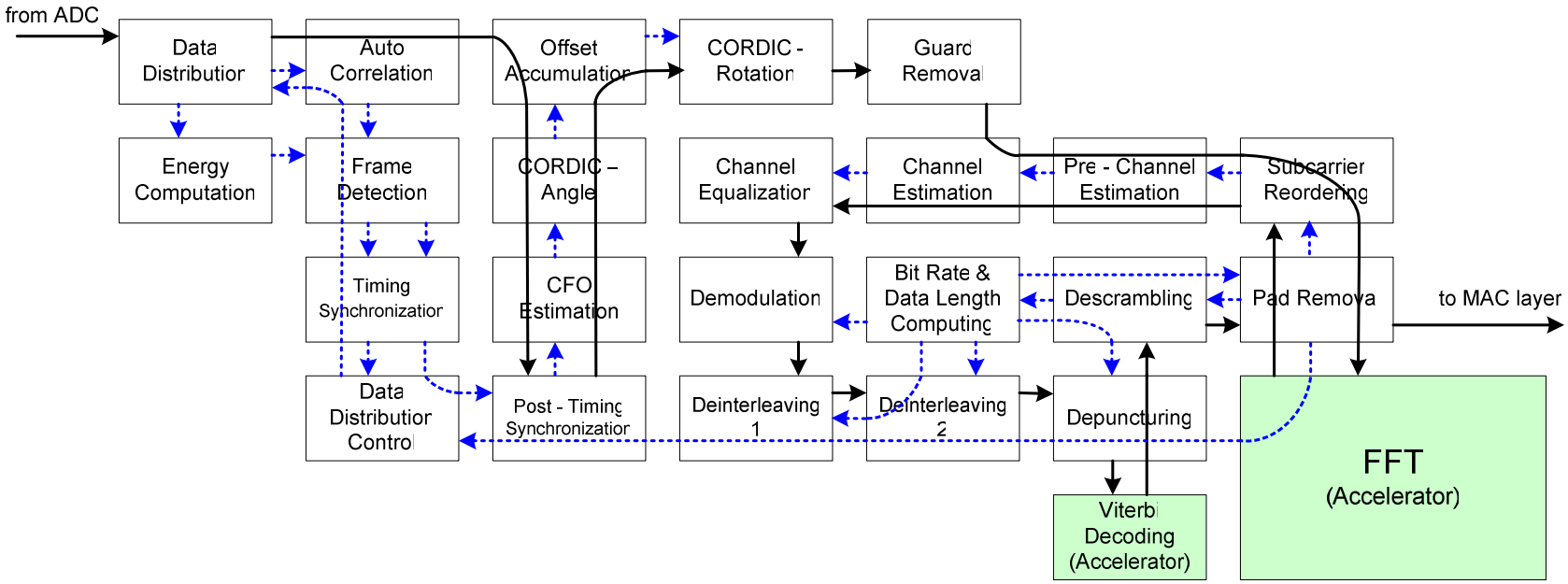
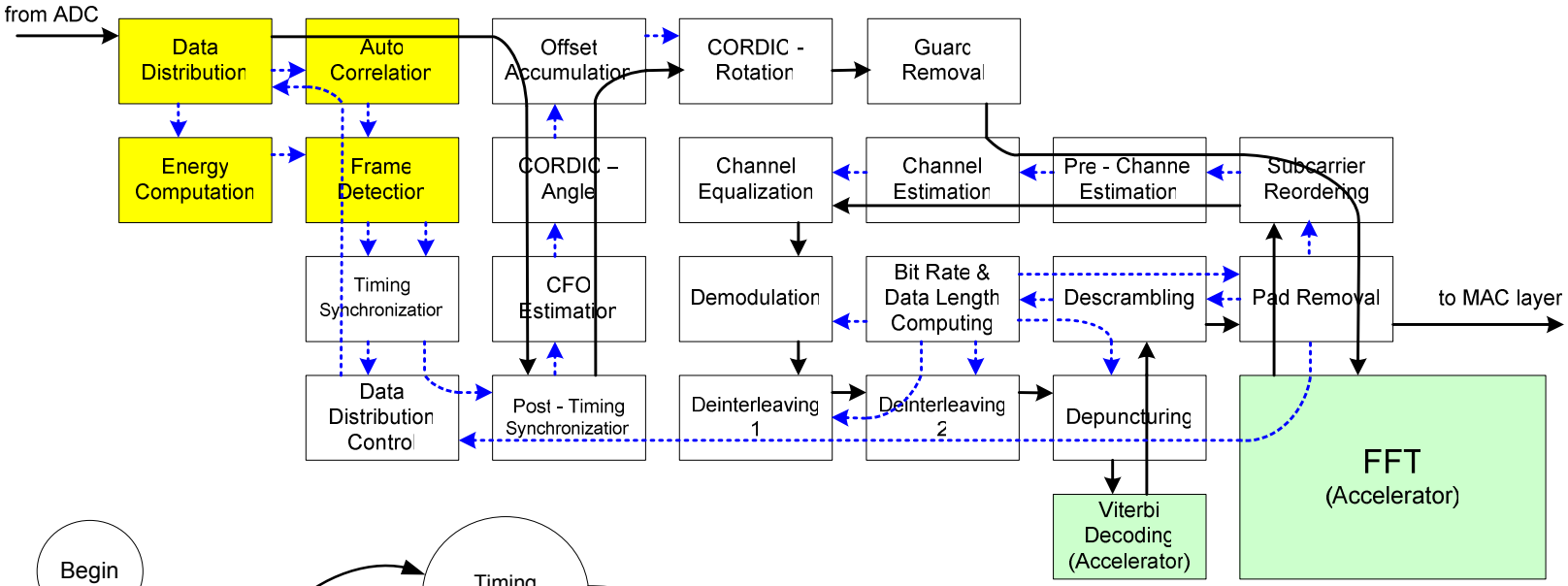
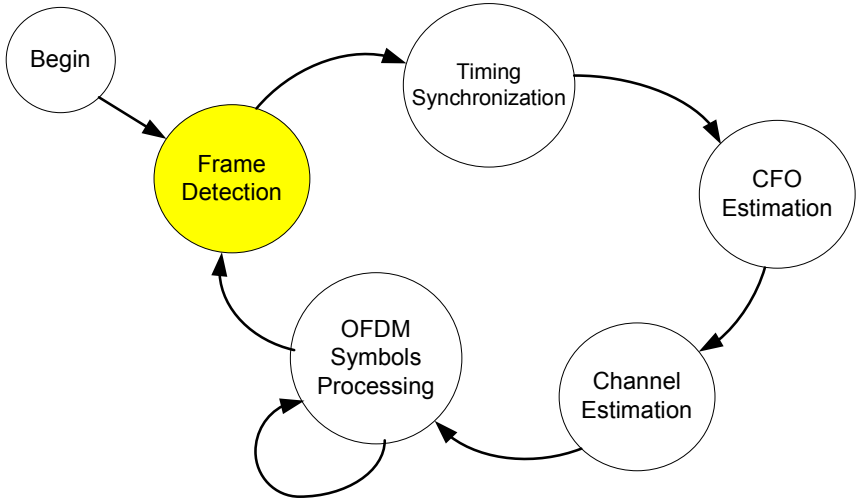
Implementation of the Receiver



- Implement whole system using Matlab
- Program each function on one/many processors using the AsAP assembly language
- Map whole system on the AsAP platform
- Compare results with Matlab

The Receiver Operates Obeying a FSM



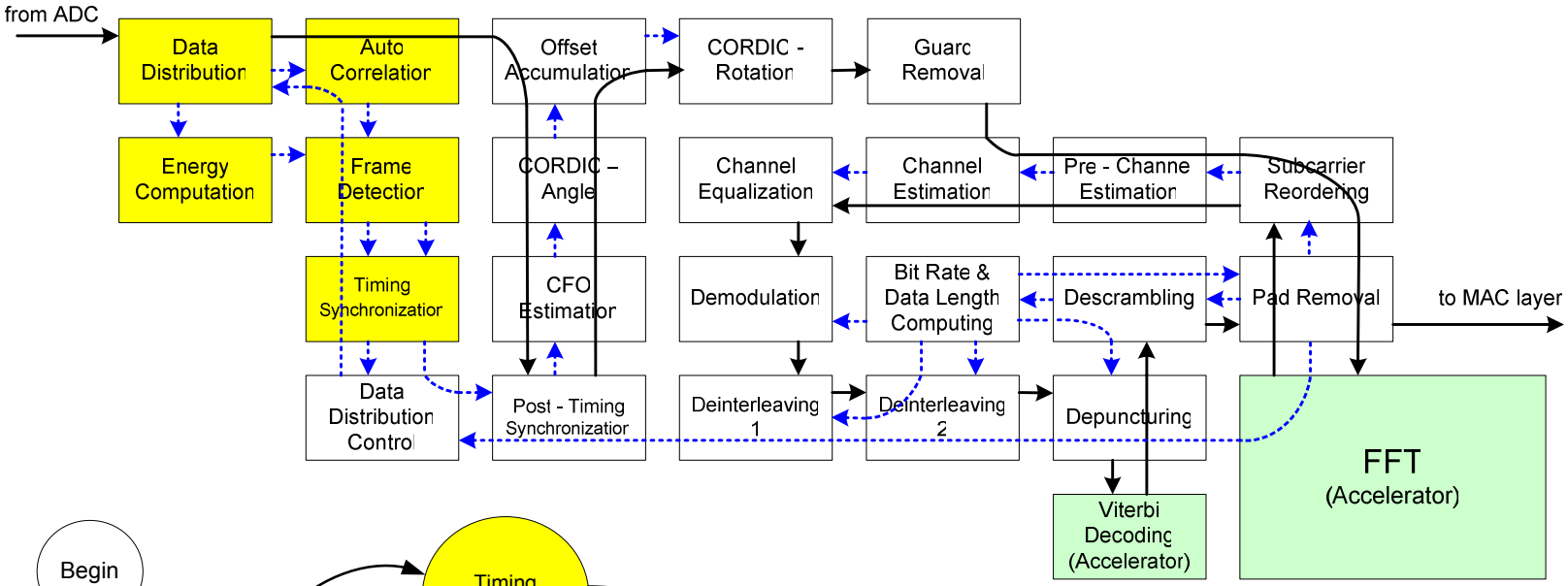


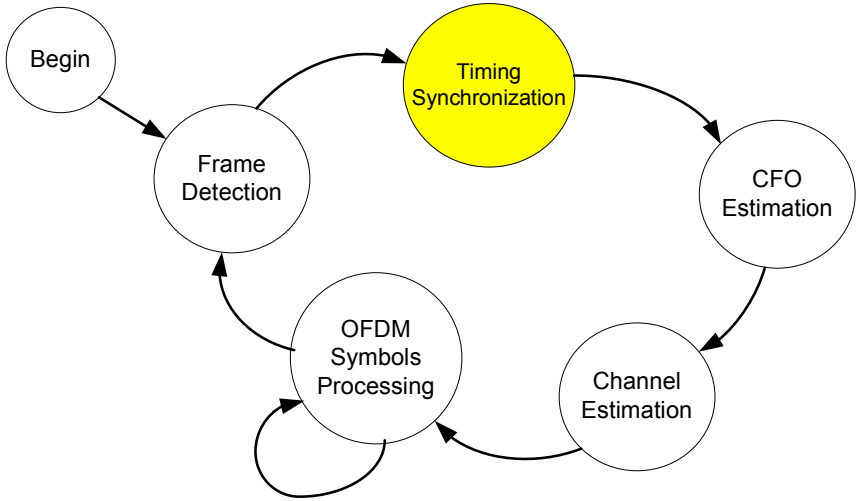
- Compute P(n) and Q(n)
- Frame is detected if

$$|P(n)|^2 > Th_{\text{det}} \cdot Q(n)^2$$

for 48 consecutive samples

The Receiver Operates Obeying a FSM

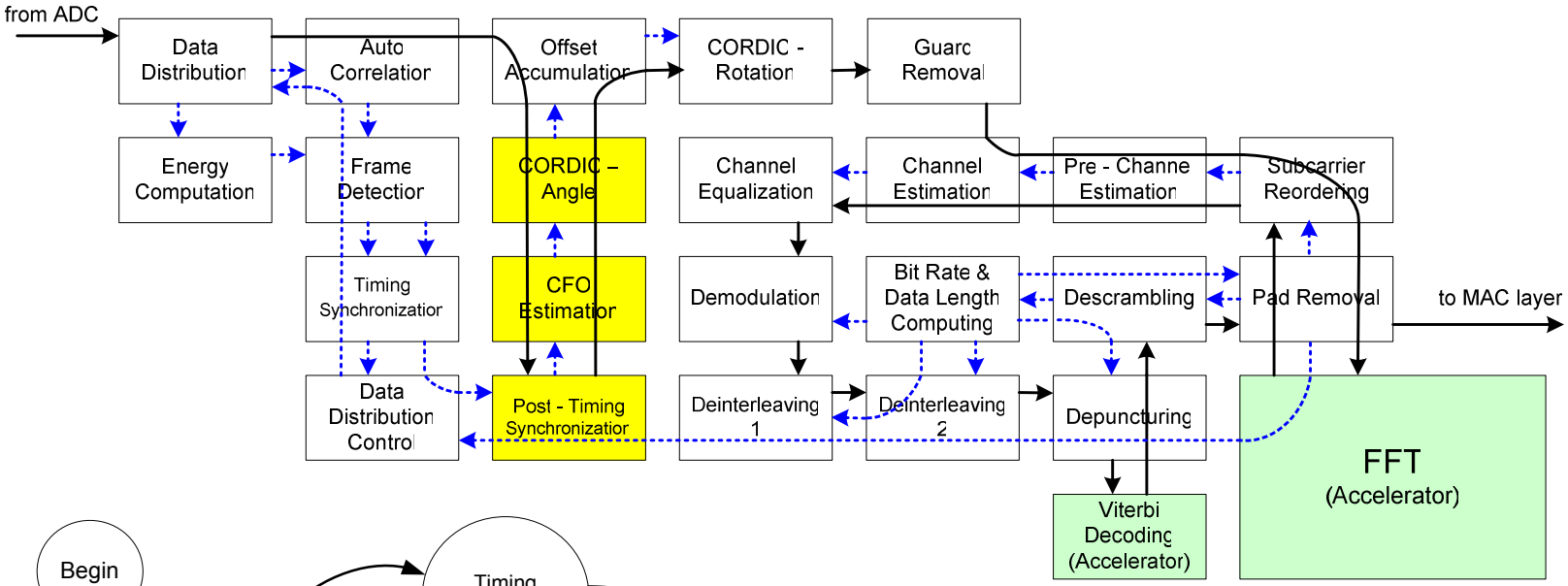


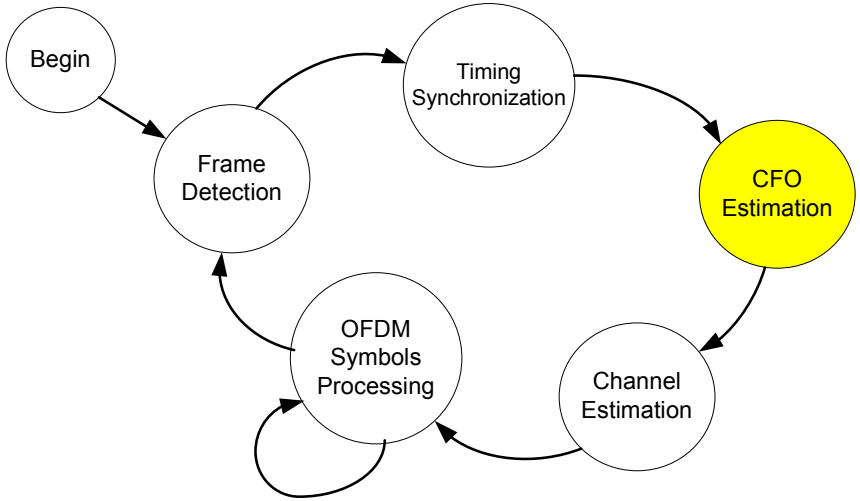


- Compute P(n) and Q(n)
- After frame is detected
- Timing is synchronized at first sample that satisfies

$$|P(n)|^2 < Th_{syn} \cdot Q(n)^2$$

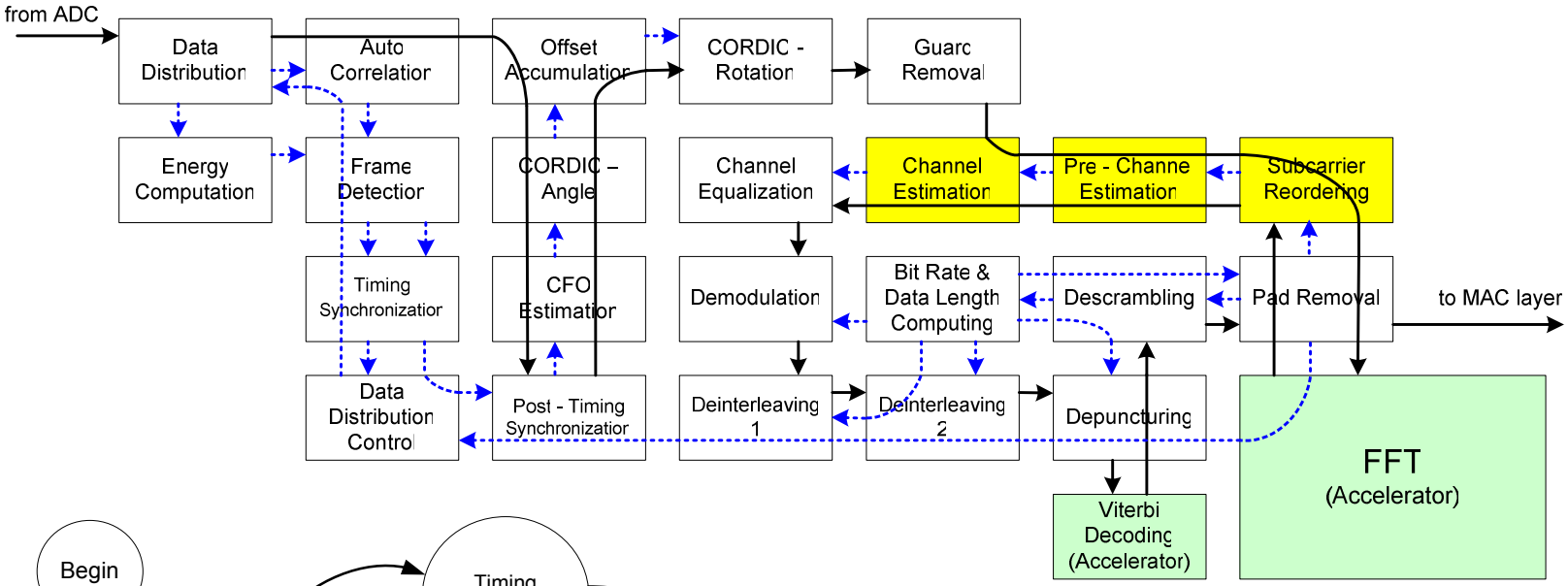
The Receiver Operates Obeying a FSM

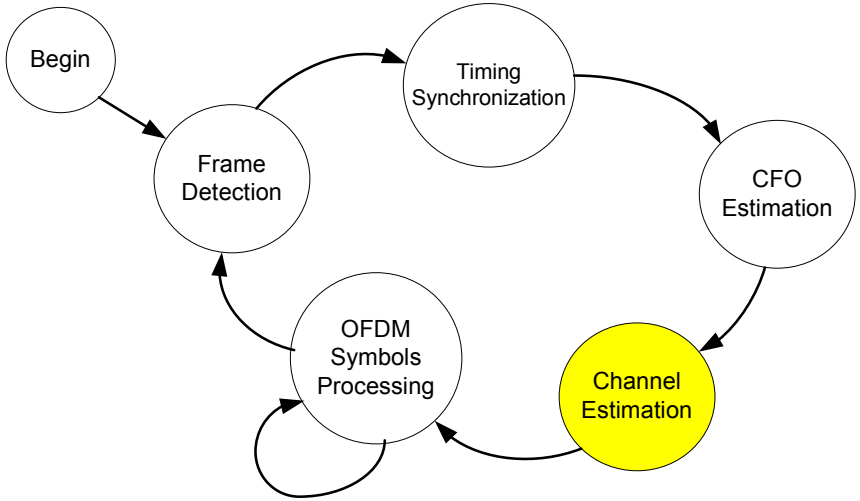




- Compute offset vector using two long-training symbols
- Compute offset angle α using CORDIC Angle algorithm

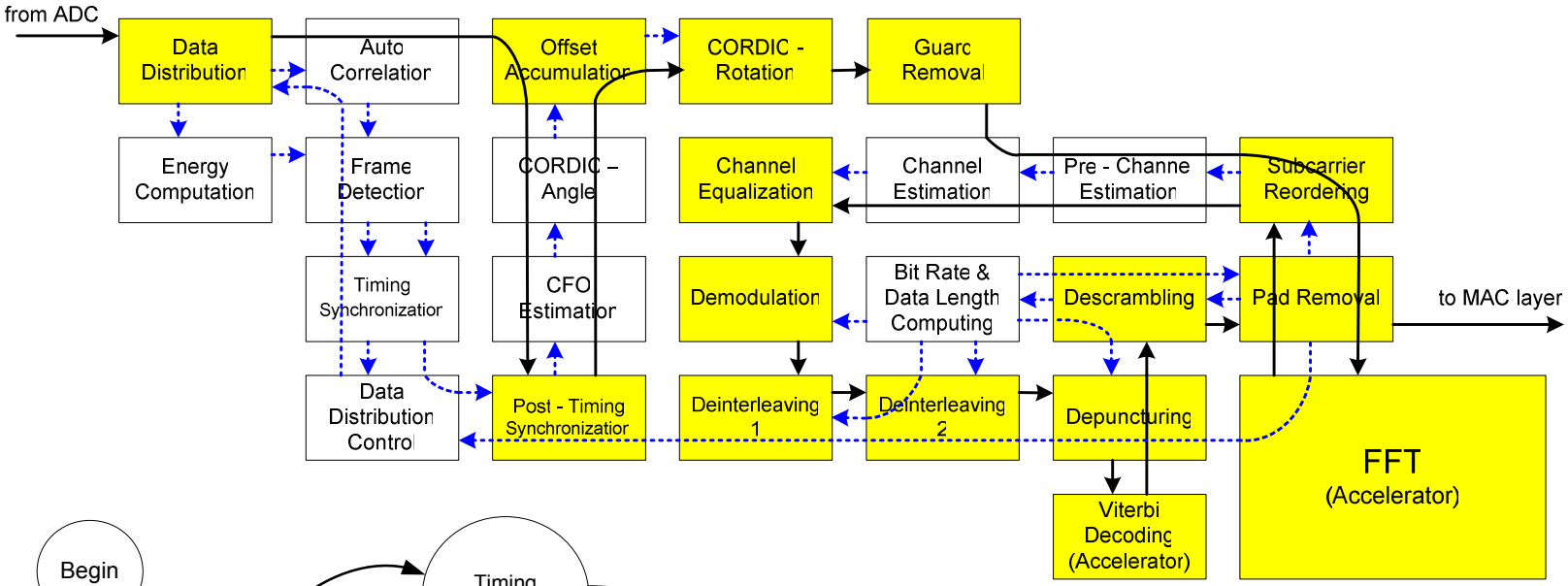
The Receiver Operates Obeying a FSM

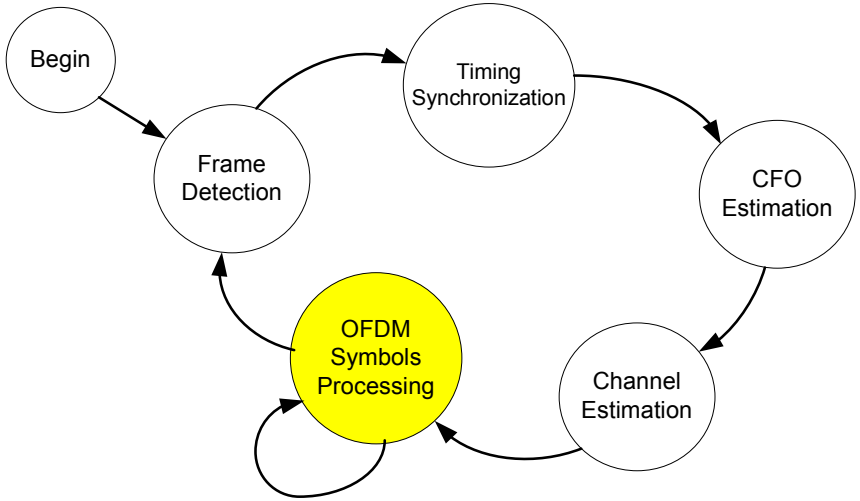




- Compute C(n) from two long-training symbols in the frequency domain (after FFT)

The Receiver Operates Obeying a FSM





- Includes all processors on the critical data path
- The OFDM SIGNAL symbol is used to decide the modulation scheme and code rate for all DATA symbols

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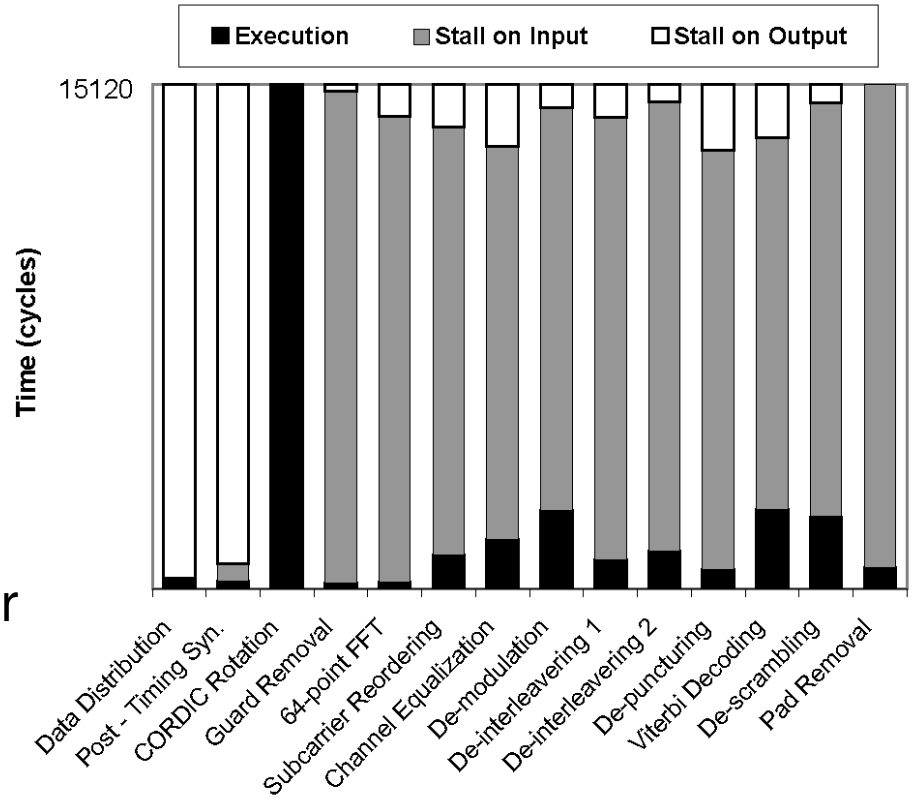
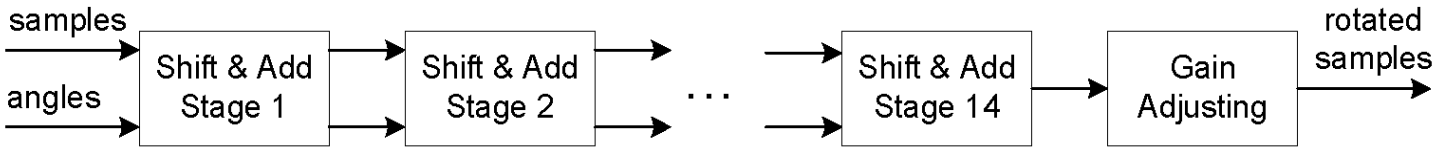
Throughput Evaluation

- Processors on the critical data path determines the receiver's throughput
- Each processor operates as one stage of a pipeline
- The CORDIC Rotation processor is system bottleneck
- One OFDM symbol is processed by each processor in 15120 cycles
- To achieve 54 Mbps throughput, all processors must run at 3.78 GHz

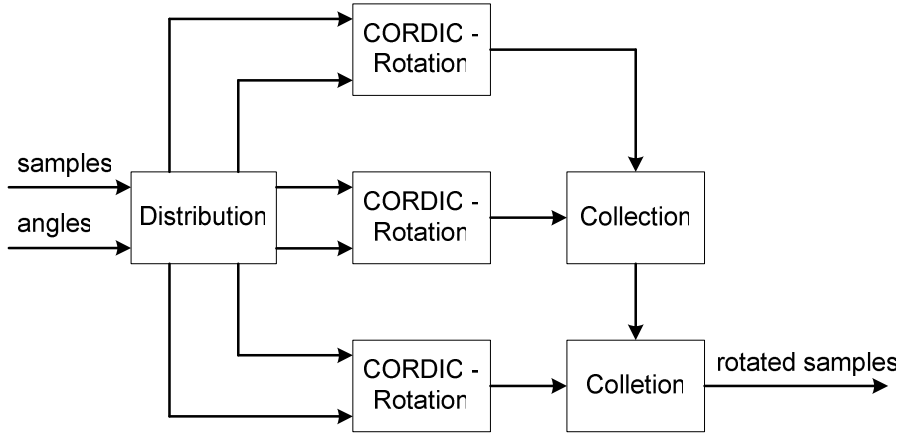


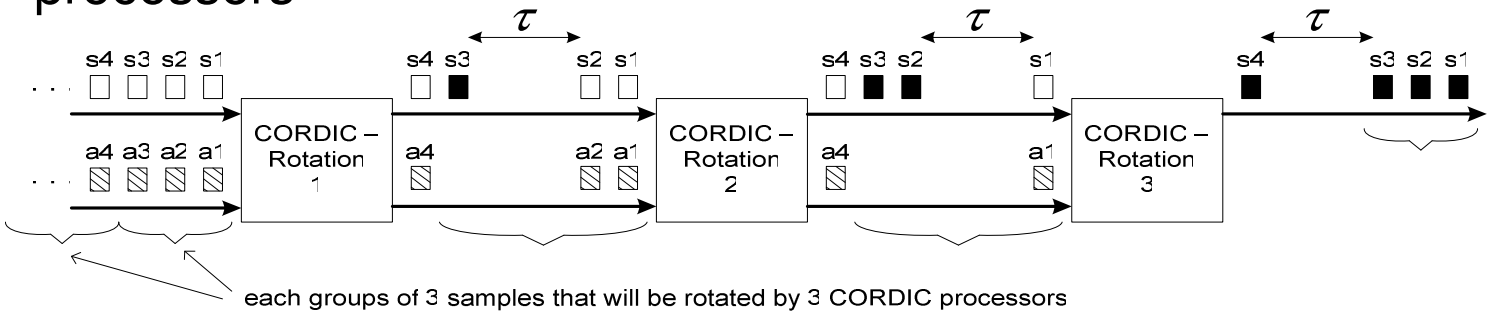
Throughput Improvement

- Using 15 processors to pipeline the CORDIC algorithm:



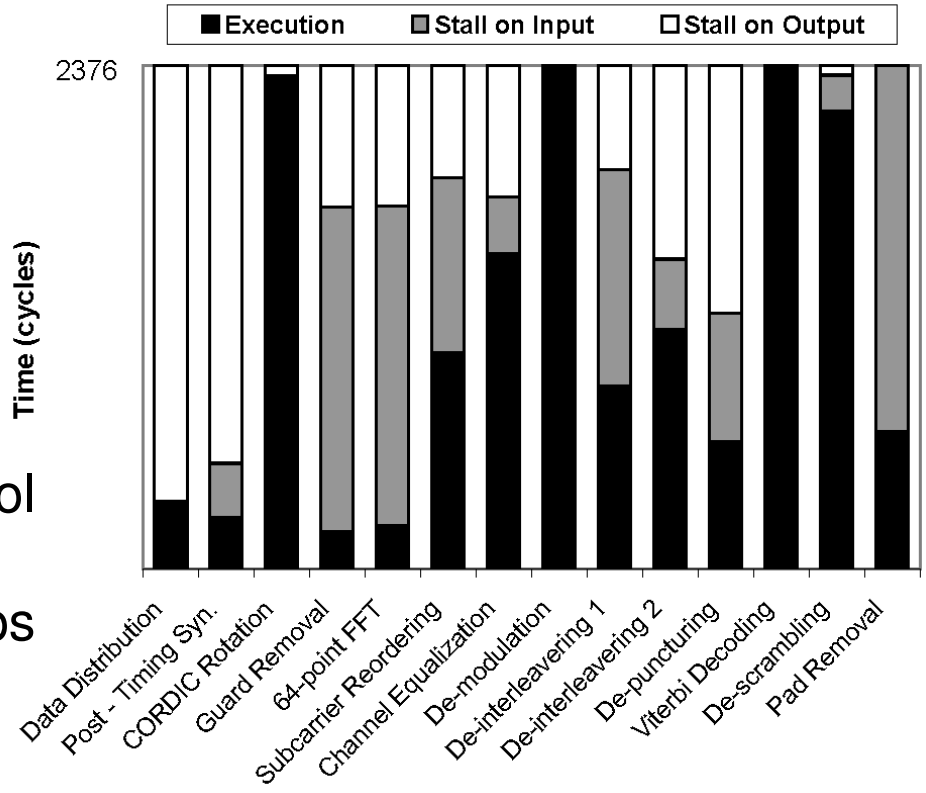
- Using many CORDIC processors in parallel:
  - Method 1: 2 N processors to support N CORDIC processors
  - Method 2: Only N processors





Throughput Improvement

- When using 7 CORDIC processors in parallel, the Viterbi Decoder becomes bottleneck
- No further improvement is possible by software
- Now, each processor processes one OFDM symbol in 2376 cycles
- The receiver obtains 54 Mbps throughput at 590 MHz



Comparison

Work by	Platform	Tech. (nm)	Max Freq. (MHz)	Fram. Det. & Syn.	CFO Est. & Comp.	Chan. Est. & Eq.	Throughput (Mbps)	Scaled to 65 nm
Tariq	TI 62x	180	200	-	-	√	1.7	4.7
Bakker	Strong ARM	350	130	√	√	-	4.3	23.2
Yung	CoPro.	180	260	-	-	√	12	33.2
Lin	SODA	180	400	√	-	√	24	66.4
Sereni	TI 64x	130	600	√	√	√	36	72
Akabane	SDR	90	280	√	-	√	54	74.7
this work	**AsAP2**	**65**	**1200**	√	√	√	**110**	**110**

- Our receiver sustains 110 Mbps throughput at max frequency of 1.2 GHz
- It is a complete one and 1.5x – 23x faster than others

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Summary

- Fine-grained many-core platform
  - Task-level parallelism
  - Highly flexible and scalable
  - Many ways to speedup an application
- A complete 802.11a baseband receiver
  - Supports all necessary features of a real receiver
  - Sustain real-time 54 Mbps throughput at 590 MHz
  - Can sustain up to 110 Mbps if running at maximum frequency
  - Many times faster than other related works
- Future work
  - Improve accelerators
  - Upgrade the platform for mapping more wireless applications

Acknowledgments

- Intellasys Inc.
- a VEF fellowship
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- ST Microelectronics
- UC Micro
- NSF Grant 0430090 and CAREER Award 0546907
- Intel
- S Machines

The End

THANK YOU !

Compute Bit Rate and Frame Length