Dynamic Voltage and Frequency Scaling Circuits with Two Supply Voltages

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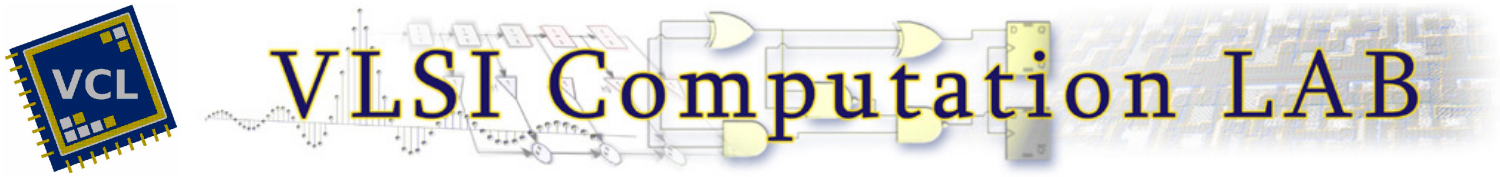

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Outline

- **Background and Motivation**
- Implementation
- Results

DVFS Background

$P_{dyn} = \alpha C V dd^2 f$ $\quad$ $Vdd \downarrow f \downarrow \Rightarrow P_{dyn,leak} \downarrow$

$E = C V dd^2$ $\quad$ $Vdd \downarrow \Rightarrow E \downarrow$

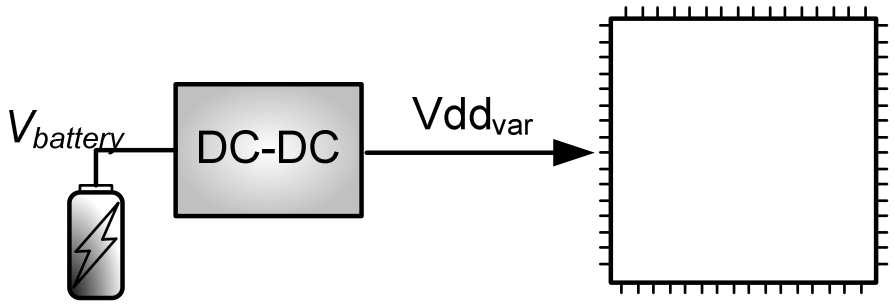
$t_d \approx C V dd/(Vdd - Vt)^{\alpha}$ $\quad$ $Vdd \downarrow \Rightarrow t_d \uparrow f_{max} \downarrow$

Reducing supply voltage:

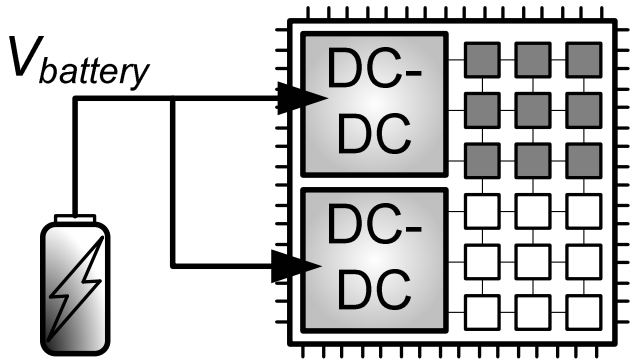
- Reduces power and energy dissipation
- Reduces maximum clock frequency due to increased gate delay

Other DVFS Schemes

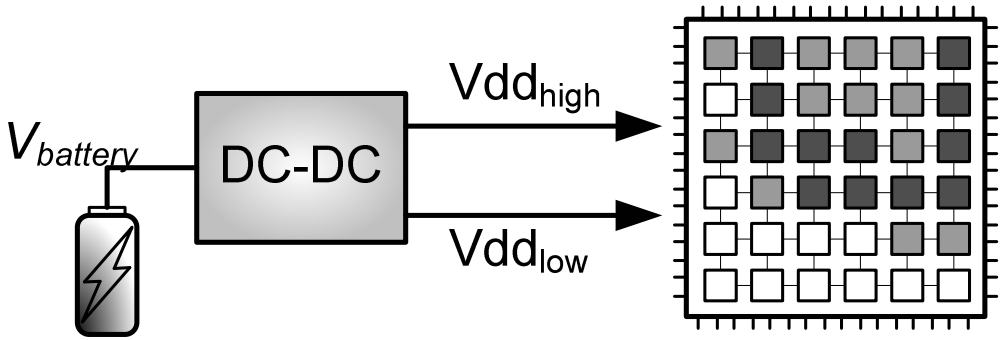
Scheme1: Off-chip DC-DC Converter



Scheme 2: On-chip DC-DC Converter



Presented DVFS Scheme



- Fine grain voltage scaling
  - Maximum power/energy reduction with minimum performance overhead
- Small area overhead by using an off-chip DC-DC converter, and switching between voltages on-chip

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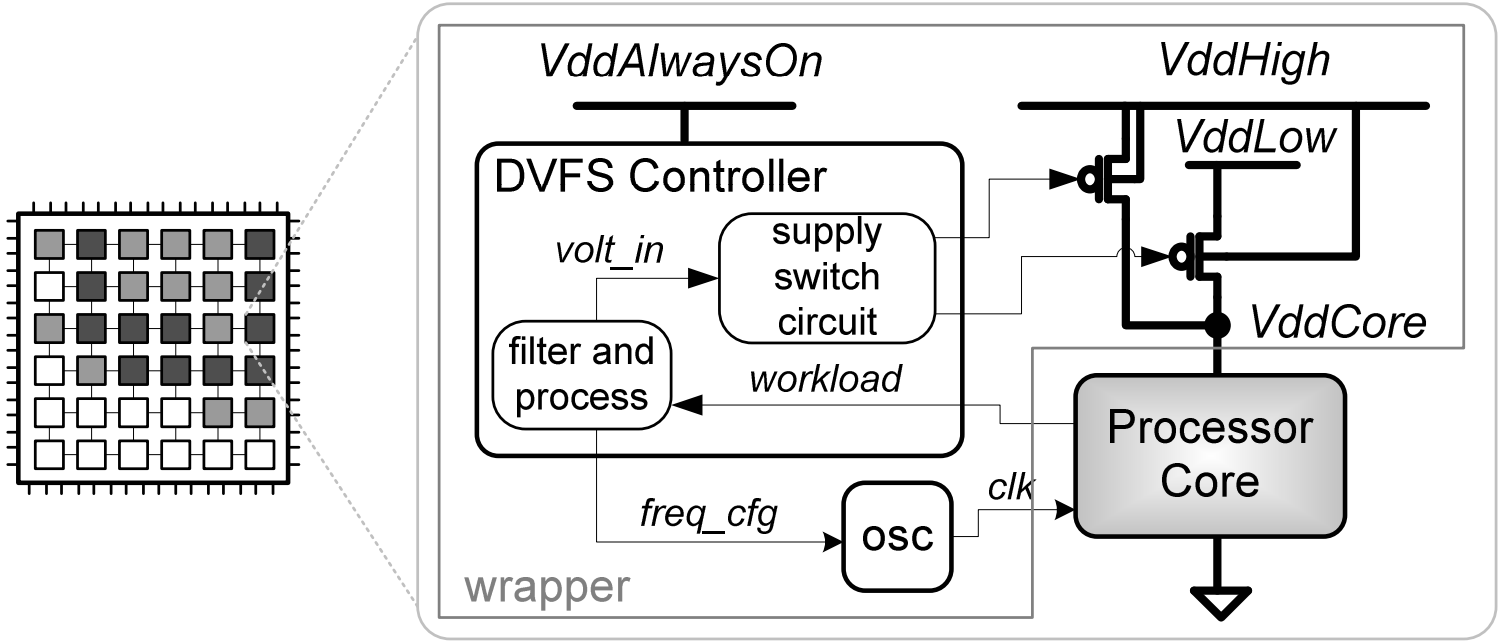
Implementation Schematic



- Voltage scaling with 2 discrete voltage levels
- Supply switching with PMOS power gates
- Automated DVFS based on workload
- Wrapper powered by always on power supply

Power Gate Sizing

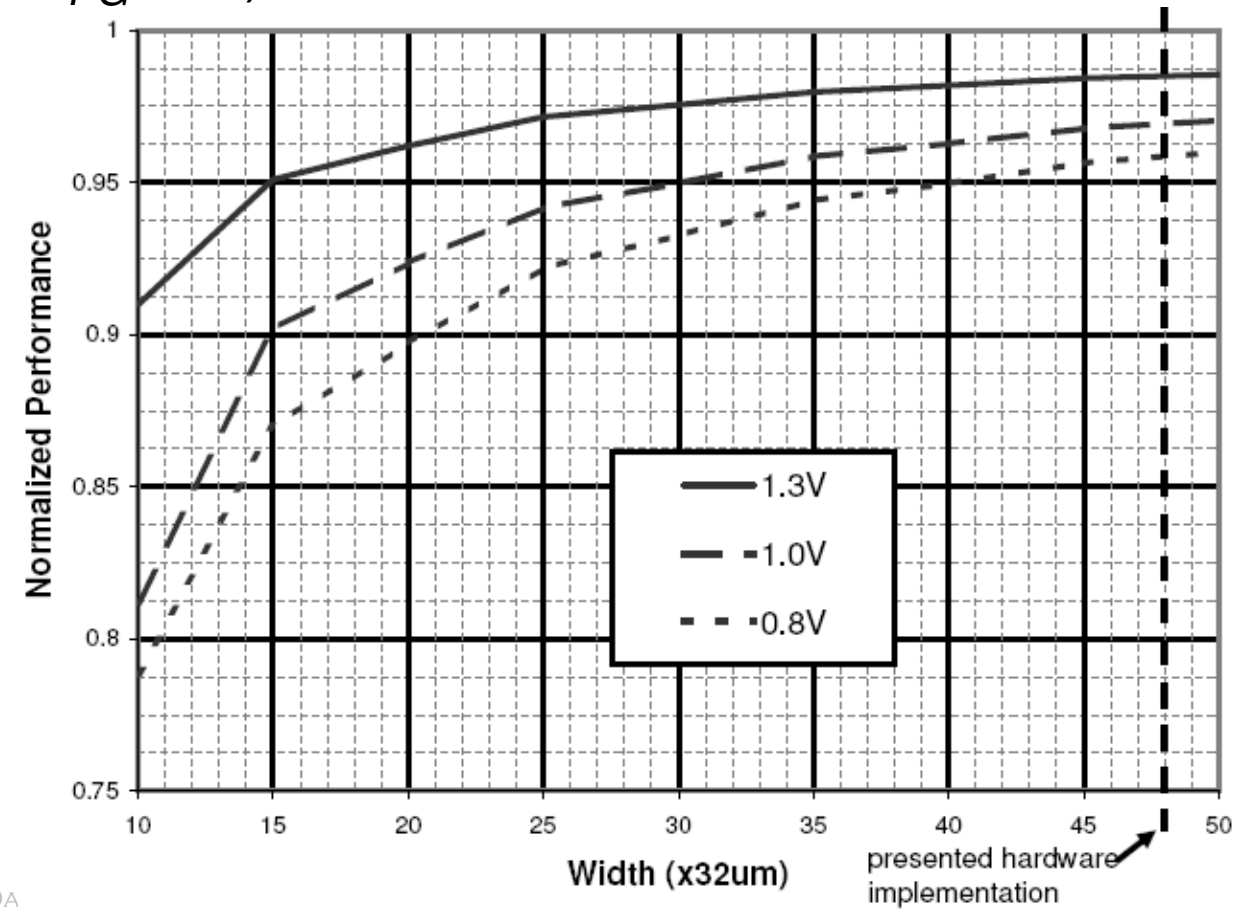
$V_{PG} = I_{PG}R_{PG}$

$R_{PG} \sim L/W$

$t_d \approx CVdd/(Vdd - V_{PG} - Vt)^{\alpha}$

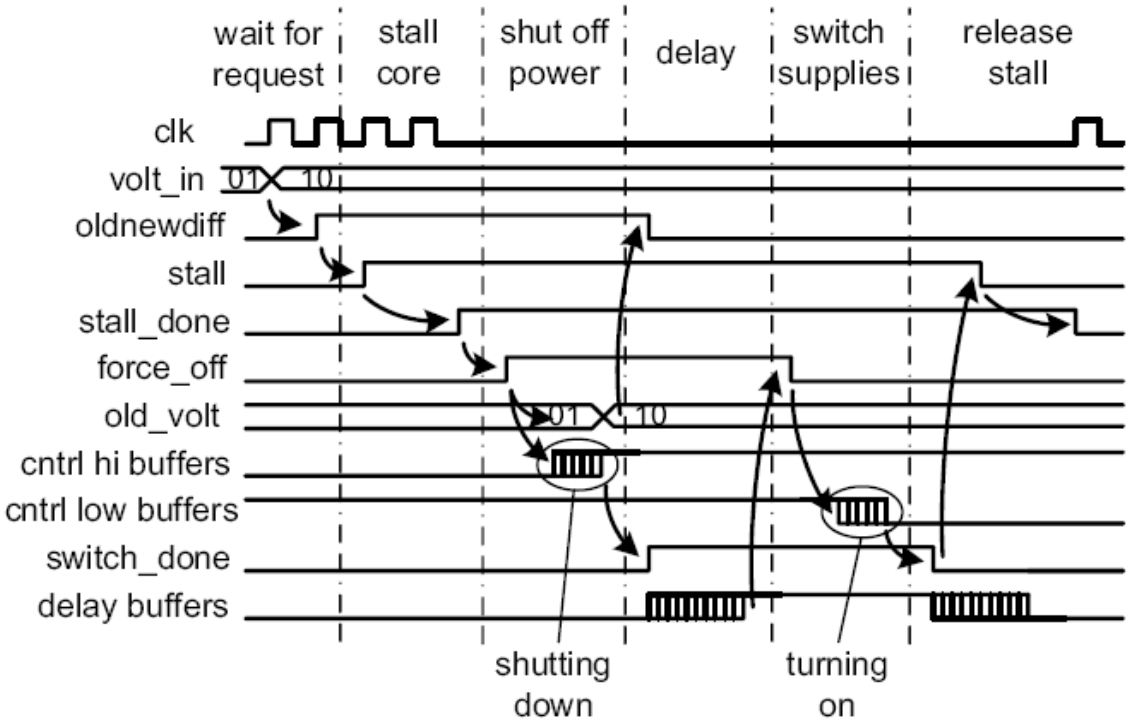
$W/L \uparrow\ V_{PG} \downarrow\ t_d \downarrow\ f_{max} \uparrow$

Voltage drop can be reduced by making *W/L* as large as possible → done by adding parallel power gates



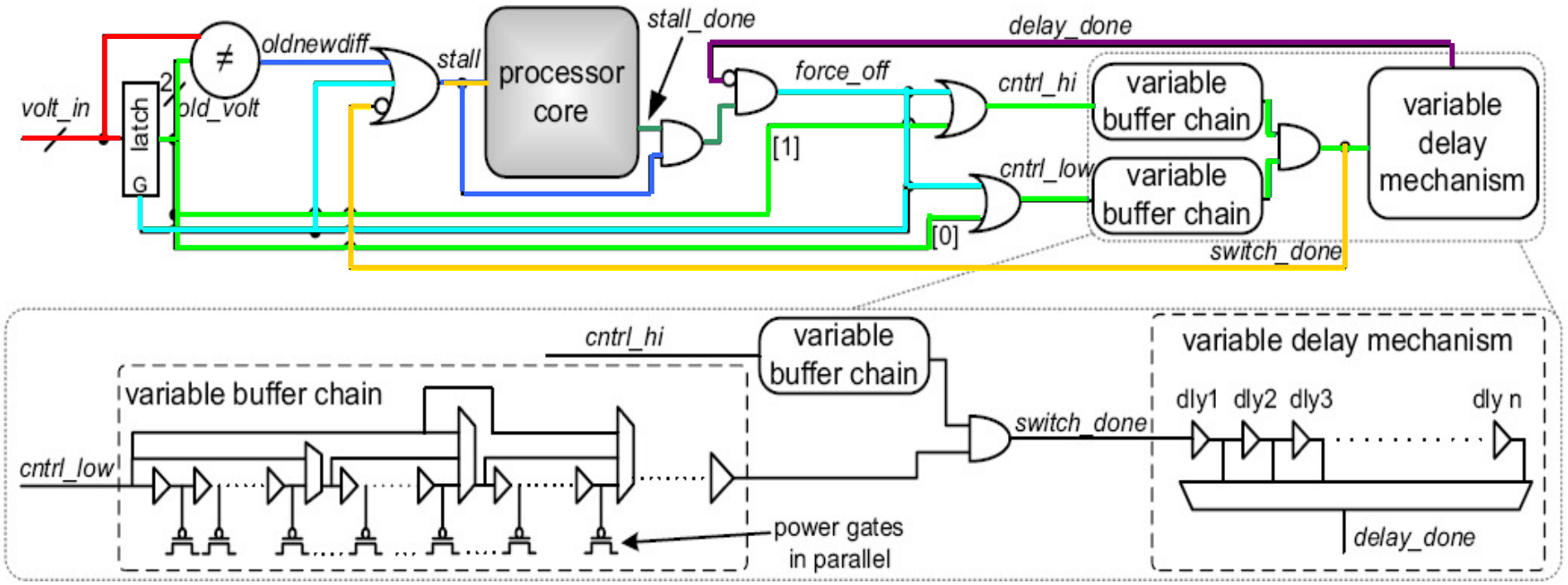
Supply Switching Scheme

- Supply grid noise:
  - Gradually switch between power supplies
- Shorting between power supplies:
  - Shut both power supplies off and wait for some time before switching
- Data corruption:
  - Stall the processor core before switching between power supplies

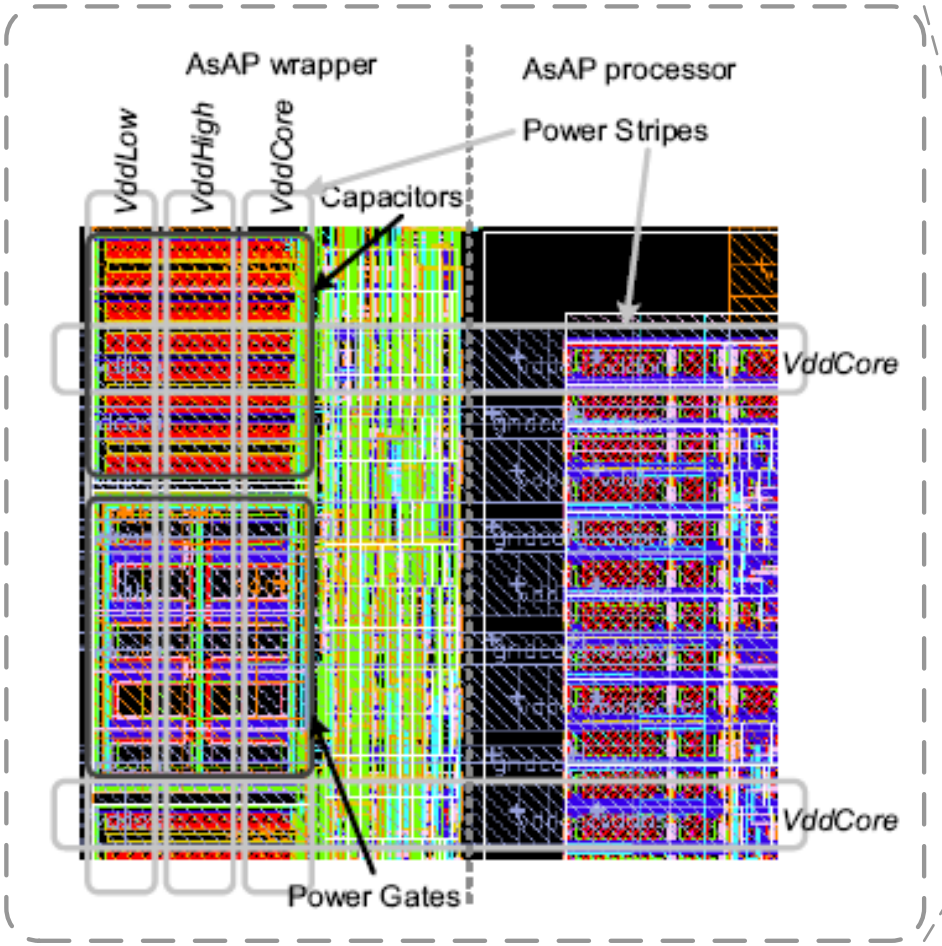


Dynamic Run-time Supply Switching Circuit

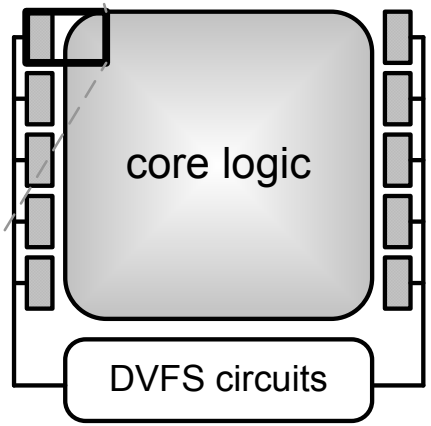
- Wait for request
- Stall core
- Shut off power
- Delay
- Supply switch
- Release stall



Physical Implementation



- Power gates are positioned along vertical power stripes
- Core power is supplied with horizontal power stripes



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Implementation Results

- Implemented in 65nm CMOS technology
- DVFS circuit area is 12% of AsAP processor's core area
- 66% of the DVFS circuit area is power gates and decoupling capacitors
- Maximum power consumption of DVFS logic is 4% of AsAP processor core's power

Energy Consumption Metric

- $P_{dyn} = \alpha C V dd^2 f$
- $E = C V dd^2$
- **Energy reduction is possible only with voltage scaling**

- $EDP = E * t_d$
- **Energy delay product measures the effect of increased delay with DVFS**

Measurement of Relative Energy Delay Product

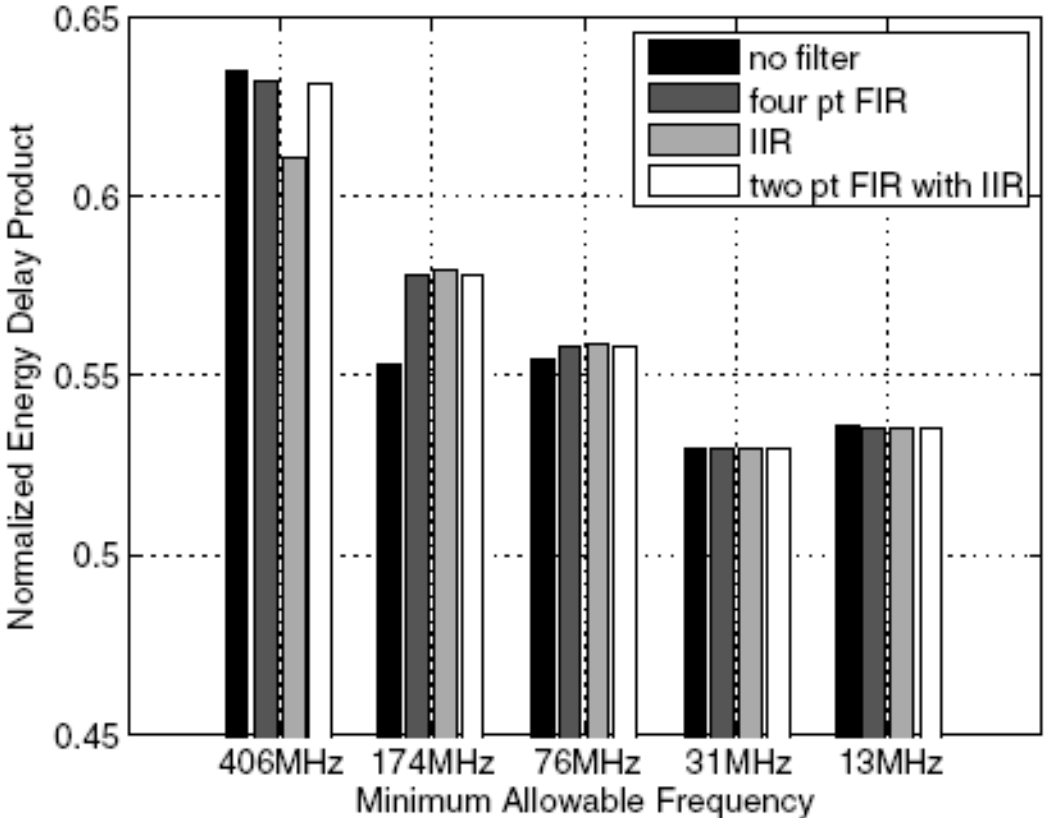
$$EDP_{rel} = \left(\frac{\beta Vdd_{Low}^2 + (1-\beta) Vdd_{High}^2}{Vdd_{High}^2} \right) \left(\frac{t_{dvfs}}{t_{orig}} \right)$$

- β is the fraction of time operating on the lower voltage
- t_{dvfs} is the total run time with DVFS
- t_{orig} is the total run time without DVFS.

9 Processor JPEG Application

Vddhigh = 1.3V, *Vddlow* = 0.8V
Maximum Frequency = 1.05 GHz

- Lower minimum frequency → Increase in time on lower supply
- *EDP* decreases as the minimum frequency decreases up until 13 MHz
- *EDP* increases as the performance overhead outweighs the energy savings



Various Applications

- *EDP* dependent on workload variations
- Increase in workload variation → Increase in switching between supplies → Increase in performance overhead → Increase in *EDP*

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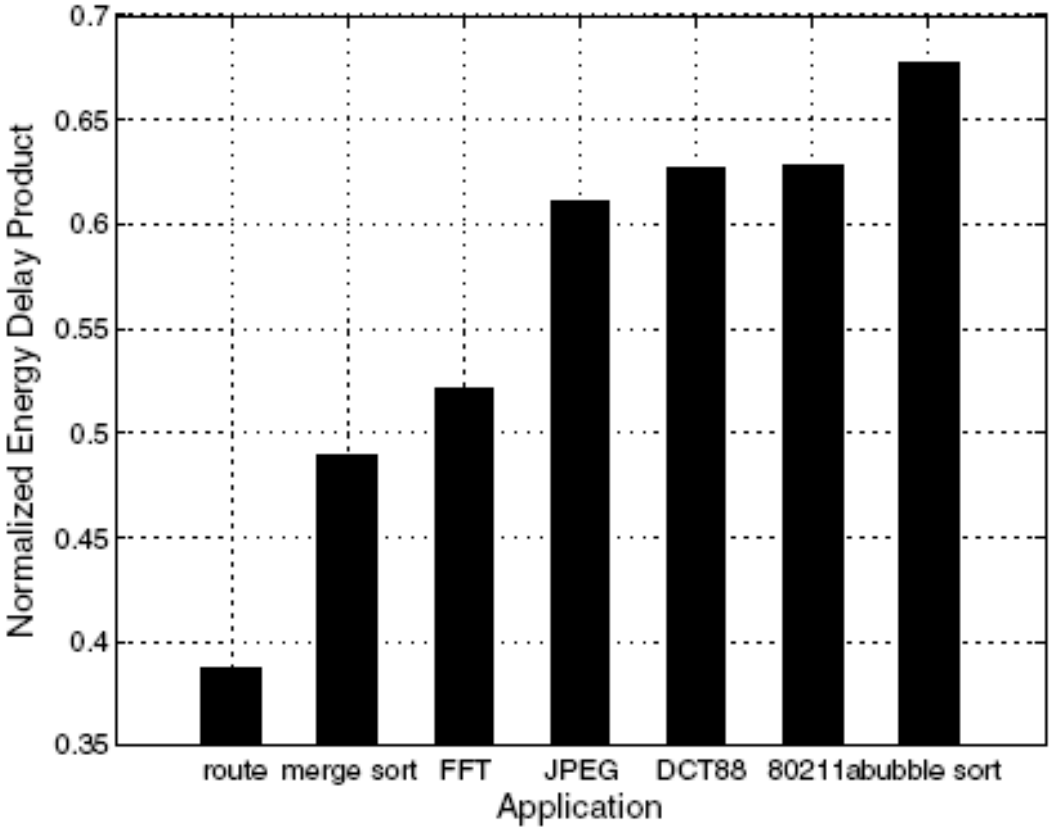
Maximum Frequency = 1.05 GHz



Summary

- DVFS with 2 supply voltages
- Power gates sized to reduce perf. loss
- Robust supply switching circuit
- EDP is reduced by 48% on a 9 processor JPEG application
- Functional in silicon at 65nm node

Acknowledgements

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