

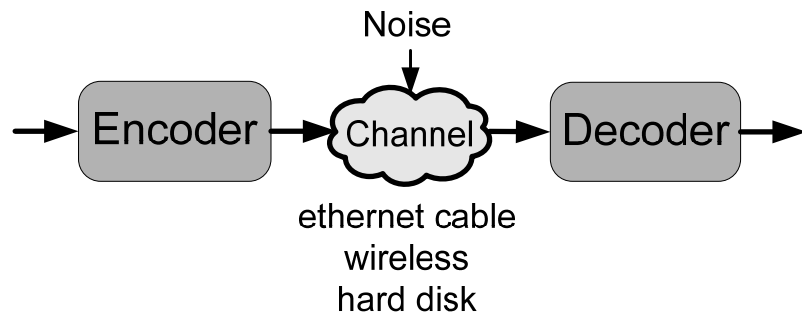
An 18 Gbps 2048-bit 10GBASE-T Ethernet LDPC Decoder



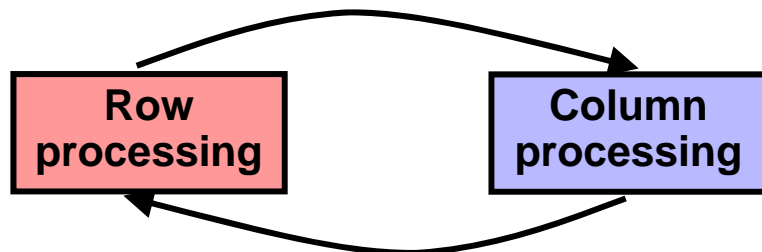
- Tinoosh Mohsenin
- Electrical & Computer Engineering, UC Davis
- tmohsenin@ucdavis.edu
- PhD, graduation date: 2008
- Adviser: Professor Bevan Baas
- Research areas
 - Energy efficient and high performance signal processing and error correction architectures
 - Multi-gigabit full-parallel LDPC decoders
 - Many-core processor architecture design

- UC Davis
- BS from Sharif University
- MS from Rice University

Research Overview



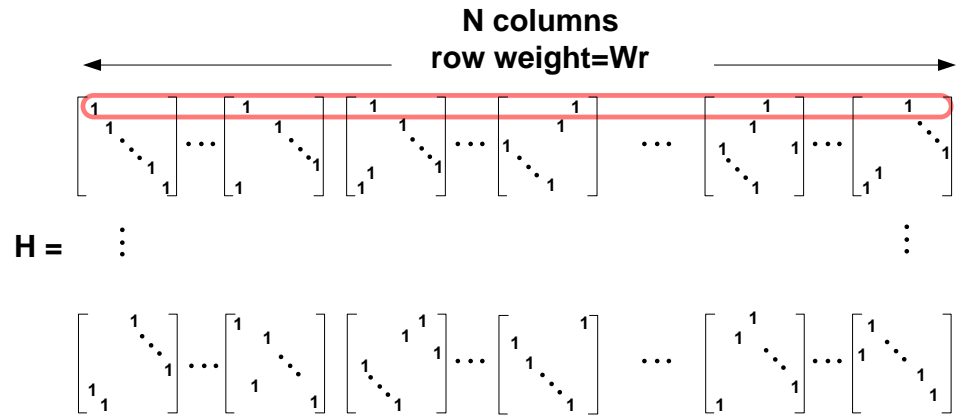
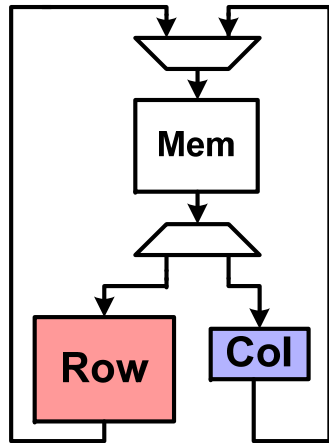
$$H = \begin{bmatrix} 0 & 0 & 1 & 1 & 0 & 0 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 0 & 0 & 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$



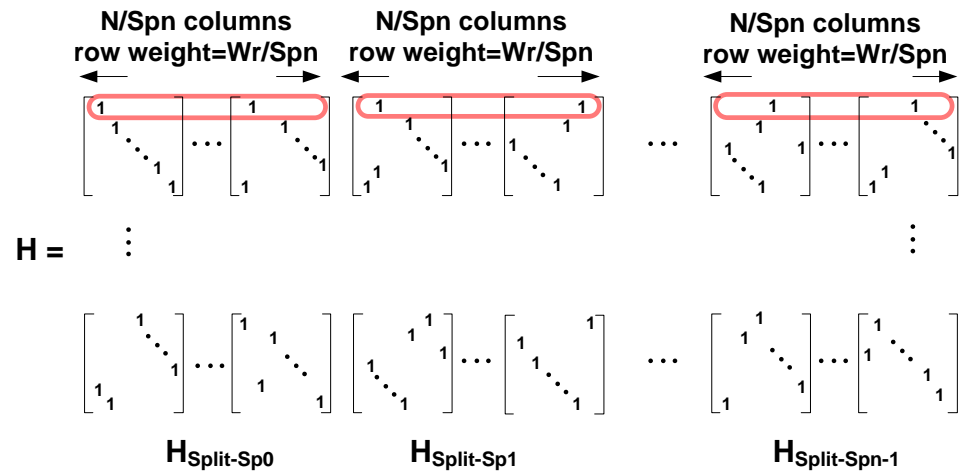
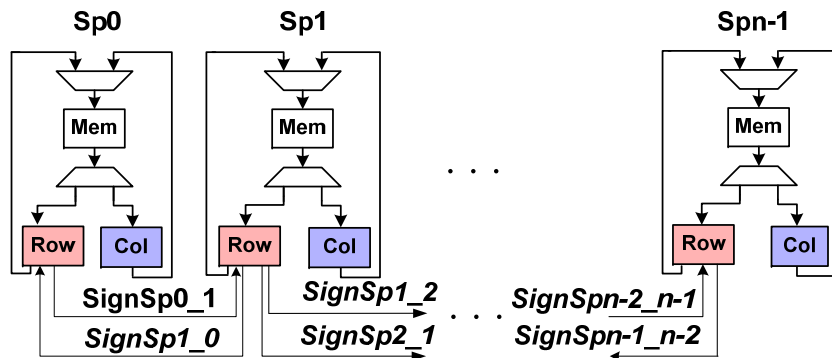
- Low Density Parity Check (LDPC) decoders
 - Algorithms
 - Architecture
 - High energy efficiency
 - High throughput
- LDPC codes applications
 - 10 Gigabit Ethernet (10GBASE-T)
 - WiMAX
 - Digital Video Broadcasting (DVB-S2)
- T. Mohsenin et al., *ICCD*, Oct 2006
- T. Mohsenin et al., *ICASSP*, Apr 2007
- A. Blanksby et al., *JSSC*, Mar 2002

Multi-Split-Row vs. Standard Decoder

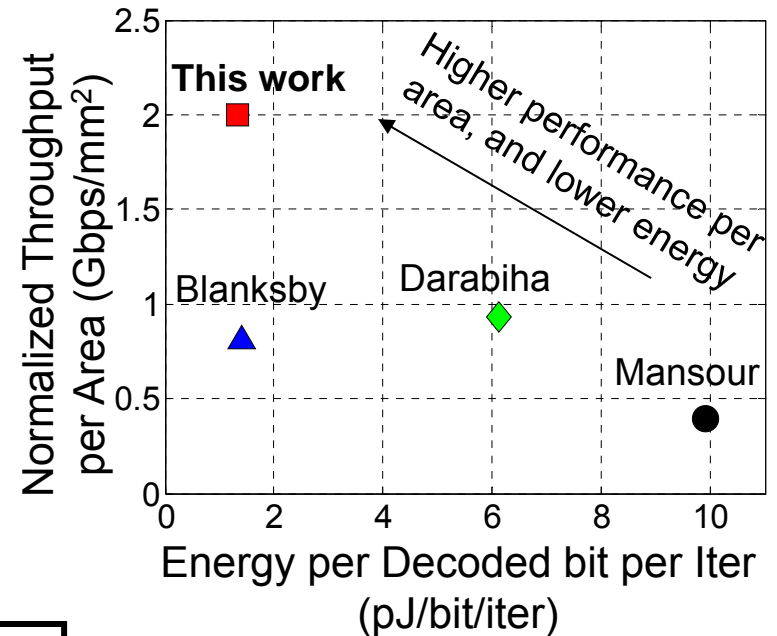
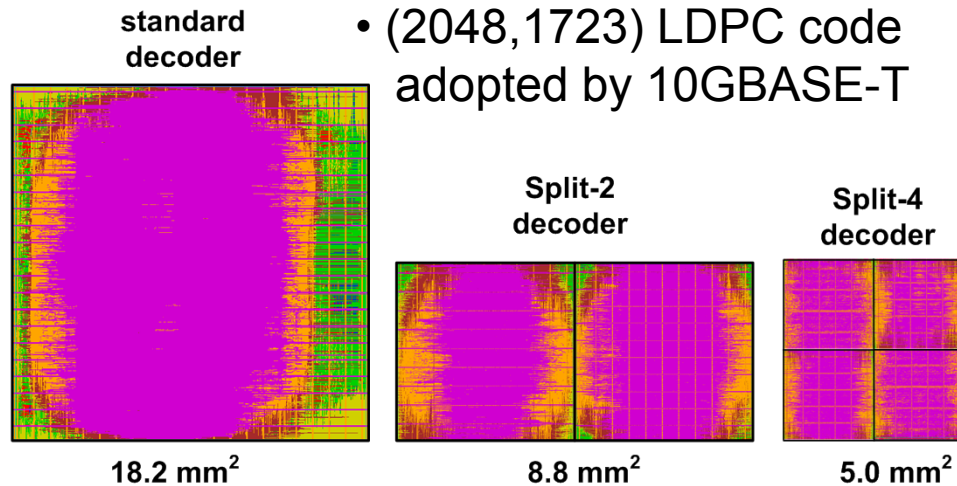
Standard decoder



Multi-Split-Row decoder



Decoder Implementation Results



10GBASE-T Code 65 nm, 1.3 V	Standard	Split-2	Split-4	Split-4 Improve.
Area Utilization	25%	50%	90%	3.6x
Avg. Wire length (μm)	175.2	115.5	73.8	2.4x
Speed (MHz)	12.5	45	133	10.6x
Throughput (Gbps)	1.7	6.1	18.2	10.6x
Energy per bit (pJ/bit)	141	79	46	3.1x

In the plot:

- 65 nm, 0.85 V
- Throughput normalized to 15 iterations
- Area: quadratically scaled with feature size, adjusted with row and column weights
- Speed: linearly scaled with feature size
- Energy: linearly scaled with feature size, quadratically scaled with voltage

[1] A. Blanksby et al., *JSSC*, Mar 2002

[2] M. Mansour et al., *JSSC*, Mar 2006

[3] A. Darabiha et al., *CICC*, Sep 2007